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Book One

Instruction Manual
for

ANDS5400

Modular A/D and D/A Data Acquisition & Distribution Systems with Digital I/O Capability

ANALOGIC®
...The Digitizers

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CONTENTS

Book One: Technical Guide to the ANDS5400 System

1. Introduction

1.0	General
1.1	Overview of ANDS5400 Instruction Manual
1.2	Configuration
1.2.1	Interface Selection
1.2.2	A/D Converter Selection
1.2.3	Analog Input Multiplexer Selection
1.2.4	D/A Converter Selection
1.2.5	Digital Input/Output Selection
1.2.6	Expansion Chassis Requirements
1.2.7	Power Consumption Characteristics
1.2.8	Typical Configuration
1.3	Typical Applications and Configurations
1.3.1	Example 1
1.3.2	Example 2
1.4	Conclusion

2. Installation

2.0	General
2.1	Environmental Conditions
2.2	Unpacking Instructions
2.3	Inspection
2.4	Pre-Installation Tests
2.5	Installation Procedures
2.6	System-Computer Integration
2.7	Remote Synchronization
2.8	Optional Power Supply Installation

3. Architectural Overview

3.0	General
3.1	Master Chassis
3.2	System Power Supply
3.3	Optional Power Supply
3.4	Internal Backplane
3.5	Display/Control Panel
3.6	User Card Backplane
3.7	Expansion Cards

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3.8 Local Front Panel Control and Display

3.9 Power

3.10 REMOTE/LOCAL Button

3.11 CLEAR Button

3.12 ANALOG Button

3.13 DYNAMIC Button

3.14 REQUEST Lite

3.15 DIGITAL Button

3.16 IN Button

3.17 OUT Button

3.18 DATA Display
3.18.1 Analog Data Interpretation
3.18.1.1 System Rules
3.18.1.2 Converter Rules
3.18.1.3 Octal-to-Decimal Conversions

3.19 RANGE Display

3.20 ADDRESS Display

3.21 Typical Local Control Front Panel Operations
3.21.1 Digital Output: Loading a D/A Converter
3.21.2 Digital Input: Reading a Digital Input Card
3.21.3 Analog Input: Reading an Analog Input Channel
3.21.4 Analog Input: Dynamic Operation
3.21.5 Digital Input: Reading Back the Range and Address Registers
3.21.6 Digital Input: Reading the Switch Register
3.21.7 Digital Input: Servicing a User Card Interrupt
3.21.8 Digital Output / Analog Input: Controlling SSH Cards
3.21.9 The CLEAR Button: System Initialization

4. Performance Enhancements

4.0 Introduction

4.1 Minimizing Measurement Errors
4.1.1 Single-Ended, Pseudo-Differential, or True Differential Signals
4.1.1.1 Single-Ended Signals
4.1.1.2 Pseudo-Differential Signals
4.1.1.3 True Differential Signals
4.1.2 Analog Signal Input Wiring
4.1.3 System Ground Connections
4.1.4 Source Impedance, System Leakage, and "Pump Out"
4.1.5 Common-Mode Constraints
4.1.6 Normal Mode Input Filtering

4.2 Accuracy Improvements
4.2.1 A/D Converter Resolution
4.2.1.1 Conversion Speed and Accuracy

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4.2.1.2 Stability
4.2.1.3 Repeatability
4.2.1.4 Noise Reduction
4.2.2 Periodic Calibration
4.2.3 Environmental Controls
4.2.4 User Card Locations
4.2.5 Slew Rate and Settling Time Error Reduction
4.2.6 Dielectric Absorption Error and Its Reduction
4.2.7 Noise and Quantization Reduction Through Signal Averaging
4.2.8 "OPEN" Channel Elimination
4.2.9 "REST" Channel Selection
4.2.10 Automatic Calibration
4.2.10.1 Automatic Calibration Techniques
4.2.10.1.1 Linearity Errors
4.2.10.1.2 Offset Errors
4.2.10.1.3 Gain Errors

4.3 Signal Averaging Using External Sync

4.4 Simultaneous Sample-and-Hold Timing Relationship
4.4.1 Dielectric Absorption in SSH Units

4.5 Programmable Gain – How and When to Use It
4.5.1 AC260 Signal Processor
4.5.2 AC261 Signal Processor
4.5.3 Comparison of AC260 and AC261 Signal Processors

4.6 Analog Output Connections

5. Maintenance & Calibration

5.0 General

5.1 Warranty and Maintenance Agreements
5.1.1 Supplemental Warranty
5.1.2 Extended Maintenance Agreement

5.2 Repair Technique

5.3 Calibration
5.3.1 Required Calibration Equipment
5.3.2 Adjustment Locations
5.3.3 Theory of Calibration
5.3.3.1 Computer Aided Calibration
5.3.3.2 System Performance Verification
5.3.3.2.1 Power Supply
5.3.3.2.2 A/D Converter
5.3.3.2.3 Signal Processor
5.3.3.2.4 Analog Input User Cards
5.3.3.2.5 Analog Output User Cards
5.3.3.2.6 Digital Input/Output User Cards
5.3.3.2.7 Special Considerations
5.3.3.2.8 User Card Calibration

5.4 Maintenance
5.4.1 Precautions
5.4.2 Disassembly Techniques

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5.5 Troubleshooting Strategy
5.5.1 Power Supply
5.5.2 Local Control
5.5.3 A/D Converter
5.5.4 Signal Processor
5.5.5 User Card Bus
5.5.6 Expansion Chassis
5.5.7 Interface

5.6 Spares Recommendation

6. Software Support

6.0 General
6.0.1 Interface Diagnostic Program
6.0.2 Self-Test Card Program
6.0.3 General Purpose Exerciser

6.1 Driver Packages for Custom Appication Programming
6.1.1 Assembly Language Driver
6.1.2 ANALIB FORTRAN Library

6.2 Diagnostic Programs

6.3 "SL" Software Packages for LSI-11 Based Systems
6.3.1 SL001 Self-Test Card Program
6.3.2 SL002 Interface (-18) Diagnostic
6.3.3 SL005 DEC FORTRAN IV
6.3.4 SL007 DEC RT-11
6.3.5 SL010 -18 Interface Driver
6.3.6 SL013 DAC Diagnostic and Test Program
6.3.7 SL014 Frequency Counter Diagnostic and Test Program
6.3.8 SL015 Change of State (COS) Diagnostic and Test Program
6.3.9 SL016 Bridge Completion (Strain Gauge) Card Diagnostic and Test Program
6.3.10 SL018 General Purpose Exerciser

6.4 "SP" Software Packages for PDP-11 Based Systems
6.4.1 SP001 Self-Test Program
6.4.2 SP002 -31 Interface Diagnostic
6.4.3 SP010 -31 Interface Driver
6.4.4 SP013 DAC Diagnostic and Test Program
6.4.5 SP014 Frequency Counter Diagnostic and Test Program
6.4.6 SP015 Change of State Diagnostic and Test Program
6.4.7 SP016 Bridge Completion (Strain Gauge) Diagnostic and Test Program
6.4.8 SP018 General Purpose Exerciser

7. Drawings and Specifications

7.0 General

7.1 Mechanical

7.2 Cables

7.3 Internal Backplane
7.3.0 General
7.3.1 Power Distribution
7.3.2 Optional Power Supply

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7.4	Interfaces
7.4.0	General
7.4.1	Interface Operation Overview
7.4.2	Slot Connections
7.4.2.1	J75 (MSB Data Latch) Slot Connections
7.4.2.2	J76 (LSB Data Latch) Slot Connections
7.4.2.3	J77 (Interface Control) Slot Connections
7.4.2.4	J78 (DMA Control) Slot Connections
7.5	Signal Processor and A/D Converter
7.5.0	General
7.5.1	J73 (Signal Processor) Slot Connections
7.5.2	J74 (A/D Converter) Slot Connections
7.6	Front Panel
7.6.0	General
7.6.1	Connector J84
7.6.2	Connector J83
7.6.3	Logic Elements
7.6.4	Interface Signal Blocking in "Local" Control
7.6.5	Local/Remote Selection
7.6.6	A/D or D/A Mode Selection
7.6.7	User Card Interrupt Requests
7.6.8	Address Register Loading
7.6.9	Range Register Loading
7.6.10	Address and Range Register Readback
7.6.11	Address Register Incrementing
7.6.12	Front Panel Digiswitch Readback
7.6.13	Digital Input and Output Modes
7.6.14	Digital or ADC Indicator Lites
7.6.15	CLEAR Signals
7.6.16	Local Oscillator
7.6.17	DYNAMIC Mode
7.6.18	Digital Strobe Pulses and SSH Control
7.6.19	Address Register Display
7.6.20	DATA Display
7.6.21	Range Register Display
7.6.22	Range Register Decoding
7.6.23	Front Panel Address Board
7.6.24	Digiswitches and Drivers
7.6.25	Address and Range Registers
7.6.26	DATA Display Multiplexer
7.6.27	A/D and D/A Decoding
7.6.28	Standard Decoding Chart (A/D 32/16 channels; D/A 4 channels)
7.6.29	System Addressing
7.6.29.0	General
7.6.29.1	Address Mode Format
7.6.29.2	Analog Mode Addressing
7.6.29.3	Digital Mode Addressing
7.6.29.4	Address Patch
7.6.29.5	Address Interpretation
7.6.29.6	Single-Ended/Differential Operation
7.6.29.7	Absolute Analog Addressing
7.6.29.8	Absolute Digital Addresses
7.6.29.9	Addressing Sample

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7.7 User Card Backplane
7.7.0 General
7.7.1 User Card Bus Pin Connections
7.7.2 User Card Address Bus
7.7.3 User Card Digital Bus
7.7.4 User Card Analog Bus
7.7.5 Digital Control Lines
7.7.5.1 $\overline{\text{CLR2}}$
7.7.5.2 DIG STROBE
7.7.5.3 RDUSR
7.7.5.4 $\overline{\text{BOX REQUEST}}$
7.7.5.5 PRIORITY IN
7.7.5.6 PRIORITY OUT

7.8 Expansion Cards
7.8.0 General
7.8.1 AC333 Expansion Card Theory of Operation
7.8.1.1 Typical Operation
7.8.1.2 Interrupt Structure
7.8.2 AC334 Expansion Chassis Expansion Card Theory of Operation
7.8.2.1 Typical Operation
7.8.2.2 Interrupt Structure

8. Quality Conformance

8.0 General

8.1 Quality of Design
8.1.1 Product Design
8.1.2 Component Specifications
8.1.3 Documentation

8.2 Quality of Components
8.2.1 Purchasing
8.2.2 Incoming Inspection
8.2.3 Storage

8.3 Quality of Manufacturing

8.4 Warranty and Field Return

Book Two: ANDS5400 User Card Documentation

9. Introduction

10. Analog Multiplexers

11. D/A Converters

12. Digital Input

13. Digital Output

14. Self-Test Card

15. I/O Cable Assemblies

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Tables and Figures in ANDS5400 Instruction Manual

Figure or Table Number	Title	Page
1-1	Configuration Guide	1-2
1-1	Interface Table	1-4
1-2	Signal Processor — ADC Matrix	1-4
1-3	Multiplexer Accuracy Matrix	1-5
1-4	DAC Matrix	1-6
1-5	Digital Input Matrix	1-6
1-6	Digital Output Matrix	1-6
1-7	User Card Power Consumption	1-7
1-2	Typical Configuration Guide Filled Out	1-8
2-1	Master Chassis	2-2
2-2	Expansion Chassis	2-2
2-3	Chassis Slide Rail Mounting	2-3
2-4	Connections to Rear of Master Chassis	2-4
2-5	Expansion Chassis Interconnections	2-5
2-6	J28 Pinout and Signals	2-6
2-7	User-Controlled Sample-and-Hold Timing	2-7
2-8	Etch Cuts for AN3500 Power Supply Installation	2-8
2-9	Installation of Optional Power Supply	2-9
3-1	Block Diagram of ANDS5400 System	3-2
3-2	Front Panel Controls and Display	3-8
3-3	Functions in "Local" and "Remote" Modes	3-9
3-1	Converter Examples	3-5
5-1	Modified Extender Board	5-3
5-2	Modified Extender Board Schematic	5-4
7-1	Single Supply Master Chassis	7-4
7-2	Single Supply Expansion Chassis	7-4
7-3	Dual Supply in the Master Chassis	7-4
7-4	Dual Supply in an Expansion Chassis	7-4
7-1	System Address Map	7-26
7-2	Address Register Bit Interpretation	7-26
7-3	Analog Address Map	7-27
7-4	Digital Input / Digital Output Address Map	7-28
7-5	Analog Input Address	7-28
7-6	Digital Input, Digital Output (Analog Output) Address	7-28
7-7	Absolute Analog Address	7-28
7-8	Absolute Digital Input, Digital Output (Analog Output) Address	7-28
7-9	Example Absolute Address Map	7-29
7-11	User Card Address Bus	7-32
7-12	Chassis Address Decoding	7-35
9-1	User Card Power Consumption	9-2

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1
INTRODUCTION

1.0 General

The ANDS5400 is one of the most versatile, flexible, and powerful data acquisition/data distribution systems available. It has a unique design philosophy and architecture whereby the customer designs a specific system by selecting a signal processor, an A/D converter, and up to 128 user cards, all of which are assembled by Analogic into a completely integrated, fully computer tested, UL Approved device. The range of components from which the user may select is continuously evolving, adding more capability to the system's applications.

The analog I/O user cards vary from simple FET multiplexers to completely isolated low level input units that can operate easily within a 300 volt rms Common Mode environment while providing a 140dB minimum Common Mode Rejection Ratio. The digital input user cards, available in TTL or optically isolated configurations, have a unique interrupt scheme that permits some of the cards to generate an interrupt for priority handling by the computer. The signal processor features both unity and programmable gain; the resolution of the A/D converter ranges from 12 to 16 bits; and the analog output devices include D/A converters ranging in resolution from 12 to 16 bits with various combinations of voltage and current outputs. Digital outputs are available in TTL, optically isolated, and contact closure versions. The ANDS5400 interfaces to a wide variety of computers, using serial line devices, IEEE 488-1975 compatible units, and programmed I/O/DMA devices.

In its fully expanded configuration the system can provide more than 4000 analog or digital inputs or digital outputs, and its unique architecture permits the analog or digital functions to be included in any one of the possible eight chassis.

1.1 Overview of the ANDS5400 Instruction Manual

This manual is divided into two books. Book One discusses the overall operation of the data acquisition/data distribution system in the following eight chapters: "Introduction," "Installation," "Architectural Overview," "Performance Enhancements," "Maintenance and Calibration," "Software Support," "Drawings and Specifications," and "Quality Conformance." This book offers complete information on all components internal to the system; i.e. interfaces, front panel and control, A/D converter, signal processor, internal backplane, power supply, and expansion modules. Book Two, providing documentation on over 80 analog and digital I/O user cards, is divided into six chapters: "Analog Multiplexers," "D/A Converters," "Digital Input," "Digital Output," "Self-Test Card," and "I/O Cable Assemblies."

After reading this introduction the customer should proceed immediately to the "Installation" chapter and "Quality Conformance" chapter, which contains the computer-based test results, the configuration guide of the user's particular system, and the manual registration card. To ensure the continuous updating of this manual as our product line expands, the customer should fill out the manual registration card and return it to Analogic.

In many cases, much of the information in this manual will be of limited use to the customer as it does not apply directly to every unique configuration. However, the purpose of this manual is to document all possible configurations of the system, thus assuring that the user will have the necessary information to expand or modify the system later.

The "Installation," "Architectural Overview," "Performance Enhancements," and "Maintenance and Calibration," chapters thoroughly document the methodology of the system. A close reading of the "Front Panel" and "Expansion Card" sections of the "Drawings and Specifications" chapter is strongly recommended.

1.2 Configuration

Using the seven basic steps outlined below (sections 1.2.1 through 1.2.7), the user selects the particular combination of components required for a specific application.

1.2.1 Interface Selection

Interface selection/design is one of the most problematic areas of a data acquisition system. However, through the use of a standardized I/O interface structure, the ANDS5400 system connects easily to five styles of computer interfaces:

- Programmed I/O/DMA Interfaces
- Programmed I/O Handshake Interfaces
- Serial Line Interfaces, including RS232, RS422, Current Loop and IEEE 488-1975 Interface
- 2 Byte 8 Bit Handshake Interface
- Buffered Control Line Interface

The user should refer to Table 1-1 and designate the appropriate interface by inserting the corresponding number in the box labeled "Interface" on the configuration guide (see Figure 1-1). With the Programmed I/O Handshake, 2 Byte 8 Bit, and Buffered Control Interfaces, the user must also indicate with the A/B subscript on the configuration guide whether the device is to be terminated or unterminated.

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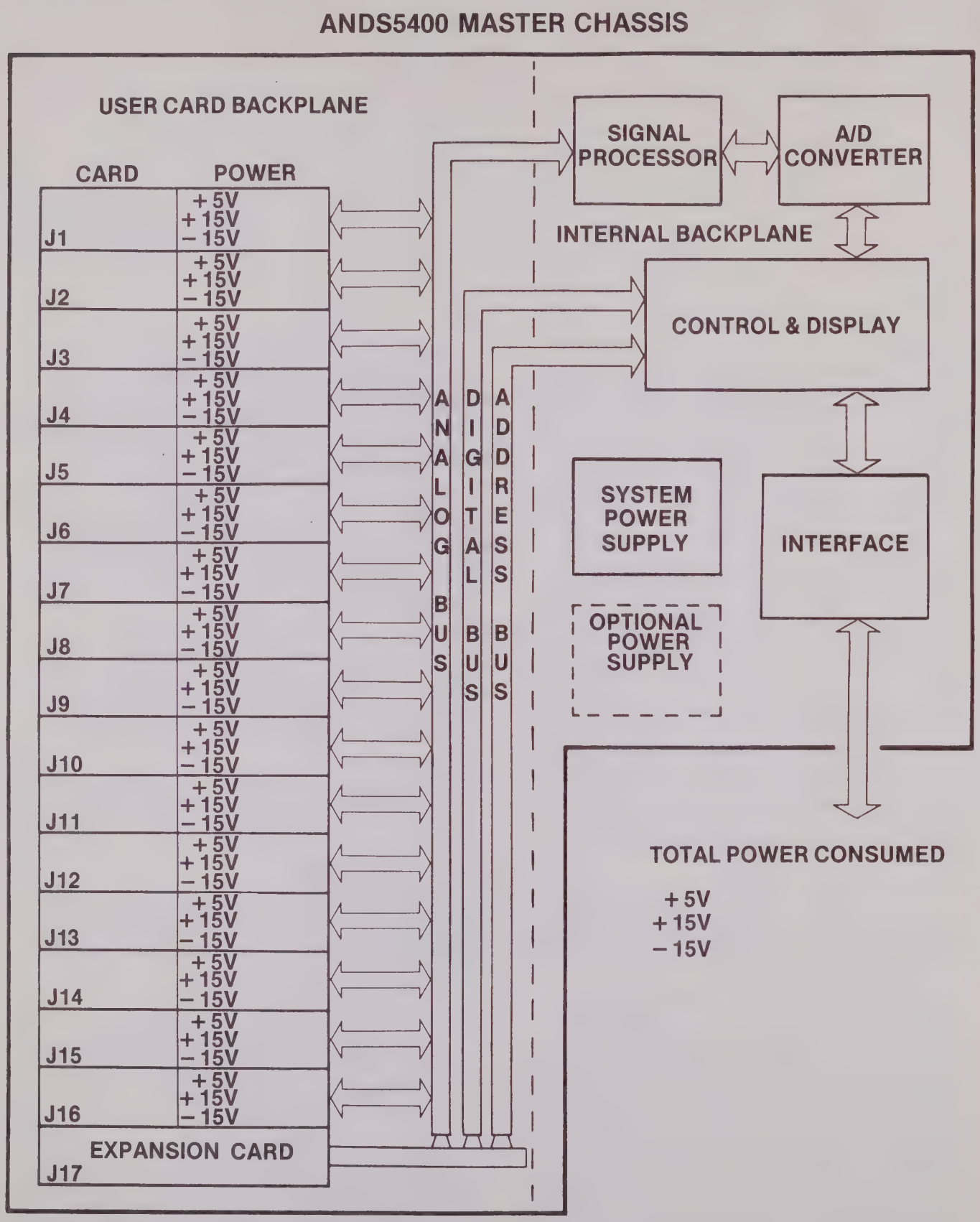

Figure 1-1 Configuration Guide

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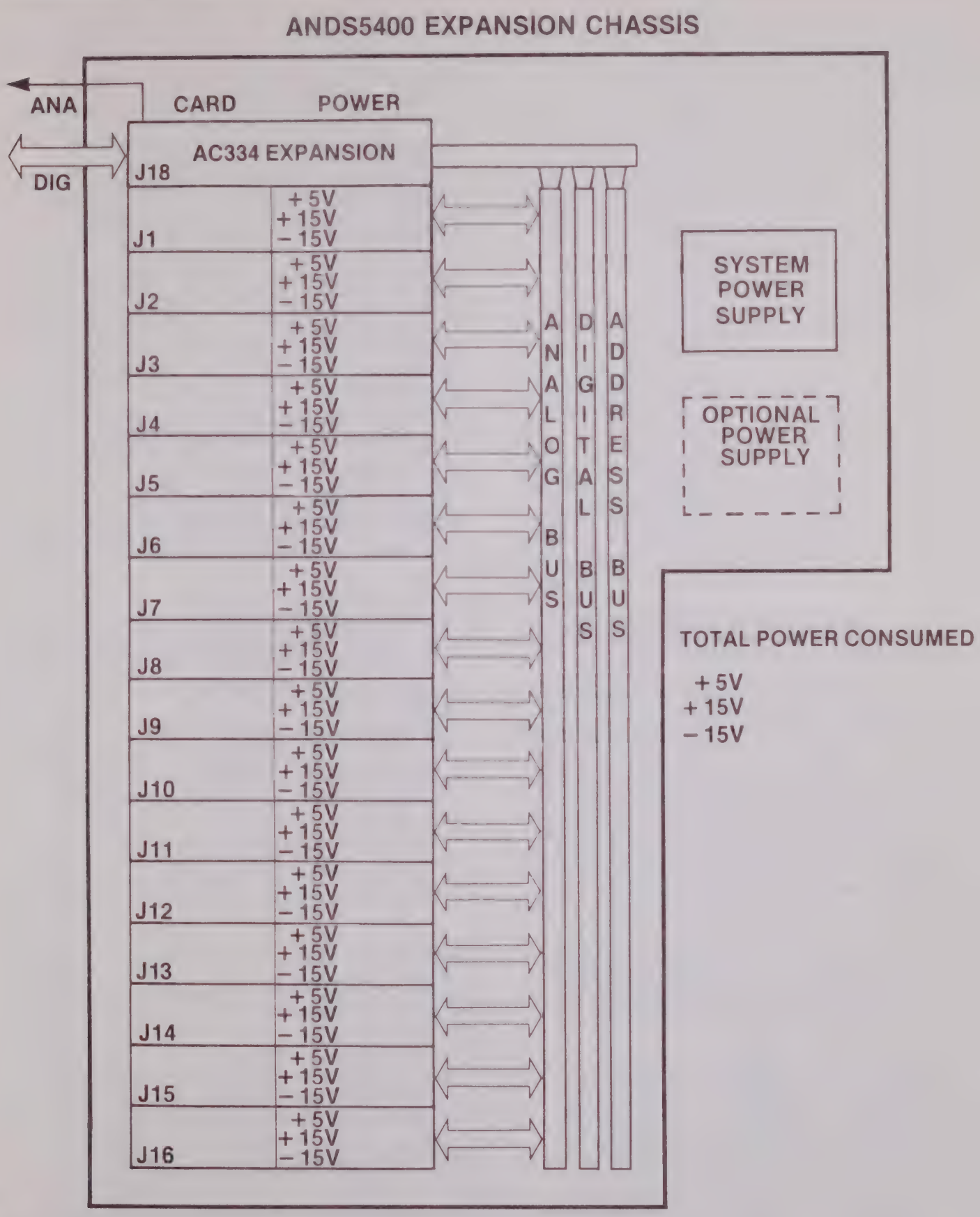

Figure 1-1 Configuration Guide

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Table 1-1 Interface Table

ANDS5400 Model Number	Potential Throughput Rate [1]	Description
-02	75kHz	DMA/PIO Interface for Nova/Eclipse Computers
-13	200Hz	IEEE 488-1975 Standard Bus Interface
-18	95kHz	LSI-11 DMA/PIO Interface for DEC Q Bus Equipment
-19 A/B [2]	100kHz	Buffered Control Line Interface (requires user designed device to generate control line signals; PI/O or DMA is determined by the user)
-23 A/B [2]	70kHz [3]	DEC DRV11 or DR11 Compatible PI/O Operation
-24 A/B [2]	70kHz [3]	HP 12566B-002 Compatible PI/O Operation
-25 A/B [2]	70kHz [3]	SPC16 I/O Module Compatible PI/O Operation
-26 A/B [2]	70kHz [3]	TI 960, 980, 990 Compatible PI/O Operation
-27 A/B [2]	70kHz [3]	Modular Computer Compatible via 4805 I/O Module
-28 A/B [2]	70kHz [3]	Interdata 3, 4, 5, and 70 UIM Module Compatible PI/O Operation
-29 A/B [2]	70kHz [3]	CA Alpha Naked Mini Compatible PI/O Operation
-30	200Hz	RS232 Serial Line Interface Baud Rates to 19.2K
-31	85kHz	PDP-11 DMA/PIO Interface for DEC Unibus Computers
-32 A/B [2]	70kHz [3]	Nova/Eclipse 4065 Compatible PI/O Operation
-34 A/B [2]	70kHz [3]	General Purpose Interface for 16 bit I/O Handshake PI/O Operation
-35	40kHz [3]	2 Byte, 8 Bit I/O Handshake PI/O Operation
-36	200Hz	RS422 Serial Line Interface PI/O Operation
-37	200Hz	20mA Current Loop Serial Line Interface PI/O Operation

[1] These throughput rates are based on a system with a 12 bit A/D converter, a unity gain sample-and-hold, and efficient programming techniques. Systems with higher resolution converters or programmable gain signal processors will have lower effective throughput rates.

[2] "A/B" indicates that the interface is available in terminated and unterminated versions.

[3] This approximate throughput rate is completely dependent on the efficiency of the program.

The base throughput rate referred to in Table 1-2 is the maximum rate at which the system can make conversions completely exclusive of the computer hardware and software; it represents the actual amount of time the system needs to make a conversion once it has been requested. Table 1-1 lists the system throughput rates that should be attainable if efficient software is written to drive the interface. However, these rates cannot be guaranteed since the actual throughput rate of the entire installation is determined by many factors, including priority assignment, interrupt handling, etc., that are outside the control of the ANDS5400. For further information on particular interfaces, refer to the "Interface" section of the "Drawings and Specifications" chapter.

1.2.2 Analog-to-Digital Conversion Selection

Each system using analog-to-digital (A/D) inputs requires an A/D converter and a signal processor module. All analog inputs in the master and expansion chassis (if required) are directed to the signal processor and A/D converter via a unique "spidered" analog expansion technique for up to seven expansion chassis.

To select the devices that will meet your speed and resolution requirements, refer to Table 1-2. The A/D converter's resolution, according to Analogic's part designation, is indicated by the last two digits of the part number; thus, the AC2712 has 12 bit resolution, and the AC8016 16 bit resolution. Proper use of Table 1-2 allows the customer to select cost-effective devices that offer maximum flexibility and optimal performance in a particular application.

Table 1-2 Signal Processor — ADC Matrix

ADC	Signal Processor		
	AC260	AC261*	AC262
AC2712	50kHz	83/22kHz	100kHz
AC2713	38kHz	55/18kHz	60kHz
AC2714	38kHz	42/15kHz	60kHz
AC8014	38kHz	42/15kHz	60kHz
AC8015	30kHz	25/12kHz	40kHz
AC8016	18kHz	24/11kHz	23kHz

Note that the conversion speeds indicated in this table are the maximum rates achievable with the -19 Interface; with any other interface the rates will be lower.

* Because of the variable settling time function of the AC261, there are dual throughput rates listed, one for unity gain (X1) and one for a gain of 32 (X32).

If analog-to-digital conversion is not required, proceed directly to section 1.2.4. Note that if analog multiplexing/conversion is required subsequent to the initial installation, the necessary devices can easily be plugged into the system to add this capability.

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There are three signal processor devices available in the ANDS5400 product line: the AC260, which is a programmable gain amplifier and a sample-and-hold with a fixed-rate settling circuit; the AC261, a programmable gain and a sample-and-hold with a variable rate settling function; and the AC262, a high speed unity gain amplifier and a sample-and-hold. The AC260 provides programmable gains of one, two, four, and eight, with a fixed period of autozeroing that compensates for thermal offsets within the signal processor. The AC261 provides gains of one, two, four, eight, sixteen, and thirty-two, with a programmable filter and variable rate to allow the appropriate input/amplifier settling time necessary with a wide range programmable gain amplifier.

Table 1-2 lists the conversion times according to the A/D converter resolution and signal processor selected. The AC262 signal processor, used with any A/D converter, provides the maximum base throughput rates. The AC260 provides lower conversion rates but with greater input gain flexibility; the AC261 potentially provides the lowest conversion rates but with even greater input gain flexibility.

The base throughput rates described in Table 1-2 indicate the time the system needs to complete a conversion. They are exclusive of the software overhead necessary to implement them and of computer latencies that may be involved in the overall computer/system operation. In the case of the AC261, with its variable settling function, the times indicated are the maximum times needed with unity gain or a gain of 32 and with the particular A/D converter resolution selected.

Due to the computer architecture (instruction cycle, etc.) and computer interface hardware, the actual system throughput rates may be significantly less than the base throughput rates indicated in Table 1-2. For example, the general purpose (parallel) interface operated under interrupt software or the RS232 and IEEE (serial or byte serial) interfaces, both of which normally are limited by the computer hardware and software to less than 300Hz, have lower base throughput rates than those indicated in the table. The most efficient operation in terms of speed is obtained by programmed I/O operation dedicated to the data acquisition system or by direct memory access (DMA), where data transfers are relatively transparent and independent of the operation of the customer's computer.

Once the proper devices have been selected, insert their model numbers in the appropriate slots in the configuration guide.

1.2.3 Analog Input Multiplexer Selection

Table 1-3 delineates analog input multiplexers compatible with all systems. The multiplexer cards may be installed in any combination with other I/O user cards in the ANDS5400 chassis. The primary criteria for selection of a particular input multiplexer is determined by the type of transducer and the magnitude of the signal that must be sent to the computer. Requirements such as Common Mode Voltage, Common Mode Rejection Ratio, filter characteristics, etc. normally reduce the number of potential candidates. The user should refer to the ANDS5400 brochure for generalized specifications or to the ANDS5400 data sheet book for specific characteristics of individual analog input multiplexers. Table 1-3 indicates the type of multiplexer, the number of channels per card, and the accuracies with varying A/D converter resolutions. The errors generated by the signal processor and A/D converter are incorporated into the accuracy specifications.

The accuracy matrix describes input-to-output accuracy with respect to the input of the multiplexer channel in question. The accuracy specifications are based on a ±10V input to the A/D converter. The first number in any column indicates the typical accuracy, and the second number indicates the maximum error in systems operating under adverse environmental conditions. Some of the multiplexers listed in the table are limited to a 12 bit throughput accuracy. However, it has been our experience in the majority of installations that, although the performance of these devices cannot be calculated beyond 12 bits, they actually do provide accuracy to 14 bits.

Once the type and number of units have been selected, record the appropriate quantities of each device, one per slot (J1-J16), in the configuration guide.

1.2.4 Digital-to-Analog Converter Selection

Table 1-4 presents the characteristics of various digital-to-analog (D/A) converters offered in the ANDS5400 product line. D/A converters may be installed in any combination with other I/O cards used in the system. This table provides the most commonly required specifications. Where further specifications are required, the user should refer to either the ANDS5400 brochure or the specific data sheet on the product in question in the ANDS5400 data sheet book. Having selected the type of unit(s) to be used, record the appropriate quantities of each device, one per slot (J1-J16), in the configuration guide.

Table 1-3 Multiplexer Accuracy Matrix

Product	Channels Per Card	ADC Resolution 12 BITS	13 BITS	14 BITS	15 BITS	16 BITS
AC280	4	.01/.03	.01/.03	.01/.03	.01/.03	.01/.03
AC281	4	.01/.03	.005/.02	.005/.01	.005/.01	.005/.01
AC405X	4	.01/.05	.008/.05	.008/.05	.008/.05	.008/.05
AC407X	4	.01/.05	.008/.05	.008/.05	.008/.05	.008/.05
AC425X	4	.01/.05	.008/.05	.008/.05	.008/.05	.008/.05
AC427X	4	.01/.05	.008/.05	.008/.05	.008/.05	.008/.05
AC43XX	4	.02/.05	.02/.05	.01/.05	.01/.05	.01/.05
AC4720 (SE)	32	.01/.03	.005/.02	.003/.01	.003/.01	.003/.01
AC4720 (DI)	16	.01/.03	.005/.02	.003/.01	.003/.01	.003/.01
AC473X	16	.01/.03	.005/.02	.005/.01	.005/.01	.005/.01
AC474X*	16	.01/.03	.005/.02	.005/.01	.005/.01	.005/.01
AC475X	16	.01/.03	.005/.02	.005/.01	.005/.01	.005/.01
AC476X*	16	.01/.03	.005/.02	.005/.01	.005/.01	.005/.01

* Requires AC260 or AC261 Signal Processor.

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Table 1-4 D/A Converters Matrix

Product	Resolution	Speed	Output	Accuracy	Channel/Module
AC1330	12 bits	50μs	Current	.02	2
AC1530	12 bits	10μs	Voltage	.02	2
AC1562*	12 bits	10μs	Voltage	.02	4
AC1700	16 bits		(Effective resolution when used with AC43XX)		4
AC1813	13 bits	15μs	Voltage	.01	2
AC1814	14 bits	15μs	Volatge	.005	2
AC1914**	14 bits	15μs	Voltage	.005	1
AC1915**	15 bits	20μs	Voltage	.003	1
AC1916**	16 bits	25μs	Voltage	.002	1

* Digital Readback is not provided.
** Temperature compensated version is available.

1.2.5 Digital Input/Output Selection

Tables 1-5 and 1-6 provide the basic characteristics of the various digital input and output devices offered in the ANDS5400 product line. Any type of digital input devices (with or without interrupt capability) and output devices may be installed in any combination in any chassis of the system. The specifications provided in these tables are those most commonly required. For further information refer to the ANDS5400 brochure or the individual data sheets for that product in the ANDS5400 data sheet book. Having selected the type of unit(s) to be used, record the appropriate quantities of each device, one per slot (J1-J16), in the configuration guide.

1.2.6 Expansion Chassis Requirements

Expansion chassis include power supplies, connectors, and all the necessary hardware and interconnection cables for the master and expansion chassis. To determine the number of expansion chassis required, total the number of input and output modules used, and divide by 16. If the answer is a whole number, subtract one; the result is the number of expansion chassis required. If the answer is a whole number and a fraction, round the fraction to the next higher whole number, and subtract one; the result is the number of expansion chassis required.

Example 1:
32 input/output devices divided by 16 equals 2;
2 - 1 = 1 expansion chassis required.

Example 2:
52 input/output devices divided by 16 equals 3.25, rounded off to 4;
4 - 1 = 3 expansion chassis required.

The maximum number of expansion chassis in any single system is seven, yielding a maximum of eight chassis in an entire system. Having determined the number of expansion chassis required, record the appropriate quanitity in the configuration guide.

Table 1-5 Digital Input Matrix

Model	Input Words	Input Type	Propagation Delay	Input Vcc	Interrupt
DC6000	2 x 16	TTL	160 ns max.	TTL	No
DC6100	2 x 16	Optical	50 μs max.	24V*	No
DC62X0	2 x 16	Optical TTL	50 μs max.	TTL or 24V*	Yes
DC630X	1	Optical TTL, Relay, Analog	Counter to 65, 536	TTL or 24V*	Yes

* The user may make modifications for a higher Vcc.

Table 1-6 Digital Output Matrix

Model	Output Words	Output Type	Propagation Delay	Output Vcc	Interrupt
DC6500	2 x 16	TTL	130 ns max.	TTL	Yes
DC6600	1 x 16	Optical	30 μs max.	≤15V	Yes
DC6700	1 x 8	Contact	50Hz	≤220VAC	Yes
DC6300	Prog. Time Base	TTL	Time Base TTL	TTL or ≤15V	Yes

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1.2.7 Power Consumption Characteristics

All chassis in the system have a ±15V and +5V power supply. However, under certain circumstances, the power dissipation by the user cards in an enclosure may necessitate an additional auxiliary power supply. This auxiliary power supply may be installed at the factory or with simple modification by field personnel.

Having determined what devices will be used in the system, the user must determine the power consumption by configuring the system, designating the appropriate cards on the configuration guide, indicating the power consumption (see Table 1-7) in the power slots, and totaling the power consumed by the individual I/O cards.

If the power consumed is greater than that available in the chassis, an AN3500 auxiliary power supply must be added. The AN3500 is available in four models that cover the four standard AC input voltages:

Model	Input
AN3500-A	100V AC 47-400Hz
AN3500-B	120V AC 47-400Hz
AN3500-C	200V AC 47-400Hz
AN3500-D	240V AC 47-400Hz

The maximum power available for user cards from a master chassis is 1.8A @ +5V and 0.6A @ ±15V. The maximum power available from an expansion chassis is 4A @ +5V and 0.9A @ ±15V. The addition of an AN3500 auxiliary power supply adds 5A @ +5V and 1A @ ±15V to the maximum available power. Refer to the "Internal Backplane" section of the "Drawings and Specifications" chapter for a more detailed discussion of the maximum available power. In most cases, if the cards are distributed carefully among the master and expansion chassis, the auxiliary power supply is not required. However, if the auxiliary power supply is required, designate it in the appropriate slot on the configuration guide.

1.2.8 Typical Configuration

Requirements:

Interface to PDP-11 computer with DMA access capability
12 bit resolution
80 kHz conversion rate
64 channels of differential high level analog input
12 thermocouple channels, type K
12 bridge inputs with internal bridge excitation
256 digital inputs
256 digital outputs
120V 60Hz power source

Table 1-7 User Card Power Consumption

Card Type	+5V	+15V	−15V	Comments
AC405X	<10mA	30mA	30mA	
AC407X	300mA	30mA	30mA	
AC425X	<20mA	30mA	30mA	
AC427X	300mA	30mA	30mA	
AC43XX	300mA	25mA	25mA	(External Excitation)
AC43XX	300mA	355mA	355mA	(Worst Case. Maximum Bridge Current Internal Excitation)
AC47XX	20mA	30mA	30mA	
AC280	50mA	60mA	60mA	
AC281	50mA	150mA	100mA	
AC133X	40mA	125mA	150mA	
AC153X	40mA	40mA	80mA	
AC1562	60mA	65mA	140mA	
AC17XX	700mA	200mA		(200mA May Be From + Or - 15V)
AC18XX	120mA	120mA	120mA	
AC19XX	220mA	190mA	60mA	(+15V Is 50mA On Non-TC Versions)
DC6000	200mA			(No ISO's, No Connections)
DC61X0	200mA			
DC62XX	340mA			(With ISO's, No Connections)
DC63XX	350mA			
DC6510	350mA			
DC66XX	150mA			(With ISO's, No Connections)
DC6700	400mA			
DC6701	50mA			(External Coil Power)
DC6702	50mA			(External Coil Power)
DC6710	600mA			
DC6711	50mA			(External Coil Power)
DC6712	50mA			(External Coil Power)
AC30X0	20mA	40mA	150mA	(150mA Tapers Off To 75mA After Warm-up)

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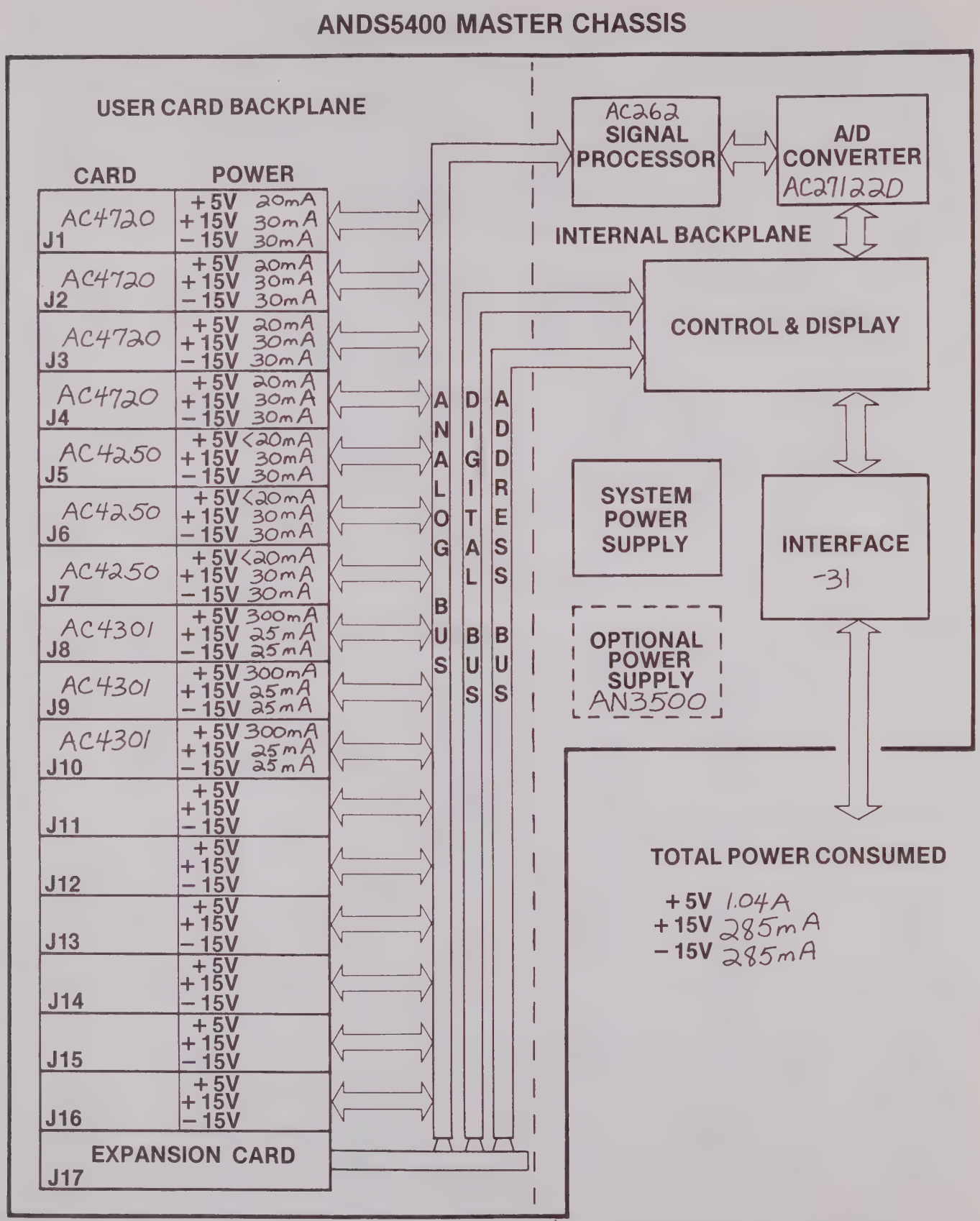
ANDS5400 MASTER CHASSIS
USER CARD BACKPLANE
CARD
POWER
AC4720 J1 +5V 20mA +15V 30mA −15V 30mA
AC4720 J2 +5V 20mA +15V 30mA −15V 30mA
AC4720 J3 +5V 20mA +15V 30mA −15V 30mA
AC4720 J4 +5V 20mA +15V 30mA −15V 30mA
AC4250 J5 +5V <20mA +15V 30mA −15V 30mA
AC4250 J6 +5V <20mA +15V 30mA −15V 30mA
AC4250 J7 +5V <20mA +15V 30mA −15V 30mA
AC4301 J8 +5V 300mA +15V 25mA −15V 25mA
AC4301 J9 +5V 300mA +15V 25mA −15V 25mA
AC4301 J10 +5V 300mA +15V 25mA −15V 25mA
J11 +5V +15V −15V
J12 +5V +15V −15V
J13 +5V +15V −15V
J14 +5V +15V −15V
J15 +5V +15V −15V
J16 +5V +15V −15V
EXPANSION CARD J17
ANALOG BUS
DIGITAL BUS
ADDRESS BUS
AC262 SIGNAL PROCESSOR
A/D CONVERTER AC27122D
INTERNAL BACKPLANE
CONTROL & DISPLAY
SYSTEM POWER SUPPLY
INTERFACE -31
OPTIONAL POWER SUPPLY AN3500
TOTAL POWER CONSUMED
+5V 1.04A
+15V 285mA
−15V 285mA

Figure 1-2 Typical Configuration Guide Filled Out

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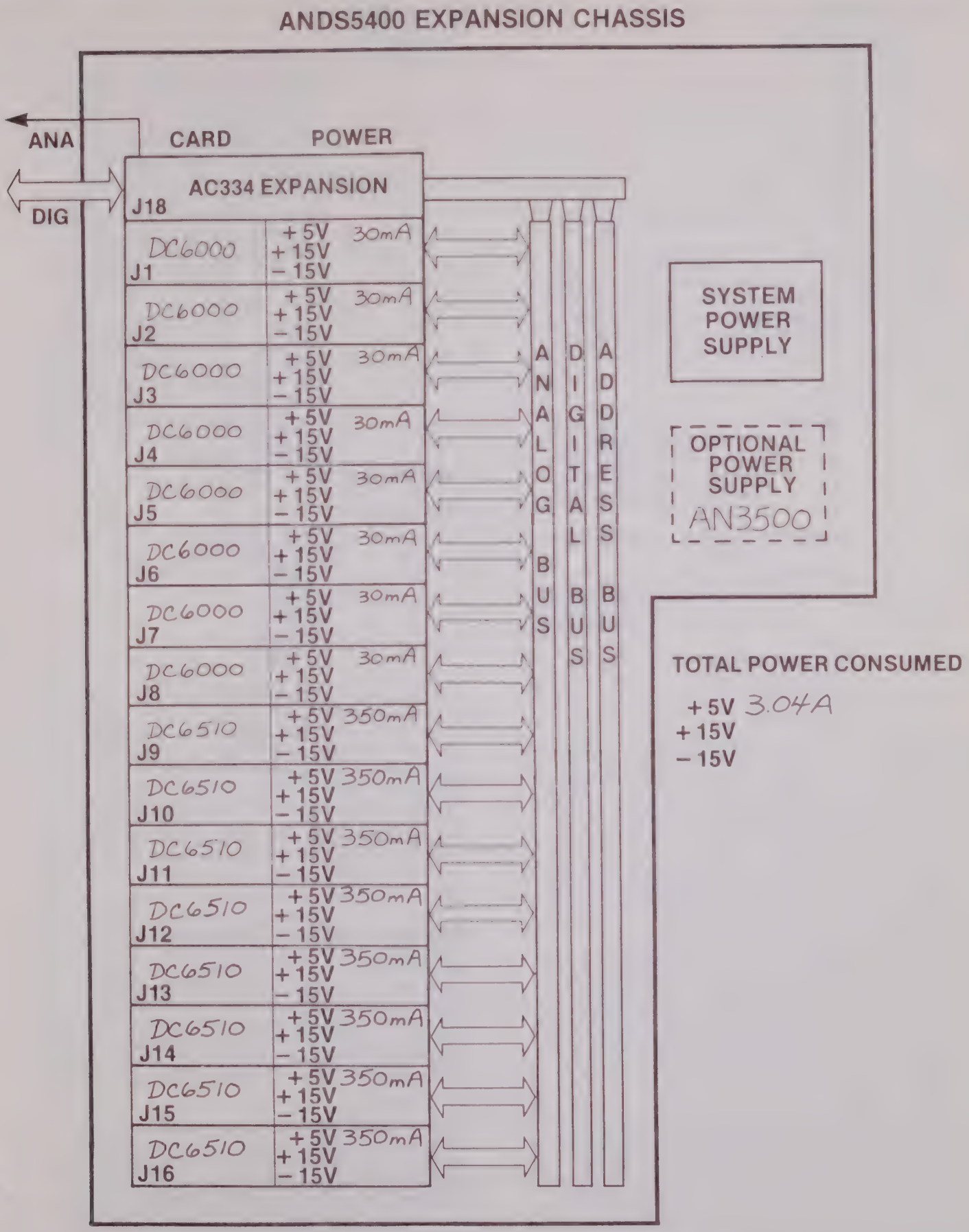

Figure 1-2 Typical Configuration Guide Filled Out

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System Configuration:

ANDS5400-B-B-31
AC262-AC27122D
4 AC4720
3 AC4250
3 AC4301
8 DC6000
8 DC6510
1 ANDS5450-B
2 AN3500-B*

*Note that the above configuration does not require 2 AN3500's, but it is recommended that they be included to provide flexibility.

1.3 Typical Applications and Configurations

This section presents two typical applications of the ANDS5400 data acquisition system, revealing several of its practical capabilities. Each example includes the requirements of a typical application and the necessary configuration to meet those requirements.

1.3.1 Example 1:

Requirements:

Application: A high speed monitor to record the propagation of a shockwave through a mine shaft and provide analog output through a high-speed plotter.

Resolution: 11 bits plus sign on input and output.

Computer Type: LSI-11.

Aggregate Throughput Rate: 80kHz (2kHz per channel, 40 channels).

Configuration:

ANDS5400-B-B-18
AC262-AC27122D
3 AC4720
1 AC15622D

The -18 interface provides DMA/PIO interface to the LSI-11/2 computer. The AC262 and AC2712 yield 11 bit plus sign resolution of the analog input at 95kHz. The three AC4720's offer 48 channels of differential analog input, and the AC15622D provides 4 channels of 12 bit analog output. This application also uses the external synchronization capability of the ANDS5400.

The data acquisition system is initialized by the computer, and subsequently a DMA cycle begins. By holding the external trigger input low, further DMA transactions are suspended prior to the first conversion. The system then waits for a START command generated by a transducer sensing the initial explosion. When the explosion occurs, the trigger signal is sent to the data acquisition system, and the system begins its conversion sequence. Under the DMA control the system then makes continuous measurements on the forty channels of interest at a rate greater than 80 kHz. This scan sequence continues for a period of time determined by the application requirements.

At the completion of the sequence the data contained in memory represents a continuous scan of the forty channels; this data is subsequently manipulated by the customer's computer and in nearly real time may be displayed on the high-speed analog recorder. The stored data will be compared to data taken from other explosions to determine the nature and propagation effects of a shockwave through a mine shaft as the explosive material and the design of the mine shaft are varied.

1.3.2 Example 2:

Requirements:

Application: Closed loop control to monitor and control the flow of material into a production process. Monitor parameters include temperature within the preheater, temperature of material leaving the preheater, number of items leaving the preheater, failure of preheater output transfer, failure of preheater input transfer, amount of material available at the input of the preheater. Control functions include preheater ON/OFF and alarms for preheater input/output transfer failure and for low material available at preheater input.

A full scan must be completed two times per second with immediate alarms for input/output transfer failure. The preheater must be maintained at an accuracy of $\pm 10^{\circ}C$. The amount of material available at the input and the number of items at the output will be displayed constantly.

Computer Type: CPU HP21MX

Configuration:

ANDS5400-B-B-24A
AC260-AC27142D
1 AC4250
1 AC4301
1 DC6301
1 DC6210
2 DC6700
1 AC3000

When energized, the ANDS5400 turns on the preheater, its associated motors, etc. via the DC6700, checks the weight of material at the input to ensure it meets minimum start-up requirements via the AC4301, self-tests itself via the AC3000, and monitors the preheater temperature via the AC4250. Once the preheater reaches the correct temperature, the DC6700 initiates product transfer from the input to the preheater. The AC4250 monitors the temperature of the preheater and turns the heat system on and off as appropriate to maintain a $\pm 10^{\circ}C$ temperature accuracy. The DC6301 counts the items flowing from the preheater.

When the AC4301 senses that the weight of material available at the input has fallen below prescribed minimums, an annunciator is actuated by the DC6700, causing the operator to bring added material to the input. If necessary, the operator can suspend input transfer by interacting with the control panel. If either the input or output transfer fails to operate, the DC6210 generates an interrupt; then via the DC6700 this interrupt initiates alarms and, as prescribed, may totally or partially shut down the process to prevent damage.

1.4 Conclusion

The remaining chapters in this manual explain in detail the installation and overall operation of the ANDS5400 and provide mechanical drawings and schematics of each component in the system. Before proceeding further the user should inspect the system and read the "Installation" and "Quality Conformance" chapters to verify that all components shipped have been received in satisfactory condition.

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2
INSTALLATION

2.0 General

This chapter describes the system's environmental conditions, unpacking instructions, inspection, pre-installation tests, installation procedures, and system-computer integration. Before opening any boxes read the environmental conditions and unpacking instructions carefully.

With each chassis Analogic supplies an accessory kit, the specified user card configuration assembled in the chassis, an AC line cord, and two 22-inch rail assemblies that mount into standard EIA 19-inch wide equipment racks. The necessary cables to interface the ANDS5400 with the customer's computer are supplied by Analogic or by the customer depending on the particular interface selected.

If it is necessary after the initial installation to add the optional auxiliary power supply, refer to the last section of this chapter.

If any of the tests in this chapter fail or if any components are missing or damaged, call Analogic's Customer Service Department immediately; the telephone number is listed in the address block at the end of the Table of Contents.

2.1 Environmental Conditions

The following environmental conditions must be met before proceeding with the installation. The unit and its accessories can tolerate a storage temperature range from -25° to +85°C and an operating temperature range from 0° to +60°C. The storage and operating humidity must be between 0% and 80% (non-condensing). The unit cannot withstand salt or other corrosive materials during storage or operation.

Each chassis dissipates approximately 90 watts with a single power supply or 180 watts with an auxiliary supply. For most installations forced air cooling is not necessary to maintain the correct operating temperature; however, if forced air cooling is used, the air must be properly filtered.

The customer's power source must correspond to that denoted by the model number of the ANDS5400. To verify the model number, remove the configuration guide from the "Quality Conformance" chapter at the end of Book One. The voltage for the system is designated by the letter in the "X" position of the system model number, ANDS5400-X-Y-ZZ, where "X" = A, B, C, or D, corresponding to 100V, 120V, 200V, or 240V. The frequency of the power source can be between 47 and 400 Hz.

2.2 Unpacking Instructions

Before opening any boxes inspect them carefully and report any damage to the carrier immediately. Open the boxes without ripping them; all boxes and packing material must be saved for storage or shipping. From each outer box remove the packing material, the inner box, slides, and accessory kit; from each inner box remove the chassis and AC line cord.

2.3 Inspection

The serial number and model number of each component of the ANDS5400 should be checked to ensure that all components ordered have been received. Remove the production configuration sheet from the "Quality Conformance" chapter. Be sure the Quality Assurance (QA) verification appears on the configuration sheet and on the configuration guide. To compare the configuration guide with the components shipped, remove the master chassis cover by turning the six quarter-turn fasteners (see Figure 2-1).

In the master chassis locate the signal processor, A/D converter (if applicable), power supply, auxiliary supply (if needed), and the user cards. One at a time, pull out each card and verify that its serial number corresponds to that on the configuration sheet and its model number corresponds to that on the configuration guide. To maintain the correct configuration replace each card before removing the next one. Replace the cover, and tighten the quarter-turn fasteners.

Remove the cover of each expansion chassis (see Figure 2-2), and repeat the verification process, removing only one card at a time to maintain the correct configuration of cards.

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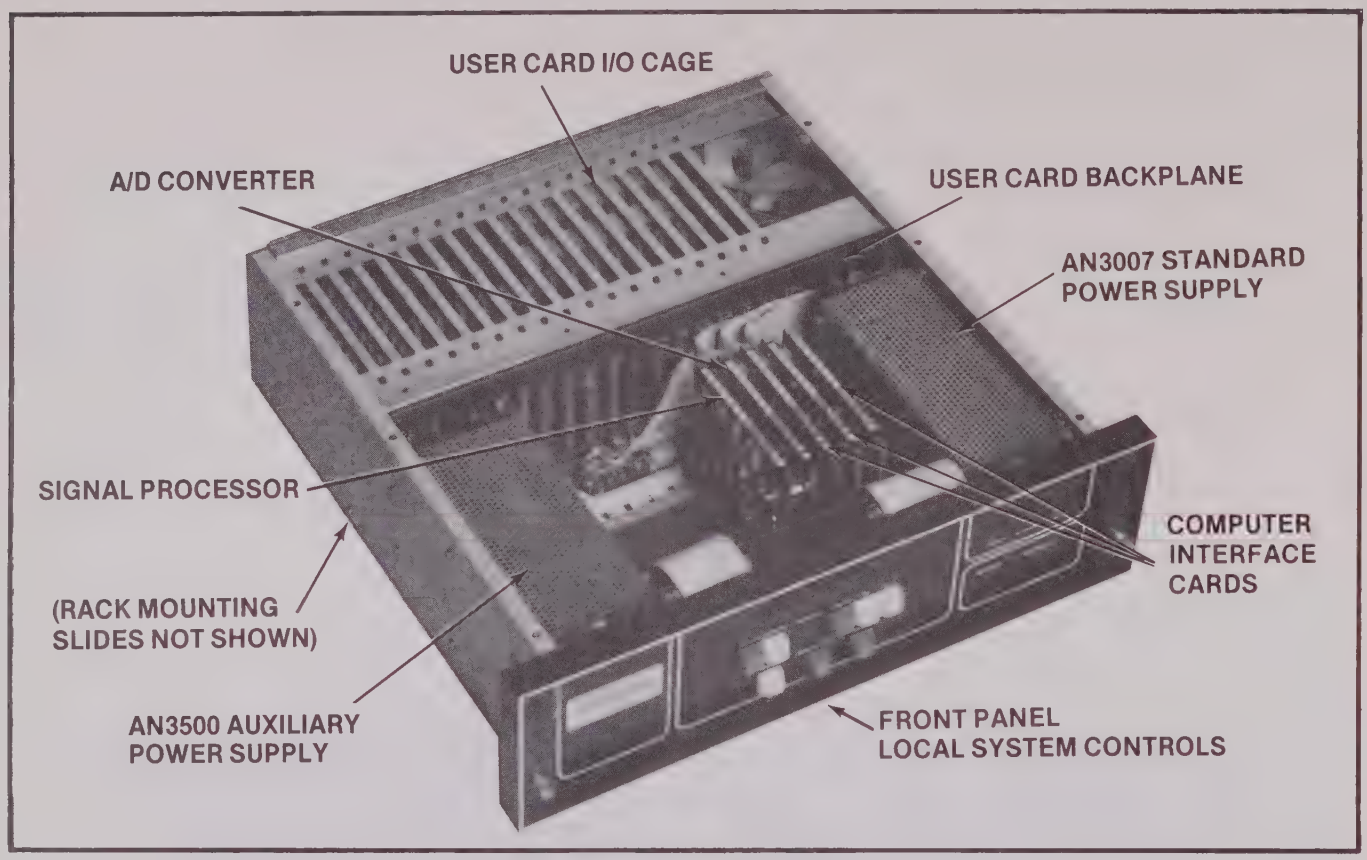

Figure 2-1. Master Chassis

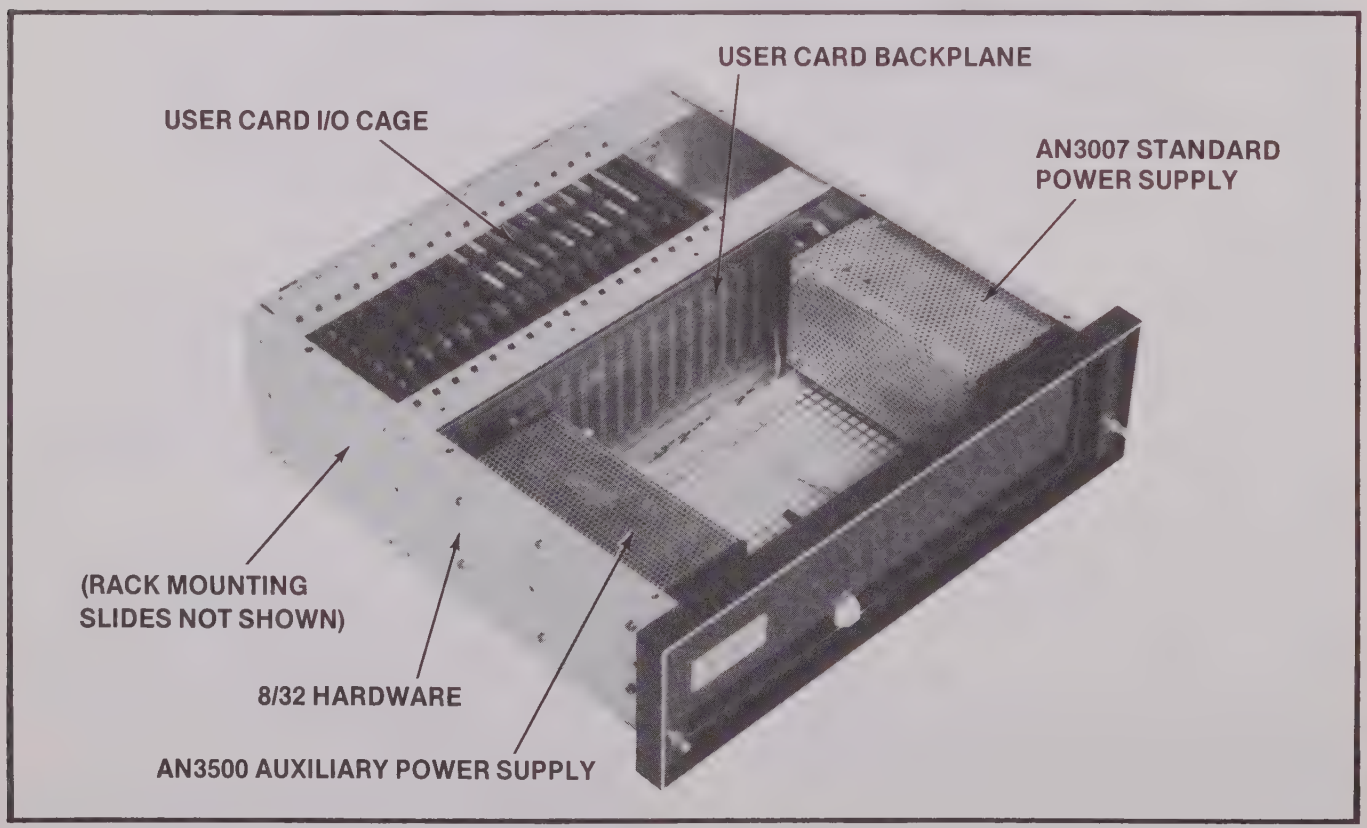

Figure 2-2. Expansion Chassis

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2.4 Pre-Installation Tests

Test the master chassis first. Be sure that the POWER button on the front panel is not depressed, that the AC power source corresponds to that indicated on the configuration guide, and that CHASSIS GROUND, POWER GROUND, and SIGNAL RETURN are strapped together at the rear of the chassis. Plug the AC line cord into the rear of the chassis then into the power source. Depress the POWER button; the REMOTE lite should glow, and the display LED's should come "alive." Check the chassis for excessive heat dissipation; the maximum "hot spot" temperature should not exceed 60°C. Verify the ± 15V and + 5V power supplies at J7 and J16 on the user card backplane (see the "Internal Backplane" section of the "Drawings and Specifications" chapter for the locations of J7 and J16).

Depress the REMOTE/LOCAL button on the front panel. Perform the tests in the "Digital Input — Reading Back the Range and Address Registers" and "Digital Input — Reading the Switch Registers" sections of the "Architectural Overview" chapter.

> Note: The "Front Panel" section of the "Drawings and Specifications" chapter explains in detail the operation of the front panel controls and the addressing system.

Unplug the chassis; it is now ready for installation. If no expansion chassis were purchased, proceed directly to the "Installation" section of this chapter.

One at a time, test each expansion chassis. Be sure the POWER button is not depressed. Plug the AC line cord into the rear of the chassis, and plug the cord into the power source outlet. Depress the POWER button; the POWER lite should glow. Check the chassis for excessive heat dissipation. Verify the ± 15V and + 5V power supplies on J7 and J16 on the user card backplane. Unplug the chassis; it is now ready for installation.

2.5 Installation Procedures

The slide rail assemblies permit the master and expansion chassis to be pulled forward out of the equipment rack for calibration, adjustment, and maintenance accessibility. To allow the chassis to slide to its fully extended position, the computer interface cable must be long enough and the racks must be located near enough to the power source outlet to allow a minimum of 24 inches of slack in the AC line cord and in all the cables to the rear of the system.

> **CAUTION:** When several chassis are fully extended, the equipment rack may become unstable.

To install the slide rails on the chassis separate them from the tracks, and remove the front and rear brackets, the latch plates, and necessary hardware from the accessory kit. Using four 8/32 screws from the accessory kit, mount the slide rails to the sides of the chassis (see Figure 2-3).

For each chassis install the slide rail tracks, front and rear brackets, and the latch plates in the equipment rack as shown in Figure 2-3. Mount the tracks to the equipment rack so that there is a 3.5 inch space above the top chassis and below the bottom chassis and, ideally, a 1.25 inch space between chassis for convection cooling.

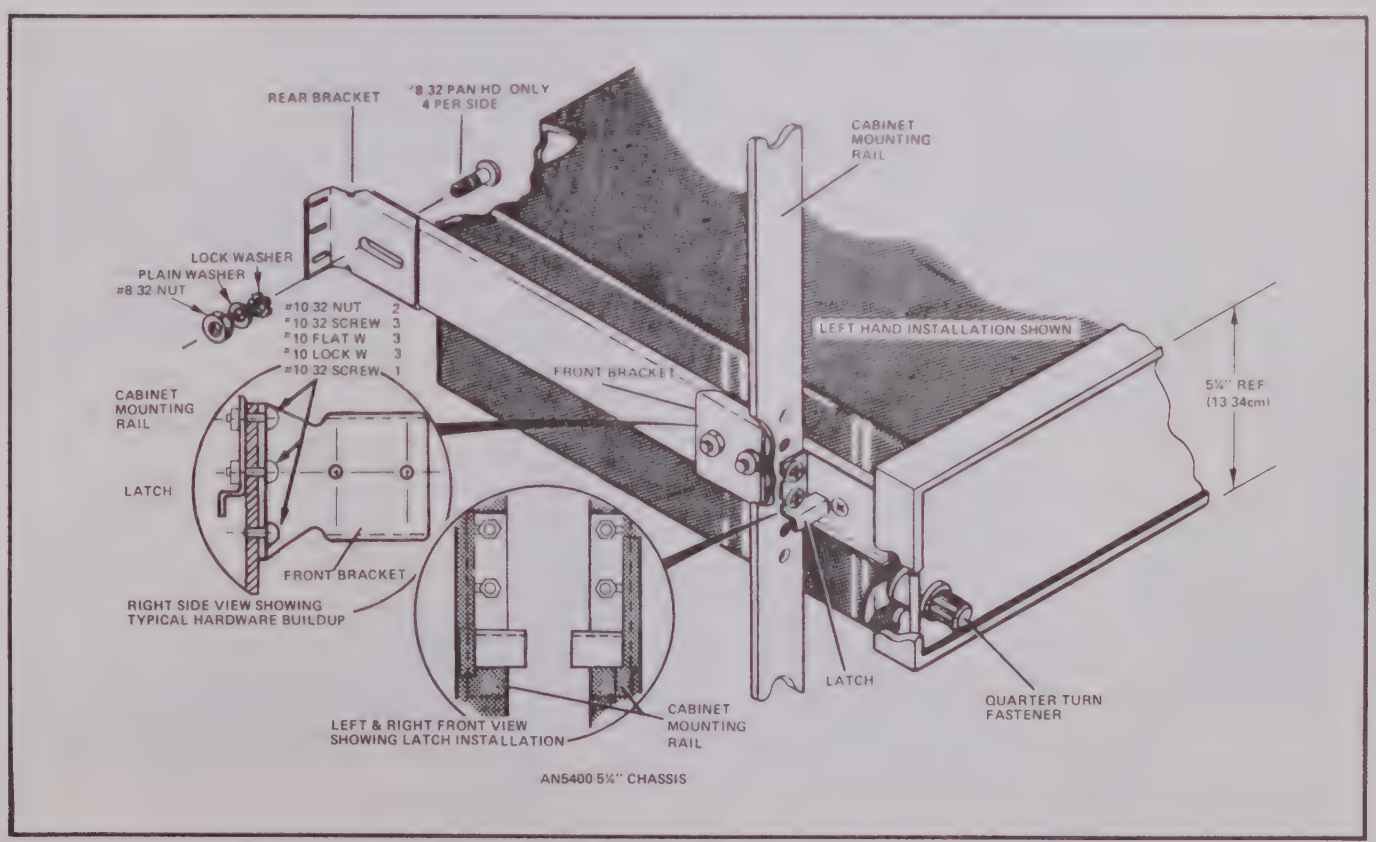

Figure 2-3. Chassis Slide-Rail Mounting

The tracks and brackets should be tight enough to hold the chassis safely but loose enough to allow adjustments for proper fit. Arrange the two rear brackets so that at least a four inch space remains at the rear of each chassis for attaching connectors and cables. Install the master and expansion chassis into the rack, making any necessary changes in the position of the slides for proper alignment, travel, and spacing. When proper fit is obtained, remove each chassis and tighten all hardware securely. Re-install each chassis into the rack. Rotate all front panel quarter-turn fasteners to engage the fixed latch plates, locking each chassis in place.

2.6 System-Computer Integration

Attach the computer interface cables to the rear panel of the master chassis; note that the cables may be supplied by Analogic or by the user, depending on the computer interface selected. Attach the customer-supplied timing and synchronization cable (if required) to J28 at the rear connector panel of the master chassis.

Note: Any signals that may be connected to J28 on the rear panel of the ANDS5400 for external synchronization of A/D conversions or simultaneous sample-and-hold (SSH) transactions are still in effect while the system is in "local" control. Therefore, it is recommended that this connector be removed during the "local" mode of operation unless it is known that the HOLD line and the TRIGGER line are always high.

Refer to Figures 2-4, 2-5. Attach the Input/Output signal cables to J1 through J16 at the rear of the master chassis. Connect the expansion cables to the rear of each expansion chassis; the 6-pin cable is the analog cable, the 50-pin ribbon cable the digital cable.

Attach one end of the digital cable to J8 on the AC333-2 card in slot J18 of the master chassis. Attach the other end of this cable to J2 on the AC334-1 card in slot J17 of the first expansion chassis. For the second expansion chassis connect its digital cable from J1 on the AC334-2 card from the first expansion chassis to J2 on the AC334-1 card in the second expansion chassis.

Continue this procedure until the last expansion chassis is connected. Note that J1 on the AC334-2 card in slot J18 in the last chassis will be empty.

Connect the analog cable from the first expansion chassis from J1 on the AC334-1 card in slot J17 of the expansion chassis to J1 on the AC333-1 card in slot J17 of the master chassis. Connect the analog cable from J1 on the AC334-1 card in J17 in the second expansion chassis to J2 of the AC333-1 card in the master chassis.

Continue this procedure for all expansion chassis, using the small connectors J1 through J7 on the master chassis for the analog cables from expansion chassis 1 through 7, respectively.

Note: J1-J6 is on slot 17 of the master chassis, and J7 is on slot J18 of the master chassis.

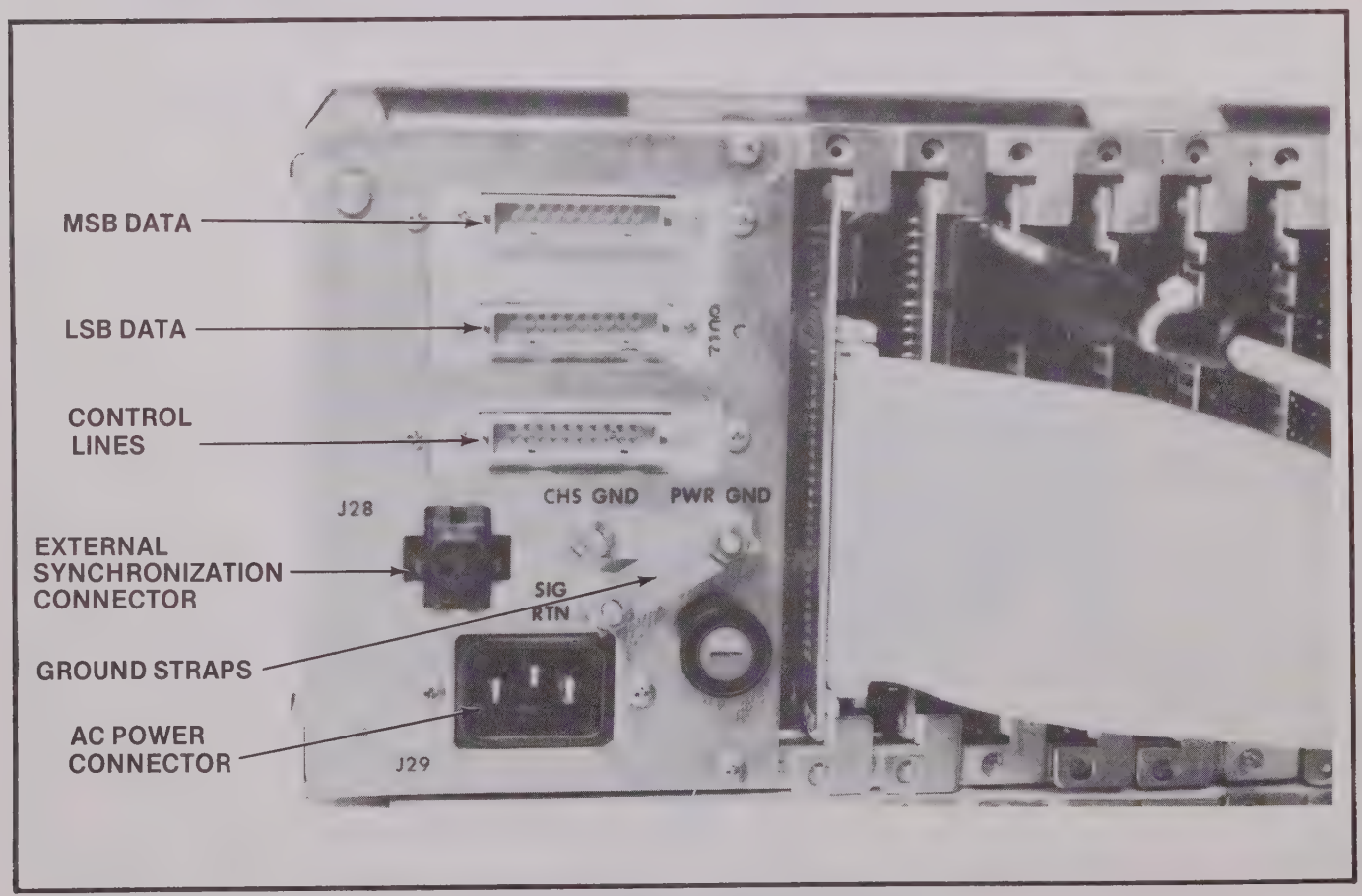

Figure 2-4. Connections to Rear of Master Chassis

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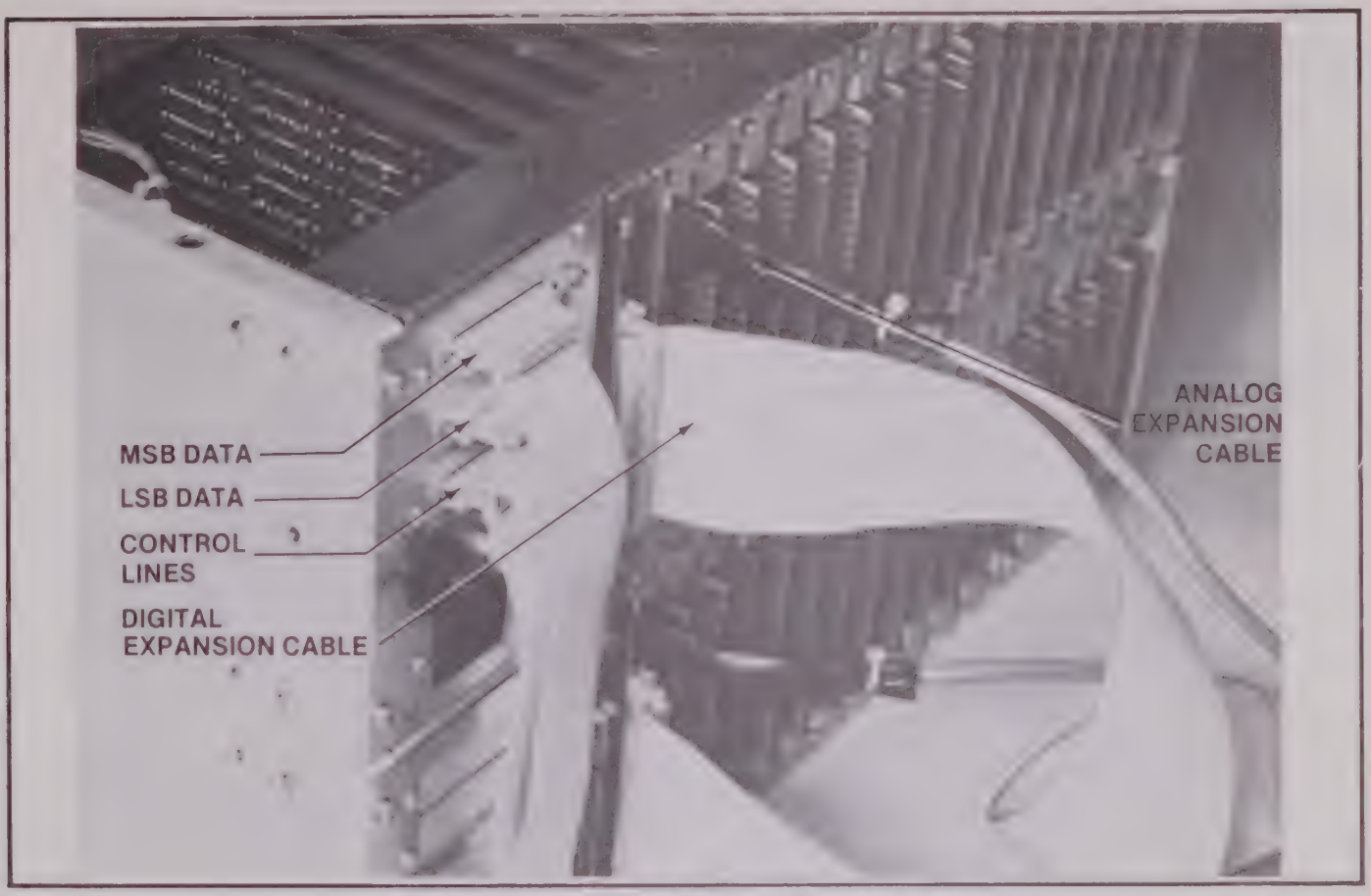

Figure 2-4. Connections to Rear of Master Chassis

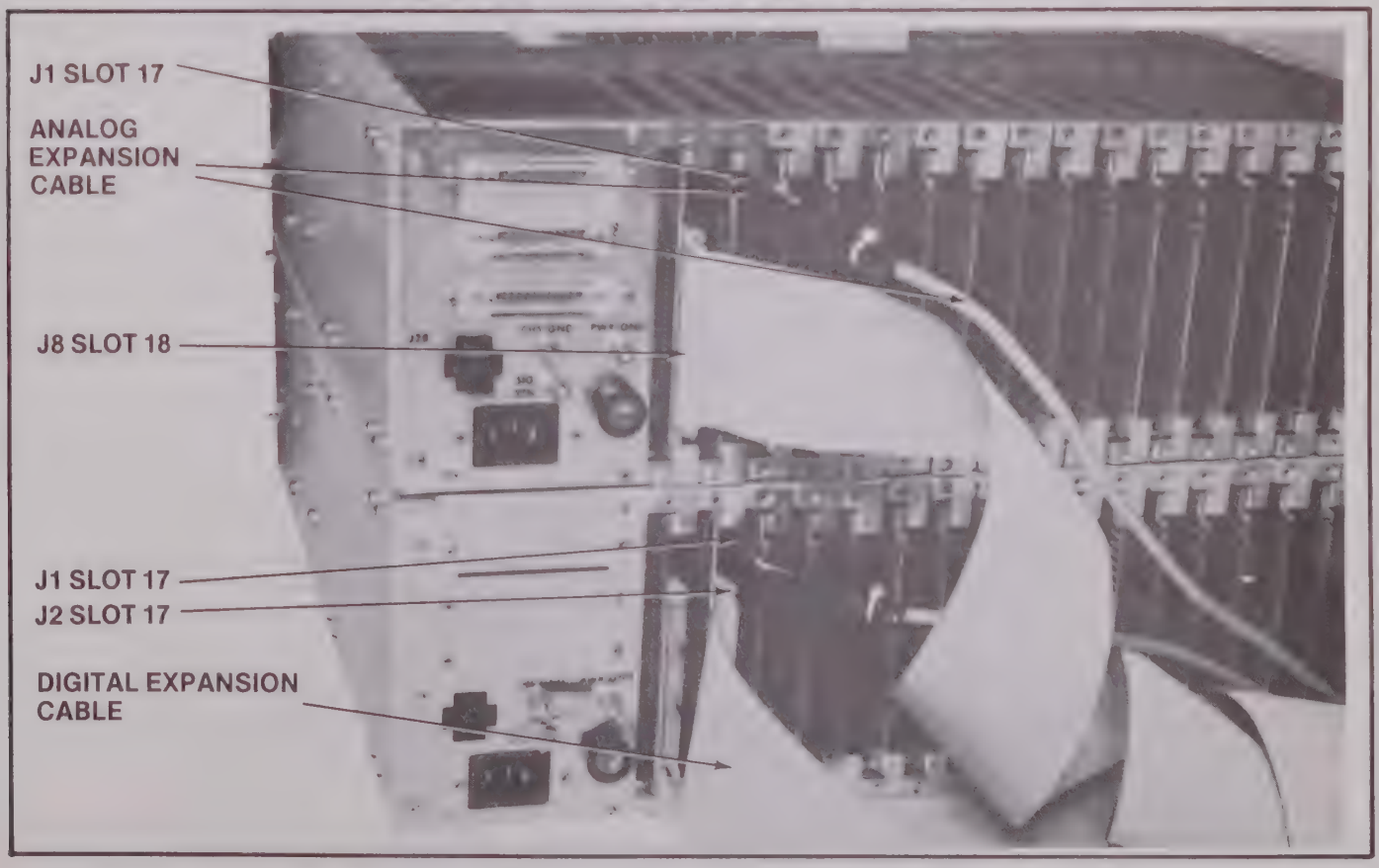

Figure 2-5. Expansion Chassis Interconnections

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To assure accurate results, disconnect the timing and synchronization cable (if used) from J28 before performing the following tests. Make sure all the POWER buttons are not depressed. Plug each AC line cord into the power source, and energize each unit. All the POWER lites should glow.

Repeat the tests in the "Digital Input — Reading Back the Range and Address Registers" and "Digital Input — Reading the Switch Registers" sections of the "Architectural Overview" chapter. After completing these tests, shut off the power, and reconnect J28.

Push all the units into the equipment rack. Secure the covers on all the chassis, and check the temperature inside each chassis. If the temperature exceeds 60°C, forced air cooling and proper air filtering must be provided.

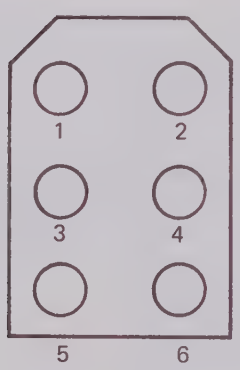
Note: A thorough reading of the "Performance Enhancements" and "Maintenance and Calibration" chapters is recommended to optimize the performance of the ANDS5400 system.

2.7 Remote Synchronization

The Remote Synchronization circuits are controlled by inputs into J28 of the master chassis. These circuits provide for synchronizing the analog-to-digital converter (ADC) and the simultaneous sample-and-hold (SSH) circuits to externally supplied signals.

Figure 2-6 shows the pinout of J28 as viewed from the rear of the master chassis. Pins 3 and 5 are used for control of SSH user cards such as the AC280. "Ready to Hold" is a CMOS output from the ANDS5400 indicating that the interface has sent the command to change the state of the sample-and-holds. "Hold" is the user input to the ANDS5400 to execute the command. For a complete description of this mode of operation, refer to "Digital Strobe Pulses and SSH Control" section of the "Front Panel" section of the "Drawings and Specifications" chapter.

Pins 2 and 4 on J28 are used for control of the ADC. READY TO MEASURE is a CMOS ouput level from the ANDS5400 indicating that the interface has issued a command to the ADC to measure. TRIGGER has an internal pull-up resistor, so it may be left floating, in which case the converter will be triggered immediately on command from the interface. The TRIGGER signal, when low, may hold off conversions indefinitely. The READY TO MEASURE signal may be cleared low by an interface clear signal. Refer to Figure 2-7 for the timing relationships of these signals.



View from rear of ANDS5400

1. Dig GND
2. Ready to Measure
3. Ready to Hold
4. Trigger
5. Hold
6. Dig GND

Figure 2-6. J28 Pinout and Signals

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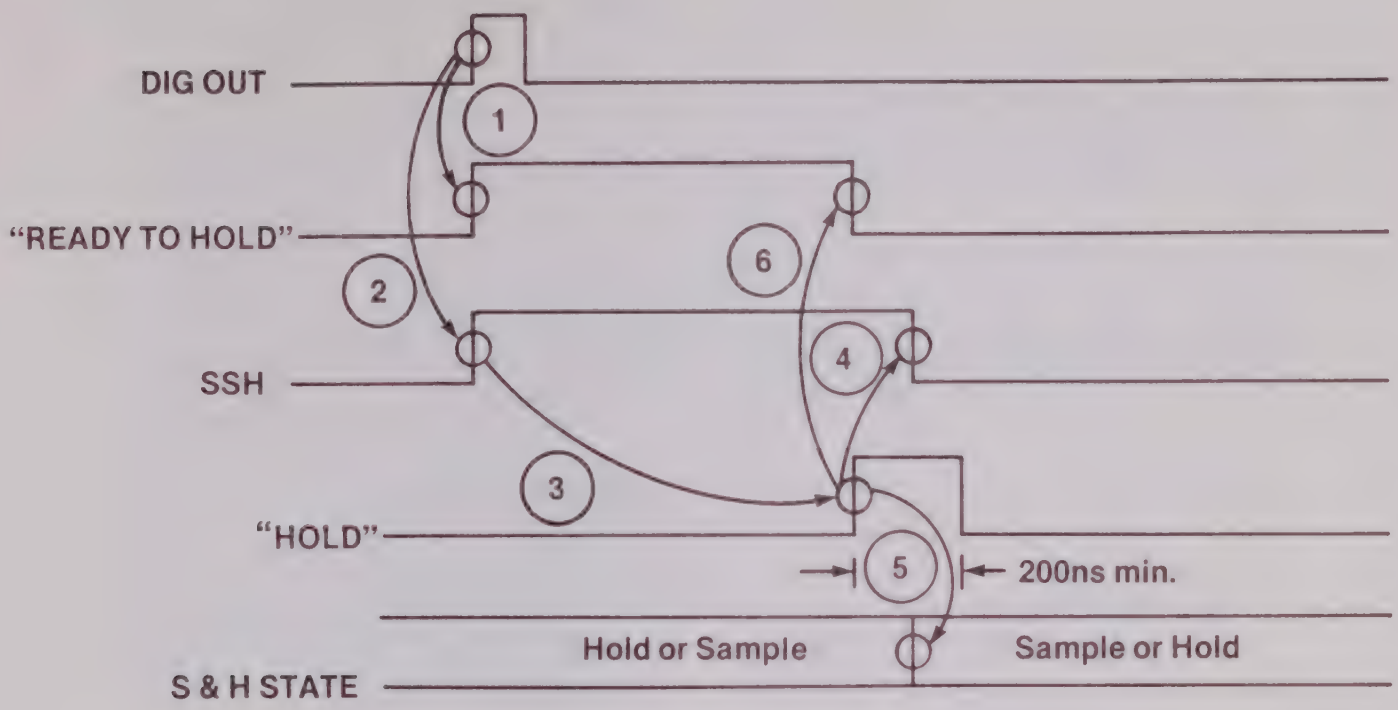

*Signals on J28 User Trigger Connectors

Maximum Time Delays

1	200ns
2	200ns
3	User-Controlled Delay
4	1.2μs
5	1.5μs
6	250ns

"READY TO HOLD" - High Current CMOS Output 2 TTL Fanout.
"HOLD" - 74 LS Input with 4.7 kΩ pullup.

Figure 2-7. User-Controlled Sample-and-Hold Timing

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3
ARCHITECTURAL OVERVIEW

3.0 General

The ANDS5400 system, a high-speed computer-controllable multi-purpose data acquisition and control system, has a flexible structure that can meet many different application requirements. The structure supports the five primary types of input and output:

1) Analog Input
2) Analog Output
3) Digital Input
4) Digital Output
5) Asynchronous Event Recognition (Interrupt Structure)

Each ANDS5400 system is tailored to a particular application by the choice of these system options:

1) Computer Interface
2) Signal Processor
3) A/D Converter
4) User Cards
5) Self-Test Capability
6) Expansion Chassis
7) Optional Power Supplies
8) Optional Cable Assemblies
9) Software Support Packages

All ANDS5400 installations have a master chassis, which includes the computer interface, signal processor, A/D converter, display panel, system control logic, and the bus structure for 16 user cards. For applications requiring more than 16 user cards, as many as seven expansion chassis connect to the master chassis; each expansion chassis can support 16 user cards, thus bringing the total capacity of a fully expanded system to 128 user cards.

3.1 Master Chassis

The master chassis, the basic building block for all ANDS5400 installations, is a 5.25 inch high, 19 inch wide, rack-mountable unit containing the system power supply, internal backplane, display/control panel, user card backplane, and expansion cards.

3.2 System Power Supply

The standard system power supply, the Analogic AN3007, supplies +15 volts at 1 Amp, -15 volts at 1 Amp, and +5 volts at 5 Amps. (See the enclosed data sheet in the "Power Supply" section of the "Drawings and Specifications" chapter). The ±15 volt sections use linear regulators, and the +5 volt section uses an efficient switching design. The unit has a transformer input with internal jumpers that are adaptable to all common line voltages. The power supply input voltage is designated by the letter in the "X" position of the ANDS5400 system model number, as shown below:

ANDS5400-X-Y-ZZ

A = 100 Volts 47 to 400 Hz
B = 120 Volts 47 to 400 Hz
C = 200 Volts 47 to 400 Hz
D = 240 Volts 47 to 400 Hz

3.3 Optional Power Supply

The AN3500 optional power supply, equivalent to the standard AN3007 power supply, may be added to the master chassis if additional current is required beyond the capacity of the standard supply. This requirement may exist if many high current user cards are installed (e.g. relay cards, bridge completion (strain gauge) cards, digital drivers, custom built cards, etc.) The AN3500 kit includes an AN3007 power supply with mounting hardware and cabling that connects to existing terminals in the system. This optional supply will be factory-installed if ordered with the original system, or it may be user-installed if high current user cards are added to the system after the original installation. Installation instructions for the AN3500 kit are in the "Installation" chapter.

The AN3500 has a current capacity equal to that of the standard power supply. When installed in the master chassis, the AN3500 provides ±15 volt power for user cards installed in slots J1 through J8 and +5 volt power for user cards in J1 through J12. The +5 volt power for the user card backplane is unequally divided between the two supplies because the standard supply carries the burden of the front panel and the computer interface. When the AN3500 is installed in an expansion chassis, it supplies ±15V and +5V power for slots J1 through J8.

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3.10 REMOTE / LOCAL Button

The REMOTE/LOCAL button transfers system control from the computer ("remote" mode) to the front panel buttons ("local" mode). In "local" control the ANDS5400 ignores all computer commands; in "remote" control all front panel buttons except POWER are ignored. The switch register settings will have no direct effect on the system while it is in the "remote" mode, although they can be interrogated by the software and, thus, may have an indirect effect on the system. Computer commands to the system can set a status indicator that will lock the system in "remote" control, preventing inadvertent "local" operation. However, once the ANDS5400 is in "local" control, no computer commands can force the system into the "remote" mode.

NOTE: J28 Interaction:
Any signals that may be connected to J28 on the rear panel of the ANDS5400 for external synchronization of A/D conversions or simultaneous sample-and-hold (SSH) transactions are still in effect while the system is in "local" control. Therefore, it is recommended that this connector be removed during the "local" mode of operation, unless it is known that the HOLD line and the TRIGGER line are always high.

3.11 CLEAR Button

When the system is in "local" control, the CLEAR button creates the clear pulse that initializes the system. See the "Front Panel" section of the "Drawings and Specifications" chapter for details of the functions performed by this pulse.

3.12 ANALOG Button

When the system is in "local" control, the ANALOG button loads the range and address registers with the information set into the switch register, and A/D conversions are made at a slow rate with the results appearing on the DATA display. To change the address or range, alter the switch settings, and push the ANALOG button again. The ANALOG lite is illuminated under the DATA display while A/D conversion results are being displayed.

3.13 DYNAMIC Button

After the ANALOG button has been pressed and the system is measuring the desired channel, the dynamic button may be pressed to simulate high speed selection and acquisition of the channel. The dynamic function inverts the MSB of the address until just before the A/D conversion is triggered.

For example, if an analog address of 0000 is chosen with the ANALOG button, the system will be connected to that channel all the time and will convert and display the results at a slow rate. If the DYNAMIC button is now pressed, the system will be connected to address 4000 (1st channel in the forth expansion chassis) until a conversion is started. The system will switch back to address 0000 for the duration of the conversion and will then return to 4000.

This address alteration simulates the normal computer controlled operation of the system, in which a channel address is chosen just prior to the A/D conversion. Any difference between the normal ANALOG data display and the DYNAMIC data display may be indicative of slew rate or settling time errors, but care must be taken to assure that the input voltage of the alternate channel is of a known value. If there is no channel or expansion chassis at the alternate address, the input may float to a level that exceeds the input capability of the system, thus giving false error indications.

The DYNAMIC function is useful primarily for troubleshooting system analog problems that cannot be seen when the system is in static operation. For this purpose the user may elect to tie the analog expansion connector used during alternate address selection (typically expansion chassis four for all the addresses in the master chassis) to a known voltage source (+ 10V, -10V, ground, etc.) for diagnostic debugging. See the "Expansion Cards" section of the "Drawings and Specifications" chapter for analog connector pinouts.

Note: The address displayed by the address lites will not be altered during DYNAMIC operation.

3.14 REQUEST Lite

The REQUEST lite is illuminated whenever any user card is requesting interrupt service.

3.15 DIGITAL Button

When the DIGITAL button is pressed, the address set into the switch register is loaded into the address register. The upper two digits of the switch register are not used in this transaction. The information stored in the range register will not be disturbed, although the range register display will be blanked as the system goes into the D/A address decoding mode.

3.16 IN Button

Pushing the IN button after pushing the DIGITAL button displays the the digital information from the selected address on the DATA lites. The data is directly connected to the display, so rapidly moving data from a digital input source may cause a blurred display.

3.17 OUT Button

Pushing the OUT button after pushing the DIGITAL button sends the data set in the switch register to the digital device whose address is loaded into the address register. The data are automatically strobed into the digital device twice each second. To alter the data the switch register may be changed after the OUT button has been pushed. Because of this feature, the DIGITAL IN button must be pressed to stop the updating of the output after the appropriate value has been loaded.

3.18 DATA Display

The DATA display consists of six LED octal digits that show 16 bit digital information coming from a digital input device or from the system A/D converter. The data may range from 0 to 177777. The source of the data is indicated by the three lites below the display. When the DIGITAL lite is lit, the data is coming from the digital device whose address is shown on the address lites. When the ANALOG lite is lit, the data is coming from the system A/D converter, which is measuring the channel shown by the ADDRESS display at a gain shown by the RANGE display. When both the ANALOG and DYNAMIC lites are lit, the source of the data is still the system A/D converter, but the system is operating in the local "dynamic" mode of addressing. Leading zeros are blanked in both ANALOG and DIGITAL IN modes, and the entire DATA display is blanked during digital output transactions.

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The DATA display is active during computer control, so all analog conversions and all digital input transactions are shown; however, the data changes so rapidly that the display usually is a blur. The last analog conversion made in a burst of measurements will remain on the display if there is a long pause in the software, but the last digital input reading may not be displayed under similar circumstances since many interfaces return the system to the output mode at the end of each transaction, thereby blanking the display.

3.18.1 Analog Data Interpretation

The digital representation of the analog voltage measured by the system follows rules established partly by the system architecture and partly by the particular converter chosen by the user. The data displayed by the front panel is in a format identical to the data read by the computer.

3.18.1.1 System Rules

1) All analog data is represented as a 16 bit, 6 octal digit number.

2) The active bits of converters having less than 16 bits are "left hand justified," such that the most significant bit is always in the left-most position.

3) The remaining bits for converters having less than 16 bits are always represented as zeros.

3.18.1.2 Converter Rules

1) All unipolar converters (those capable of measuring only positive voltages) use binary coding, such that 000000 represents zero volts and 100000 represents 1/2 scale.

2) All bipolar converters (those with equal positive and negative spans) use 2's complement coding, such that 000000 represents zero volts, 140000 represents -1/2 scale, and 040000 represents + 1/2 scale.

3) BCD, offset binary, and 1's complement coding A/D converters are not used.

4) The number of bits of resolution (12 to 16), the choice of unipolar or bipolar, and the voltage range of the converter are determined by the user.

5) All system converters have a binary weighting scale: i.e. starting at the MSB, each bit has half the value of the previous one.

3.18.1.3 Octal-to-Decimal Conversions

With a "programmer's" calculator that can convert between octal and decimal numbers, there is an easy way to convert the DATA display into an analog value:

1) Enter the six digit octal number from the display into the calculator. Be sure to enter all six digits regardless of the number of bits in the A/D converter, and be sure to have the calculator in the octal mode.

2) Convert the octal number to a decimal number.

3) Divide the result of step 2 by 65536 (decimal).

4) Multiply the result of step 3 by the full scale range (FSR) of the A/D converter. (0-10 V A/D = 10 V FSR, ± 10 V A/D = 20 V FSR, etc.)

5) The displayed result is correct for unipolar converters or for bipolar converters with positive inputs (i.e. the MSB is off). If a bipolar converter has a negative input (the MSB is on, and the octal number entered in step 1 was greater than 100000), subtract the FSR from the result of step 4.

6) If programmable gain was used, divide the result by the gain used (e.g. 1, 2, 4, etc.) to find the system input voltage; and, if there is gain on the input user cards (e.g. isoplexers, thermoplexer, etc.), divide this result by that gain to find the sensor voltage.

This technique is also useful to system programmers for converting from the raw binary A/D results to floating point real numbers since the technique is fast and does not depend on the number of bits in the converter. If this method is used, higher or lower resolution converters may be installed in the system without software alterations.

3.19 RANGE Display

The four bit range code is indicated by the octal range display whenever the system is in the ANALOG mode. The range code varies from 0 to 17. (The leading zero is blanked for single digit ranges.)

3.20 ADDRESS Display

The 12 bit address, appearing as four octal digits in the ADDRESS display, ranges from 0 to 7777. (Leading zeros are blanked.) Refer to "Address Bus Bit Interpretation" in the "Front Panel" section of the chapter entitled "Drawings and Specifications" for a detailed explanation of the addressing system.

Table 3-1 Converter Examples

Voltage	16 Bit, ±10V	16 Bit, 0 to +10V	12 Bit ±5V
+ FULL SCALE	077777 (+9.999695V)	177777 (+9.999847V)	077760 (+4.9976V)
+1/2 SCALE	040000 (+5.0V)	100000 (+5.0V)	040000 (+2.5V)
Zero	000000 (0V)	000000 (0V)	000000 (0V)
-1/2 Scale	140000 (-5.0V)	Not Applicable	140000 (-2.5V)
- Full Scale	100000 (-10.0V)	Not Applicable	100000 (-5.0V) Page

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3.21 Typical Local Control Front Panel Operations

3.21.1 Digital Output: Loading a D/A Converter

Assumption: A 12 bit, ± 10 volt, AC1562 four channel D/A converter is located in slot J12 of the master chassis. We wish to set the output of the last channel on the card to 0 volts, followed by + 5 volts, and finally -9.375 volts.

1) Energize the system, and press the REMOTE/LOCAL button to put the system in "local" control.

2) Set the switch register to 000057, the address for the last digital channel in slot 12 of the master chassis, and press the DIGITAL button. The address register should display 57.

3) Set the switch register to 000000, the code for 0 volts for a bipolar converter, and press the OUT button. The 000000 data is being sent to channel 57 twice each second.

4) The code for + 5 volts is 040000, so we can change the switch register to this code, and the system will automatically update the D/A within 0.5 second. It is possible that the update pulse will occur while we are moving the switches, causing a spurious code to be momentarily loaded into the D/A. To avoid this possibility we can press the IN button before moving the switches then press the OUT button after the switches are set. This action will inhibit update pulses while the switches are being moved.

5) The code for -9.375 volts is 104000. We can follow either technique described in step 4 to load in this new code. When we are through with this operation, we may want to perform another function on a different card at a new system address. However, before setting the new address into the switch register, we must exit from the "digital out" mode; otherwise, the new address will be sent to the D/A as data. We can exit from this mode by pressing the IN button as in step 4, or we can press the DIGITAL or the ANALOG button.

3.21.2 Digital Input: Reading a Digital Input Card

Assumption: We want to look at the 16 bit data connected to the first channel on a two channel digital input card, a DC6000, located in slot 3 of the third expansion chassis.

1) Energize the system, and put it in "local" control.

2) The address for slot 3 of the third expansion chassis is 0310. Set this address into the switch register, and press the DIGITAL button.

3) Press the IN button. The 16 bit data from the channel will be displayed on the data lites. The data is coming directly from the inputs on the DC6000, and any alterations in the data at the input of the DC6000 will be displayed immediately.

3.21.3 Analog Input: Reading an Analog Input Channel

Assumption: We want to read the analog input from the third differential channel of an AC4720 input card located in slot 4 of the second expansion chassis. The signal processor card AC260 has a gain of two, and the system A/D converter is a 12 bit, ± 10 volt unit.

1) Energize the system, and put it in "local" control.

2) Set the upper two digits of the switch register to the desired signal processor range code (00 to 17), and set the lower four digits to the desired analog channel. In this case, set the switches to 112144 (11 = range, 2144 = address).

3) Press the ANALOG button. The range and address registers will be loaded with 112144, and the A/D converter results will be shown on the DATA display and updated twice each second.

4) Assume the DATA display shows 103740. According to the analog data interpretation guidelines for a ± 10 volt A/D converter, this code equals a voltage of -9.384766. Since this result has a gain of two preceeding it, the actual voltage at the card input is half this value, -4.692383.

3.21.4 Analog Input: Dynamic Operation

In the preceding example the analog input from the selected channel is always connected to the input of the signal processor card and remains at a static level that is measured twice each second. However, in a computer controlled measurement the input level is not static; the channel is addressed just before the conversion is started. The "dynamic" operation simulates this variable input. If the DYNAMIC button is pressed, the system will "rest" on a channel other than the one to be measured until just before the measurement is made. The "rest" channel address is found by complementing the MSB of the address.

Thus, in the preceding example the system would "rest" on channel 5144, the third differential channel on a card in slot four of the fifth expansion chassis. If this channel is connected to a known voltage source (preferably, a variable voltage source), the DYNAMIC mode can be used to examine the effect on the system of acquiring a voltage after "resting" on a different voltage. Obviously, the usefulness of the DYNAMIC mode is limited to special testing and evaluation situations where suspected system problems are being debugged by knowledgeable technical or field service personnel using controlled system configurations.

3.21.5 Digital Input: Reading Back the Range and Address Registers

1) Energize the system, and put it in "local" control.

2) Set the switch register to 123456, and press the ANALOG button. 12 will appear in the range register, and 3456 in the address register.

3) Set the switch register to 002000, which is the digital input address, to readback the range and address registers. Press the DIGITAL and the IN buttons. 123456 will appear on the DATA display, indicating a correct readback of the range and address registers. Note that the range register display is blanked since the system is in the digital input mode.

3.21.6 Digital Input: Reading the Switch Register

1) Energize the system, and put it in "local" control.

2) Set the switch register to 007000, the switch register readback address, and press the DIGITAL and IN

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buttons. 7000 will appear on the DATA display. Now as the switch register is varied, the DATA display will follow it since in the digital input mode there is a direct connection between the source and the display.

3.21.7 Digital Input: Servicing a User Card Interrupt

Assumption: To service a user card interrupt, a user card capable of causing an interrupt must be properly installed in the system and must be requesting interrupt service. For example, assume that there is a frequency counter card DC6300 installed in slot J1 of the master chassis; we will force it to create an interrupt.

1) Energize the system, and put it in "local" control.

2) The REQUEST lite on the front panel should be off since all interrupt generating cards are disabled during power-up. Set the switch register to 000003, the address of the interrupt register on the frequency counter card, and press the DIGITAL button. Press the OUT button which will send 3 to address 3, thus setting the interrupt enable bit and the interrupt trigger bit on the card. Note that the REQUEST lite comes on. Press the IN button to terminate the output transaction.

3) Set the switch register to 004000, the address for reading interrupt vectors, and press the DIGITAL button. Press the IN button, and the DATA display will show the interrupt vector set on the PC vector switch on the frequency counter card. (Note that only the lower 8 bits of the data word are meaningful when reading vectors.) The REQUEST lite will go off.

4) Press the ANALOG button to terminate the digital input transaction. The REQUEST lite will stay off since only one card was requesting service in this example. If another card had been requesting interrupt service, the REQUEST lite would have come back on; in this case, pressing the DIGITAL and IN buttons would have allowed the second vector to be read.

3.21.8 Digital Ouput/Analog Input: Controlling SSH Cards

Assumption: The system has a four channel simultaneous sample-and-hold (SSH) card AC280 installed in slot J3 of the master chassis. We want to read the signals connected to the card while the channels are in "sample," and we want to verify that the channels can be put into "hold."

1) Energize the system, and put it in "local" control.

2) Press the CLEAR button, putting the AC280 in the "sample" state.

3) Set the switch register to 100100 (10 = single-ended unity gain; 0100 = address), and press the ANALOG button. The DATA display will show the A/D conversion result for the first channel. Set the switch register to 100110, and press the ANALOG button to see the result for the second channel; set the switch register to 100120, and press the ANALOG button to see the result for the third channel; set the switch register to 100130, and press the ANALOG button to see the result for the fourth channel. (Note: the AC280 has offset controls for each channel that, when properly adjusted, will give accurate results when the channels are read in "hold" under computer control. When the channels are read in "sample," there will be a small error, approximately 5 to 20mV.)

4) To command the units to go into "hold," set the switch register to 004003, press the DIGITAL button, then press the OUT button. Press the IN button to terminate the OUT transaction.

5) Repeat step 3 to read the analog values for each channel. The results from each channel will appear to drift away from the original value at rates of speed that depend upon the droop characteristics of each channel. A typical sample-and-hold amplifier has a droop specification of 1mV/msec; thus, when a computer controlled measurement is made 200 μsec after the "hold" command, the output will have changed by no more than 0.2mV. In "local" control the same droop rate can be thought of as 1 volt/second, and the analog results may appear to drift quickly away from their original values.

6) The sample-and-holds may be put back into "sample" by pressing the CLEAR button or by repeating step 4 with an address of 004000.

3.21.9 The CLEAR Button: System Initialization

The CLEAR button may be pushed at any time during "local" control to initialize the system status. The exact functions performed by the CLEAR button depend upon the design and the jumper options of the installed user cards since the clear line is available to all the user cards on the user bus.

A. Functions always performed by the CLEAR button:
   1) Range Register Set To Zero
   2) Address Register Set To Zero
   3) Analog Input Mode Set

B. Possible functions of the CLEAR button (Dependent on user cards and jumper options selected):
   1) All S&H Cards Set To "Sample"
   2) Relays Opened
   3) Digital Outputs Set To Zero
   4) DAC Input Latch Set To Zero

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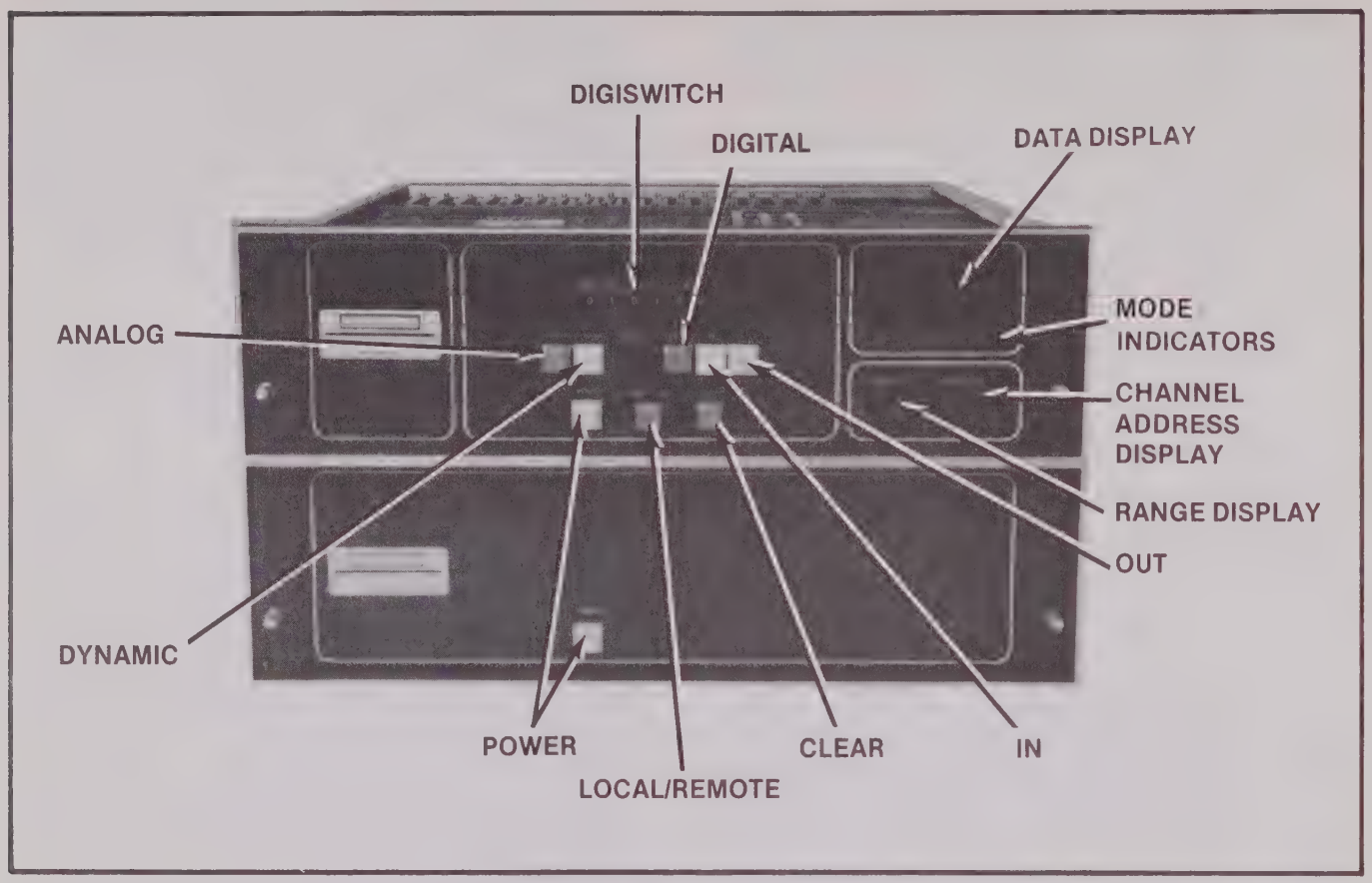

Figure 3-2. Front Panel Controls and Display

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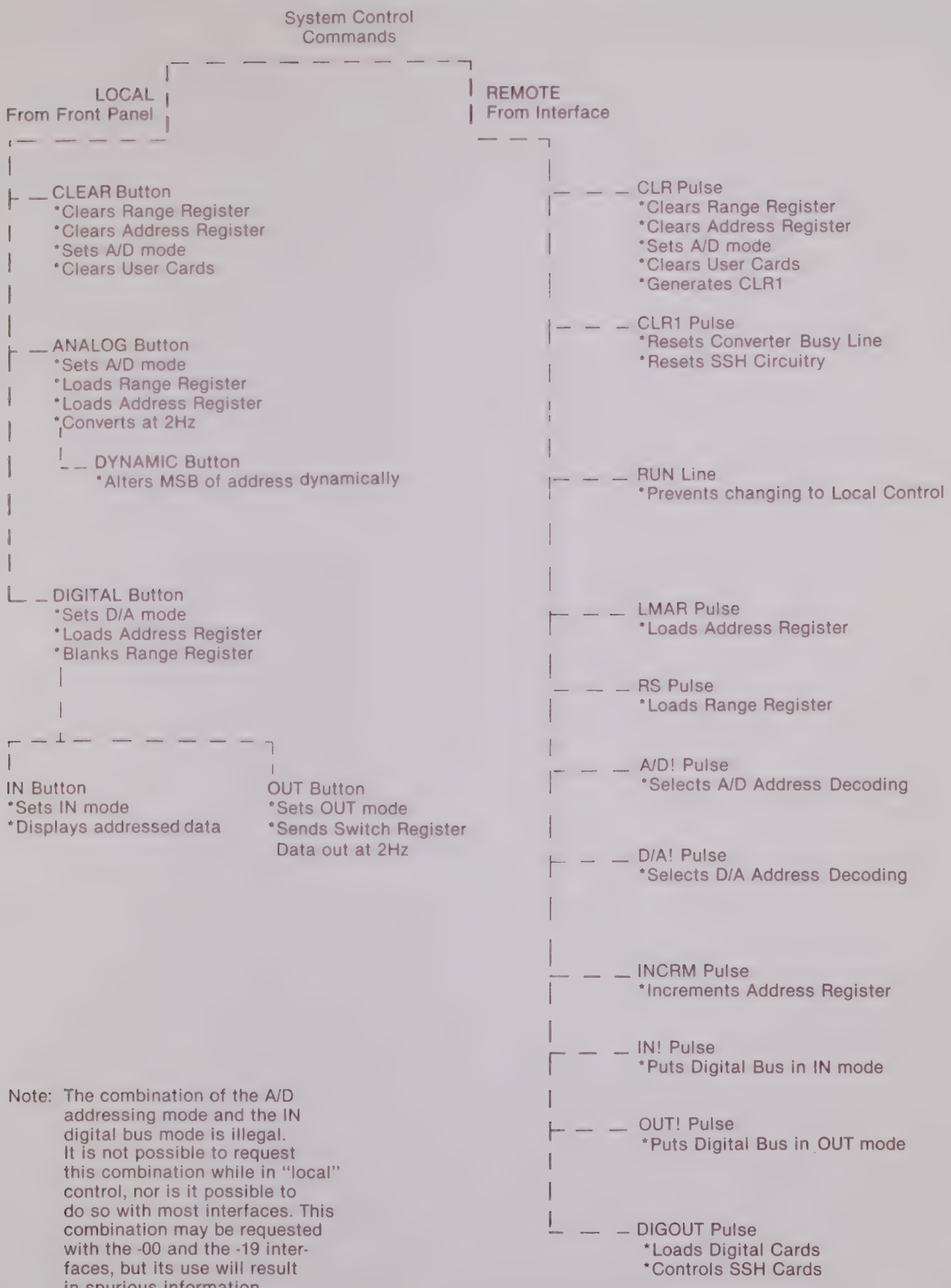
Figure 3-3 Functions in "Local" and "Remote" Modes



Note: The combination of the A/D addressing mode and the IN digital bus mode is illegal. It is not possible to request this combination while in "local" control, nor is it possible to do so with most interfaces. This combination may be requested with the -00 and the -19 interfaces, but its use will result in spurious information.

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4 PERFORMANCE ENHANCEMENTS

4.0 Introduction

This chapter answers the most commonly asked questions about performance, accuracy, noise, calibration techniques, wiring techniques, and reliability; and it provides suggestions about the choice and location of user cards and about alterations in software and hardware that allow the user to optimize the system's performance.

Large scale (greater then 100 channels), high speed (greater than 1000 channel/sec measurement rate) data acquisition systems have only been available since the mid-sixties. With the advent of high speed computers, which could make decisions and deal with data at a very high rate, the main limitations on overall system capabilities were the peripherals that brought information to the computer, stored information, or displayed the results. In the early days of analog data processing, "automated" versions of standard laboratory equipment brought information to computers; but it was soon apparent that these devices, which were designed for manual usage to measure and display data for visual interpretation, lacked the speed and reliability required under computer control.

Analogic was among the first companies to repond to the needs of the industry. We announced our first high speed multiplexed system (the AN5200) in 1969; this was followed by the AN5800 system, the AN5400, and ultimately the ANDS5400. Today's system incorporates sophisticated direct memory access and memory-mapped interfaces, digital input and digital output capability, vectored interrupts, switching power supplies, precision transformer isolated amplifiers, large expansion capabilities, and a host of features that makes it easy to use without sacrificing economy. The ANDS5400, achieving an excellent balance of speed, accuracy, and flexibility, exemplifies the state-of-the-art data acquisition system.

However, despite the tremendous advances in flexibility, architecture, and economy, today's system is only slightly faster and more accurate than the first systems Analogic produced! This is due to basic limitations dictated by the laws of physics and electronics as they relate to multiplexed data acquisition systems. A graph of increases in analog measurement speed and accuracy during the last three decades follows a curve that is exponential in nature with current equipment well along the "flat" portion of the curve. On the other hand, increases in the speed and capability of digital computers over the same time period have been so dramatic that a graph follows an almost constantly rising straight line.

It is very difficult to produce consistantly high quality analog measurement equipment with today's speed and accuracy requirements because there is little margin for error; yet it is still possible, and at Analogic we take great pride in our exhaustive component selection, burn-in, and thorough automated testing that, according to our customers, result in the best equipment on the market.

The ANDS5400 was designed to measure 100,000 channels of data per second with an analog accuracy of 0.01% of full scale range. This basic checkpoint is achieved with a -19 interface, an AC262 signal processor, an AC2712 A/D converter, and an AC4720 input multiplexer card. Other combinations may yield slightly higher throughputs or accuracies. At this speed the system must receive an analog address, acquire the analog signal from the selected channel, convert it to a digital value, and indicate the completion of the conversion to the user.

In this example, the 10 μsec that elapse from the start to the end of the conversion process includes 6 μsec for the loading of the address and the acquisition of the analog signal and 4 μsec for the A/D conversion. About 1 μsec is required for the address to stabilize and reach the input multiplexer card, so only 5 μsec are available to acquire and settle on the new analog signal to an accuracy of 0.01%. The settling time requirement is dominated by the time constant dictated by the analog bus characteristics. Since it takes 10 time constants to settle to 0.01%, the entire system time constant must be less than 500 nsec, resulting in a full power bandwidth requirement of more than 2Mhz! At this speed the system must handle 20V p-p signals in a differential configuration and maintain noise of less than 1mV p-p. Since the system will digitize errors caused by poor wiring or poor usage as well as the desired signal, at these speeds and accuracies careful control must be exercised by the user in signal wiring, noise reduction techniques, channel usage, and software control to optimize the system's performance.

4.1 Minimizing Measurement Errors

4.1.1 Single-Ended, Pseudo-Differential, or True Differential Signals

Usually one of the first questions asked during system purchase or installation is what type of input configuration should be used. The three available types are explained below.

4.1.1.1 Single-Ended Signals

It is important to realize that all voltages have two measuring points. In the single-ended mode of operation one point is the source output, the other point the

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ANDS5400 system chassis. The accuracy of the measurement depends on how well the source return is connected to the ANDS5400 chassis. Any ground currents, ground loops, or magnetic fields that cause a voltage drop in the connection between the chassis and the source return will distort the accuracy of the measurment. When there are many sources spread over a large distance, there will likely be several different paths between the source returns and the chassis, causing many types of errors. This situation is similar to that of connecting the low side of a digital voltmeter to its own chassis and probing the signal levels in a computer system with the positive lead; it is possible to distinguish a "1" from a "0" with this technique, but the ground pins of the IC's will read 100 to 300mV above ground because of the ground drops in the computer chassis and in the ground lead of the AC line-cord. Even with careful wiring, the single-ended mode of operation should be avoided if accuracies better than 1% of full scale (± 10V range) are required.

4.1.1.2 Pseudo-Differential Signals

In pseudo-differential operation the signal return line is disconnected from the ANDS5400 chassis and brought closer to the sources, and the return line is tied to a point that is as close as possible to the return leads of all the sources. Unfortunately, if the sources are spread over a great distance, there will not be a common point that can serve as the return for all of them. This situation is like the digital voltmeter case cited above, except that the low input of the meter is connected to the ground pin of an IC in the middle of the system. Thus, the drop in the AC line ground connection is avoided, but there are still ground currents flowing in the power supply to the IC's. However, careful wiring can result in accuracies approaching 1% of full scale on the 10 volt range.

To use pseudo-differential operation in the ANDS5400, the signal return line must be disconnected from the chassis and wired to the user's local return point. The signal return line is available at many points in a typical ANDS5400 system, and the user must be certain that there are no hidden connections to ground. The line is available on the "return" terminal at the rear of the chassis where a strap must be removed to free it from ground. The line is also available to all user cards on user card bus pins 20 and X. Some user cards do not use the line at all, but many bring it to the rear connector for customer usage. For example, the AC4720 user card brings the line to pins 22 and A for customer usage. The customer must be sure that no unknown ground connections are made on these pins, resulting in ground loops and causing additional errors. Finally, the isoplexer and thermoplexer user cards have internal jumpers that can connect signal return to ground; the customer must be sure that these are removed for pseudo-differential operation. If only one chassis in a multi-chassis system will be used in pseudo-differential operation, the customer need only be concerned with the signal return line in that chassis since the line is multiplexed and will be treated separately in each enclosure.

4.1.1.3 True Differential Signals

True differential operation requires two wires connected directly across each source for every measurement. Again, using the digital voltmeter example, this would be equivalent to putting the low side of the meter on the ground lead of each IC as its voltages are being measured. In this manner, since all ground drops and loops are avoided, the highest possible accuracy is achieved. Although true differential operation offers half as many channels for twice as many wires, in most systems it provides 10 to 100 times improved accuracy and significantly reduces the error condition of the installation.

Note that a ground reference must be provided to the system chassis from the transducer to limit the common mode voltage, unless an isolation amplifier card is used.

4.1.2 Analog Signal Input Wiring

Questions commonly arise about the length, type, and shielding requirements for input connections. Length is generally dictated by each installation; however, it should be noted that the noise brought into the system will usually increase with wiring length. Successful installations have been made with wires over 1000 ft. in length, but the customer must be certain that the loading effects of such a cable will not adversely affect the sources.

The type of wire chosen depends primarily on environmental factors. Only small currents flow in most input connections, so that the gauge of wire is important only for its resistance to physical breakage, although wires used with current inputs (e.g. 10-50mA) must support their rated current at full scale.

The shielding of the input connections is most important since only with proper shielding will the integrity of the original signal be maintained at the system input terminals. Two types of noise coupling, magnetic and electrostatic, must be avoided.

Magnetic coupling occurs whenever the two wires bringing the signal to the system form an open loop through which magnetic flux can pass. This "one-turn transformer" will cause the magnetic noise to add to the original signal. Nearly every environment abounds with 60Hz magnetic noise from power lines, transformers, etc. Commonly a 1 square foot open loop will pick up 10 to 300mV of 60Hz noise. In a differential input configuration the best solution for this magnetic noise is to twist pairs of wires, naturally forming very small loops in opposing directions, thus tending to cancel out magnetic noise. Two or three twists per inch are sufficient unless very large magnetic fields are present. Unfortunately, in single-ended and pseudo-differential modes there is no way to eliminate all loops since a single return line must serve for many sources; however, keeping the source outputs and returns physically close together will help.

Electrostatic or capacitive coupling is caused by rapidly moving external signals in close proximity to the signal wires; the capacitance between these signals allows noise to couple into the signal leads. Typically, the primary sources of this noise are the inputs to other channels wired to the system. The best solution for this type of noise is to shield the individual input wires or pairs of wires with braid or foil. The addition of a shield adds a capacitive "plate" between the noise and the signals so that the noise will couple to the shield and not to the signals. To be effective the shield must be connected to a low impedance ground. This ground connection should be made only at the source end of the wire; if the shield is grounded at both ends, it will form a ground loop that will carry large currents, making the shield itself a source of noise. Furthermore, since the original signal is best maintained by surrounding it with its own environment, grounding the shield at the source preserves the signal's purity. If we ground the shield at the system end, we will corrupt the signal with the "hostile" system environment through capacitive coupling. However, if the sources are truly floating (e.g. thermocouples), then the shield can be grounded at the system end. If cards with isolation amplifiers are used (e.g. isoplexers or thermoplexers), then the shield should be connected to the guard or shield terminal for each channel; this will surround the entire amplifier section with the source environment.

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In summary, the best wiring technique for grounded sources is a twisted differential pair that is shielded, with the shield grounded only at the source. When true floating sources are present, a twisted differential pair should again be used, but with the shield connected at the ANDS5400. For isolated amplifier cards a twisted differential pair should be used, and the shield should be connected to the guard input for each channel, whether the sources are floating or grounded.

Note: A ground reference must be provided to the system chassis from the transducer to limit the common mode voltage unless an isolation amplifier card is used.

4.1.3 System Ground Connections

What is the best way to connect the system ground terminals and power returns to other grounds in the installation? This is a difficult question because installations vary greatly and it is impossible to avoid conflicting ground requirements. Three terminals at the rear of the ANDS5400 labeled CHASSIS GROUND, POWER GROUND, and SIGNAL RETURN are all strapped together when the unit leaves the factory. In general, these straps should be left on. The CHASSIS GROUND terminal connects directly to the metalwork at the terminal, the POWER GROUND connects to the +5 volt and ±15 volt power supply returns, and SIGNAL RETURN functions as the low side of the analog input for single-ended or pseudo-differential measurements. SIGNAL RETURN should be left connected to POWER GROUND unless the pseudo-differential input mode is used. The CHASSIS GROUND is connected to the POWER GROUND to keep the potential of the chassis close to that of the internal power supplies; thus, the chassis acts as a shield for the internal electronics.

Many ground connections are made to the system during installation that may not be apparent. The system is grounded to the computer through the interface cable, it is grounded to the AC power system through the ground wire of the linecord, it is grounded to the rack through the slides, and it may be grounded to other digital devices through connections on digital input and output cards. Grounding conflicts cannot be avoided, but we recommend that that a ground braid be used to connect the analog source grounds to the system chassis and that all other external ground leads be connected only to the chassis terminal to avoid any large ground currents in the analog ground paths.

4.1.4 Source Impedance, System Leakage, and "Pump Out"

All analog input ports for the ANDS5400, except for current inputs, have very high impedances; however, the data sheets for some cards recommend a 1k ohm or lower source impedance. This suggestion stems from two potential problem areas: noise susceptibility and system "pump out." Since the system input impedance is very high, the impedance of the wiring will assume that of the sources; the higher the source impedance, the more likely the wiring will pick up noise.

System "pump out" occurs on cards like the AC4720 that have solid state multiplexers connecting the outside signals directly to the system analog bus. Since the analog bus is somewhat capacitive, it will maintain a "charge" at a level equal to that of the previous signal. When a new channel is selected, a reverse flow of current occurs, discharging the analog bus through the source. This "pump out" effect depends on the magnitude of the previously measured signal and the frequency with which new channels are selected; but, if the source impedance is less than 1k ohm, the charge will be absorbed by the source within the settling time of the system. Cards that have amplifiers or filters for each channel do not exhibit this effect, and cards that have one amplifier for several channels greatly reduce the "pump out" charge.

Another effect of the source/input impedance is the series resistive loop it forms in the analog input circuits. This error source can normally be ignored; however, if the customer designs a special input card for the system, this error should be carefully considered. The source impedance in series with the input impedance and wire impedance form a resistive divider network that will attenuate the voltage being delivered to the input. This calculable error source will have less and less effect as the input impedance of the design increases.

4.1.5 Common-Mode Constraints

In the differential mode any signal that exists on both the high and low input terminals is a "common" signal that should be rejected by the system. The magnitude of common-mode signals that can be rejected by the system and the frequency response characteristics of that rejection are factors that depend on the user cards and signal processor chosen for the system. Cards that have transformer-coupled isolated amplifiers (e.g. isoplexer and thermoplexer cards) can handle very large (300 volt) common mode signals with high rejection over a broad frequency range (DC to 1Mhz). Cards that are not isolated (e.g. any 47XX card) do not have any inherent common-mode rejection; they pass the differential signal to the signal processor for rejection at that point.

The common-mode rejection of the signal processor has both magnitude and frequency limitations that affect all non-isolated input cards; the customer must be aware of these limitations to optimize the performance of the system. Because the signal processor is the "gateway" through which all analog signals pass, it must have a very high bandwidth. Consequently, its differential amplifier is a "classical," double-buffered, textbook design, which offers high bandwidth but has two inherent constraints: the maximum amplitude of either input lead with respect to analog ground must be handled by amplifiers that run from the system power supplies; and the varying input paths in a multiplexed system result in capacitive imbalances, causing the common-mode rejection capability to taper off at high frequencies.

The common-mode voltage limitations for the AC261, AC262, and AC265 user cards are such that neither lead of a differential input can exceed 11.5 volts above power return; or, in other words, the signal plus common-mode voltage must be less than 11.5 volts with respect to power return. The AC260 has an additional constraint: (signal x gain) + common-mode voltage <11.5 volts. There are two easy ways to check the common-mode voltage in an installed system.

1) Connect an oscilloscope with the ground lead on the POWER RETURN terminal and examine each side of all the differential inputs at the system connectors. For the AC262, AC265, and AC261 neither lead can exceed 11.5 volts including peak noise excursions. For the AC260 the same limit holds for unity gain; limits of 6.5 volts, 3.5 volts, and 2.75 volts apply to gains of 2, 4, and 8, respectively.

2) Use the system to measure the common-mode voltage. Simply load in a unity gain, single-ended range code (00) and examine each individual input lead with the system A/D converter. Look first at the normal channel ad-

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dress for the differential channel; then look at the next higher address. Record the smaller of the two readings for each channel; then read the same channel differentially (range code 10). Add the low single-ended reading and the differential readings together and check the results against the limits listed above.

The frequency response characteristics of common-mode rejection for all the signal processors are similar. They exhibit high rejection: 80dB at frequencies from DC to 60Hz, about 40dB up to 5kHz, and 20dB up to 300kHz. These rejection characteristics are more than adequate in most system applications; however, if large amounts of high-frequency common-mode voltage are present, the isolation amplifiers are best.

4.1.6 Normal Mode Input Filtering

Various analog user input cards for the ANDS5400 have filters that limit the bandwidth of the signal before it is measured. These cards may be selected by the customer to eliminate unwanted harmonics, to provide "anti-aliasing," or to stabilize closed-loop systems. In addition, these filters reduce high frequency noise brought to the system through the wiring. The ANDS5400 has a wide bandwidth, and it will accurately measure small "spikes" on its inputs that are only 100 nsec wide. These noise spikes can be eliminated by averaging multiple measurements, but it is easier and faster to eliminate them at the input with a bandwidth limiting filter.

4.2 Accuracy Improvements

4.2.1 A/D Converter Resolution

Questions often arise as to the best choice of A/D converter resolution for a particular application or system. Higher resolution converters potentially offer more accuracy than lower resolution converters, but input signal noise, system noise or other measurement errors may make the increased resolution meaningless. The appropriate resolution for the job can usually be determined by answering the following questions:

1) How quickly must the conversion be made?

2) What accuracy (in % of full scale) is required?

3) Is very long term stability important, and/or is the environment subject to extreme variations?

4) Is repeatability of primary importance?

5) Will noise reduction techniques be used?

4.2.1.1 Conversion Speed and Accuracy

The answers to the first two questions, about conversion speed and accuracy, may limit the choice of converters. The higher resolution models run slower. (Refer to Table 1-2 in the "Introduction" chapter of Book One). Higher absolute accuracy can be obtained with higher resolution converters — up to a point. With a resolution greater than 13 or 14 bits, other system error sources begin to affect the accuracy of the converter. Therefore, additional resolution may be meaningless unless noise averaging techniques are used or unless questions three and four are answered affirmatively.

4.2.1.2 Stability

Question three, relating to a need for long term stability and/or long term calibration requirements, reflects the fact that the higher resolution converters have been designed to keep their accuracy for the same length of time and under the same environmental conditions as the lower resolution converters. Since the performance requirements are much more stringent in the high resolution converters, they use higher quality, more stable components to meet the accuracy goals over time and temperature. As a result, a 14 bit converter might be a better choice than a 12 bit model in applications involving long calibration cycles and/or severe environments, even if the higher resolution is not needed.

4.2.1.3 Repeatability

An affirmative answer to question four may indicate that repeatability is a more important factor than accuracy in a particular application. For example, in closed loop control it may be important to keep a process established at a particular set point, where the absolute value of the set point may not be of as much importance as the stability of the control, the monotonicity of the conversions, and the ability to return to the same point after an external disturbance. In such an application the higher resolution converters are most appropriate since their increased resolution and stability and their higher accuracy allow for tighter control.

4.2.1.4 Noise Reduction

The last question deals with the reduction of system and measurement noise errors so that the higher resolution available from the converter can be used. Two types of noise reduction are of primary importance. First, input bandwidth limiting could be used to limit the system's response to high frequency noise (i.e. use low bandwidth input cards from the "isoplexer" series or use filter input cards from the AC4700 series). Second, software averaging techniques can be used to "filter" out spikes and high frequency noise by averaging several readings together. Experience has shown that in a typical application 20 averaged readings on a single channel will produce results that are pure and quiet to a 15 bit level.

The basic suggestion is to choose the highest resolution converter that can be used within the speed constraints of the system. This will provide the most latitude in any future requirements that may arise during system integration. Economic pressures may affect converter choices; however, remember that the converter is the one gateway through which all analog information must pass, and its price is reflected only once — no matter how large the system may become.

4.2.2 Periodic Calibration

ANDS5400 systems can differ so much in size and type that it is very difficult to recommend a specific calibration technique or interval. However, on most systems the following maintenance and calibration procedures should be performed every six months:

1) Cleaning: Remove the system chassis and vacuum out any dust or dirt accumulations. One at a time, remove all user cards and clean all contacts with an alcohol solvent (do not use any abrasive cleaners). Replace all user cards.

2) Power Supply Adjustment: Adjust all power supply outputs to within 1% of nominal for each output under load. (Note: three adjustments are required on standard units, six adjustments on chassis with the optional AC3500 supply.)

3) Analog Calibration: Using "local" control and precise voltage standards, calibrate the signal processor timing, the A/D converter, the signal processor offsets, the

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expansion chassis expansion card amplifiers, any analog input cards with adjustments, and any analog output cards.

4) Interface Verification: Run a diagnostic program that is suited to verify the performance of the interface between the host computer and the ANDS5400 system. Analogic supplies such programs for the PDP-11 and the LSI-11 interfaces.

5) Analog Verification: Run a program designed to check the A/D converter, the signal processor, the expansion bus structure, and the user card bus. Analogic's self-test program, available for the LSI-11 and PDP-11 computers, serves this purpose.

6) User Card Verification: Run a program that can exercise all user card inputs and outputs both analog and digital to insure integrity between every system connection and the computer. The Analogic exerciser program, available for LSI-11 and PDP-11, is ideally suited for this purpose.

7) Detailed User Card Performance Checks: It is tedious and difficult to check some very complex user cards (e.g. frequency counter, bridge completion (strain gauge), and COS cards) with general purpose programs. For cards like these a specific diagnostic and test program is best. Analogic offers these programs for complex user cards interfaced to the LSI-11 computer.

4.2.3 Environmental Controls

The ANDS5400 has been designed to operate in a wide variety of environmental conditions. It does not require "clean room" or "computer room" placement, but, as a high precision instrument it should be in a "human tolerant" environment. Each chassis dissipates up to 200 watts. A large system may require forced air to keep the temperature between the user cards below 60°C. This larger temperature rise is found in a very limited number of installations and usually only under faulty conditions; e.g. bridge completion (strain gauge) card inputs where, for one reason or another, a number of sensor faults have occurred. Since heat rises, the system has been designed to accept convection cooling with a flow from the bottom to the top, but this flow can be hindered completely if the system is sandwiched between two solid covers. Therefore, two 1.75 inch blank panels should be used on either side of a ANDS5400 system that would be sandwiched between two solid covers. In multi-chassis installations every two chassis should have a 5.25 inch blank panel between them and the next pair of chassis. Basically, as with any rack mounted installation, the idea is to spread out all of the chassis within the space allowed. When the system is fully installed, measure the temperature between adjacent user cards to ensure that at no point does this temperature exceed 60°C.

The ANDS5400 is less sensitive to vibration than most electronic units because it does not have any moving parts (except relays on some user cards) and the PC cards are small and well supported. Any continuous vibration that causes perceptible movement of the user cards should be avoided; but the system has been designed to survive in any commercial or moderate industrial application and has passed fairly severe seismic qualification tests for use in nuclear monitoring environments.

Extremely dirty or corrosive atmospheres should be avoided since the ANDS5400 may have over 1500 plug-in connections in a single chassis installation. Analogic uses high-quality gold plated contacts, but the negligible current flows in the analog and CMOS digital bus structure are susceptible to degradation after a long exposure to dirt or corrosives, like salt. As described in the "Maintenance and Calibration" chapter, the contacts should be cleaned every six months with an alcohol solvent. All relays used in the system are sealed and do not require any maintenance.

4.2.4 User Card Locations

A significant advantage of the ANDS5400 is its universal bus structure that allows the user to place any type of card in any location, provided that the maximum system power draw is not exceeded. To optimize the performance of the system there are some configuration of the user cards the should be avoided to prevent unexpected noise.

Analogic has taken steps to prevent the introduction of noise from asynchronous sources within the chassis, but we have no control over the introduction of noise from user connected signals. Therefore, unless cabling, space, or addressing constraints prevent it, the user cards should be arranged in three catagories in the order listed below:

1) Analog input cards
2) Analog output cards
3) Digital input/output cards

In this way, the noise from the signals coming to the digital input cards and the noise generated by the digital output cards (or relay contacts) will not be close to the analog cards, and the noise generated by the analog output cards will not couple to the analog inputs. In addition, the digital cards and analog output cards tend to produce a lot of heat which can be kept away from the analog input cards. For optimum separation in a multi-chassis installation, the first chassis can be used for analog inputs, the second for analog outputs, and the third for digital cards. Be sure to avoid empty slots within the "digital" chassis before any interrupt generating cards; otherwise, the interrupt priority chain will be broken.

4.2.5 Slew Rate and Settling Time Error Reduction

The error caused by scanning from one channel to the next when the channels have voltages that are at the extreme opposite ends of the input range is due to settling time and slew rate limitations within the analog structure of the ANDS5400 system. An exaggerated illustration of this problem appears below:

CHAN 1 Input = −9.900 volts
CHAN 2 Input = +9.900 volts

System Results
(Each channel read three times, continuous scanning sequence)

CHAN 2 = +9.900
CHAN 1 = −9.126
CHAN 1 = −9.900
CHAN 1 = −9.900
CHAN 2 = +8.973
CHAN 2 = +9.900
CHAN 2 = +9.900
CHAN 1 = −9.104

This over-dramatized example illustrates a failure of the system to acquire the new input voltage before the A/D conversion begins. In the ANDS5400 the input signal is connected to the signal processor at all times until the analog address changes. When the address changes, it takes some finite amount of time for the voltage from the

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new channel to settle to rated accuracy at the signal processor output. The ANDS5400 receives the new address and the command to measure simultaneously. To allow for some settling time, each signal processor has a delay so that the new signal can be acquired before the A/D converter is started. This delay is set at 6 μsec in the AC262, 14 μsec in the AC260, and varies from 7 to 70 μsec in the AC261 (depending on gain). These fixed delays allow the input to settle to an accuracy of 0.01% of full scale for an input change of 20 volts when using any Analogic user card within its operating limits. This error can amount to 2 millivolts; it may be more if a source impedance higher than the specified 1k ohm is encountered.

Although these errors are fairly small, they will show up on converters with more than 13 bits. If the input voltage to the system is allowed to exceed full scale, the errors can grow significantly because the input range would then exceed 20V, thus requiring even more settling time.

If these errors prove troublesome, two approaches will minimize them. One approach is to increase the settling time by lengthening the delay time established by the signal processor before the conversion is started. This is usually accomplished by adjusting the delay pot on the signal processor card; refer to the signal processor schematic, data sheet, and theory of operation in Book One to make this adjustment. The necessary time increase might be 20% or 30% to lower the error to less than 1mV. The second approach is to allow for a second conversion on each channel in software which would effectively double the settling time for each channel.

This approach might be applied only to channels where a large voltage change from a previous channel is expected. If this software approach is used, be sure that the first reading is disregarded (do not average the two readings together) and be sure that the second reading is taken immediately after the first without addressing a new channel (do not scan a series of channels twice, because the second scan will have the same settling time errors as the first scan).

The problems outlined above will not exist in most applications as long as the source impedance is less than 1k ohm.

4.2.6 Dielectric Absorption Error and Its Reduction

Dielectric absorption refers to the property of a capacitor that allows it to "remember" the last voltage that was applied to it. A large electrolytic capacitor can be charged to a high voltage, discharged with a short circuit, and, when the short is removed, the capacitor will recharge to a large voltage all by itself. The voltage that caused the "recharge" was held by impurities in the dielectric of the capacitor that absorbed a charge initially but did not release that charge immediately when the capacitor was shorted. This same effect exists in a data acquisition system but, fortunately, to a much smaller degree. When a channel is selected, the system analog bus, the analog expansion cables (if used), the expansion cards, the internal backplane, the signal processor PC board, and the capacitor at the output of the sample-and-hold all charge up to the voltage that is applied to that channel.

All the elements that make up the analog bus structure have some dielectric absorption error associated with them, and, when a new channel is selected, this "leakage" from the dielectric capacitor will have some small effect on the reading from the new channel. In a typical ANDS5400 installation this error is less than 2mV in the worst cases and looks much like a slew rate error since it depends upon the voltage on the previous channel, but several characteristics can be noted that will differentiate between the two:

1) A slew rate error will appear even if the first conversion selects the first channel for only a brief time; a dielectric absorption error will appear only if the first channel is allowed to charge up for several hundred microseconds or more.

2) If the voltage difference between the first and second channels is reduced, a slew rate error will disappear very quickly, yet a dielectric error will be reduced only in proportion to the reduction in the voltage difference. For example, a 10% reduction in the voltage difference may completely eliminate a slew rate error but would only reduce the dielectric error by 10%.

3) Dielectric absorption errors are very sensitive to the time spent on each channel because their time constants are much longer than any others in the analog bus structure. If the error on the second channel depends on how long the first channel was addressed or if the second channel error tapers off slowly with successive measurements made on the second channel, then it is a dielectric error and not a slew rate or settling time error.

Dielectric absorption errors are quite small. Analogic uses the highest quality polystyrene capacitors in critical locations to minimize the errors, but they may be noticable with high resolution systems, particularly those with high signal processor gains since the signal processor amplifies the dielectric errors from the analog bus. If in critical measurements the errors become troublesome, the user can take several steps to minimize them.

1) If the analog bus is driven by a low impedance, the source can override the "leakage" caused by dielectric absorption in the bus structure. Many analog input user cards have amplifiers on them which will override the "leakage" (e.g. isoplexers, thermoplexers, AC4700's with filters, etc.). However, some cards do not have such amplifiers (e.g. AC4720, self-test external inputs); and, if a card without an amplifier is driven by a high source impedance (i.e. greater than 1k ohm), the dielectric error will be aggravated.

2) Some dielectric absorption error comes from the sample-and-hold capacitor in the signal processor. Signal processors that have an auto-zero feature hold the voltage across this capacitor at zero unless a measurement is in progress; this feature effectively reduces the error. Thus, the AC260 and AC261 are less prone to dielectric errors than the higher speed AC262.

3) Since the dielectric error depends on both a long "charge up" time and the selection of a channel with a voltage that is far different than the next channel to be measured, it may be worthwhile to select a channel with zero volts when the system is not in use. See the "Rest Channel" section in this chapter.

4) If a large number of input channels are to be used with a high gain signal processor, it will help to group these channels together and, after "resting" on zero volts (the "rest" time need be only about 1 msec), measure the channels sequentially.

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4.2.7 Noise and Quanitization Reduction Through Signal Averaging

To achieve the ultimate in accuracy, resolution, and noise reduction, average several readings from a single channel together if time allows. If this approach is adopted, make ten or more measurements on a single channel (without addressing another channel between conversions), disregard the highest and lowest readings, and average the remaining answers together. Several benefits are derived from signal averaging:

1) Noise is reduced since the effect of a single random noise pulse is diluted by the averaging process.

2) Staying on one channel for several conversions reduces both the slew rate and the settling time errors; and disregarding the highest and lowest readings eliminates any single answer that is affected by speed.

3) Quantization error is reduced. Quantization is a natural result of any analog-to-digital conversion process, in which an infinitely variable input is expressed in finite numerical increments. For example, in a 12 bit, ± 10 volt A/D converter the LSB has a value of 5 millivolts, so input voltage changes of 2, 3, or 4 millivolts may not have any effect on the result. However, with signal averaging if there is a small amount of random noise, the averaged result will show the effect of signal increases that are smaller than the LSB of the converter. In fact, to achieve this goal, it is an advantage to have some noise to assist in the reading of signal changes smaller than one LSB. This averaging process is similar to a process called "dithering," used in some converters to attain finer resolution.

4.2.8 "OPEN" Channel Elimination

Often unused channels in a large data acquisition system are left "open" or completely disconnected from all signals. This is a poor practice because small leakages in the system usually cause these inputs to be driven to saturation at either the + or − power supply limits. The ANDS5400 system does contain protection against overvoltage inputs, but the protection is limited because protective devices add capacitance to the analog bus and any limitation to the input voltage range also limits the allowable common-mode voltage. The addressing of an "open" channel usually causes the entire analog structure to be driven into saturation, increasing the settling time required for the next normal channel. Even if open channels are not addressed during normal A/D addressing scans, they may still be addressed accidently during digital input or digital output transactions since the analog addressing structure is still "alive" while the system is in the digital mode. The best solution for these problems is to ground all unused channels. With differential inputs be sure to connect the two inputs together; then ground them to the chassis to eliminate unknown common-mode voltages.

4.2.9 "REST" Channel Selection

When the ANDS5400 system is not in use, it is best to leave the system addressed to a channel with zero volts to guarantee the smallest possible slew rate, settling time, and dielectric absorption errors on the first channel measured. One method of implementing this on a system that does not have all seven expansion chassis is to attach a connector to J7 on the master chassis expansion card in slot J18, shorting the three analog buses (EVEN, ODD, and SIGNAL RETURN) to one another and to the chassis. The result will be zero volts for all analog addresses from 7000 to 7777 (octal). The Data General and LSI-11 interfaces automatically select address 7777 at the end of a DMA scan when the DMA "stop" code is loaded into the address register, so no further action is necessary when using DMA scans with these two interfaces. Another method can be used if an analog input card is in slot J1 of the master chassis: if the input to channel 0 on this card is shorted to ground, a clear instruction can be sent to the ANDS5400 that will cause the selection of address 0000.

4.2.10 Automatic Calibration

If the ultimate in accuracy is desired and if some of the suggestions previously discussed have been implemented, the only remaining errors of any significance will be offset, gain, and linearity errors. These three errors will be very small indeed — virtually unnoticable with resolutions under 13 bits. However, if the highest absolute accuracy is desired, some steps can be taken to remove any residual offset, gain, and linearity errors. In order to discuss the solutions we must examine their main sources:

1) Linearity Errors are primarily caused by the A/D converter and secondarily by errors from high gain stages or very low pass filters.

2) Offset Errors are caused by drifts in any semiconductor stage, with or without amplification; e.g. an A/D converter, a signal processor, an expansion chassis amplifier, or any analog input card with amplifiers.

3) Gain Errors are caused by drifts in reference diodes or resistors used in A/D converters, signal processors, or high gain stages on user cards.

4.2.10.1 Automatic Calibration Techniques

4.2.10.1.1 Linearity Errors

Linearity problems are inherent in any successive approximation converter; for this reason Analogic uses bulk metal and wire wound resistors, both of which have the highest possible stability. Linearity errors in the converter components can only be corrected by the factory, but these errors can be difficult to notice. The best check of A/D converter linearity is done with the self-test card and program, which runs a complete check for missing codes and a complete analysis of converter linearity in about five minutes. This check should be done every six months as a regular part of periodic calibration.

Potential linearity problems also exist in any high gain stage when the open loop gain is unstable and small compared to the closed loop gain. In the ANDS5400 high gain stages are used in the isoplexers, thermoplexers, and AC261 signal processors. Because of careful design, component selection, and testing, the card's specified linearity is guaranteed. If verification is desired, the customer can run the specific diagnostic packages for critical user cards or the Exerciser package on any card to check the transfer function of the device at a few points.

4.2.10.1.2 Offset Errors

Offset drifts can come from various places, and in general they can be controlled by one of three techniques:

1) Manual Calibration: Because of the high stability devices used in the ANDS5400, offset errors can be compensated for with adjustments made every six months during periodic calibration. The programmable gain signal

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processors and the high gain isoplexers and thermoplexers have auto-zero cycles that automatically control offsets for very low drift.

2) Automatic System Calibration: The Self-Test Card or a shorted channel on an AC4720 multiplexer card provides an easy way to measure the offsets of the signal processor and A/D converter combination. Since these two devices are the "gateway" through which all measurements pass, a high confidence of minimum system offset can be obtained by comparing readings taken on a channel shorted to zero volts. A software program can be written that periodically measures the shorted channel; and, if the system offset exceeds pre-set limits, the software could automatically subtract the measured offset from all subsequent A/D readings or notify the operator of excessive offset. For maximum noise reduction with this technique, be sure to measure the offset using the signal averaging techniques described earlier.

3) Automatic Chassis, Card, or Channel Calibration: It is possible to go even further than system calibration, if desired.

a) In a multi-chassis system the user could measure a shorted channel in each chassis to include the expansion amplifier offsets; these corrections would then be subtracted from the readings taken in each chassis.

b) On most of the cards in the AC4700 series a pair of amplifiers is shared by all channels on the card. Therefore, a single shorted channel on the card can be used to measure all the offsets involved with that card in the system.

c) A relay can be used to switch each input channel to a shorted input for "per channel" offset measurement and correction. Since these offsets are so small, signal averaging techniques must always be used to obtain the most accurate corrections.

If these more advanced techniques are used, the earlier techniques can be abandoned since "per channel" offset measurements would include all system offsets.

4.2.10.1.3 Gain Errors

The same type of controls listed above for offset errors relate to gain errors associated with the A/D converter and the signal processor. Periodic manual calibration will be sufficient in most cases, but for the best control the Self-Test Card, which has a precise temperature controlled reference at 90% of full scale, can be used automatically to check the A/D and signal processor gain accuracy. Even tighter control can be attained with a switching relay per channel and an external programmable source such as the AC1916TC2D, which checks both offset and gain errors for each input. This capability is included on the bridge completion (strain gauge) card (AC4300) and the new isoplexer and thermoplexer cards. When measuring and correcting gain errors, either under computer control or manually, it should be noted that offset errors are being measured at the same time; therefore, offset errors must be removed before the gain errors can be detected. Again, signal averaging techniques should be used to make these delicate measurements.

4.3 Signal Averaging Using External Sync

Occasionally, because of poor wiring, insufficient shielding, or poor sensor design, the input signals may have an abundance of noise directly related to the 50Hz, 60Hz, or 400Hz power line frequency. If this noise appears, the signal averaging suggestions mentioned earlier will not improve signal integrity since all measurements will be made over such a short time that the low frequency noise will not be reduced. However, this type of noise can be reduced if a series of measurements are made that exactly span one cycle of the noise frequency. For such accurate timing the external sync connector (J28) at the rear of the ANDS5400 can be used to trigger the conversions at the precise time desired. For example, if 60Hz noise is the problem, a 600Hz clock applied to J28 will allow 10 measurements to span exactly one cycle of the line frequency. Refer to the "Architectural Overview" chapter of this manual for details on the use of J28.

4.4 Simultaneous Sample-And-Hold (SSH) Timing Relationship

The ANDS5400 system includes a digital command structure that allows for the simultaneous control of any number of sample-and-hold cards either through direct computer commands or through external user supplied synchronization pulses. This structure allows the user to "freeze" several different input voltages at one point in time so that they can then be measured sequentially without losing their original value. It is important to realize that the sample-and-hold units cannot hold their original output voltages indefinitely and will begin to deviate from their original outputs within prescribed voltage/time limits (typically 1 millivolt per millisecond). Consequently, the user must read the sample-and-hold outputs within a very short time after they have been put into "hold" to avoid errors caused by "droop".

For example, if we had eight channels that were put into "hold" at one time and we allowed no more than 2 millivolts of error from "droop," we have only 2 milliseconds to read all eight channels or 250 microseconds per channel. This is enough time for each conversion with most configurations, but it may tax the software and the computer interface beyond their capabilities. Some slow interfaces (e.g. Serial or IEEE) would be unable to measure one simultaneous sample-and-hold (SSH) channel without significant error.

In the fastest configurations with a 12 bit A/D converter, an AC262 signal processor, and a DMA interface capable of sustained conversion rates of 80,000 channels per second, we could measure about 100 channels of SSH with enough time allowed for the software to start the DMA after the "hold" command has been issued.

4.4.1 Dielectric Absorption in SSH Units

Another important parameter to consider carefully when using simultaneous sample-and-hold units is dielectric absorption. This problem can significantly affect accuracy in this type of input device. The primary element of concern is the amount of time that the device is in the "sample" mode as opposed to the amount of time in the "hold" mode. The ratio of these times, as shown in the formula given on the AC280/281 data sheet (see Book Two), will result in a specific and calculable error source at the output of the SSH. As a rule of thumb, as long as the ratio of "hold" time to "sample" time is less than 5, errors should be less than 1mV. Under any circumstances, the programming of the ANDS5400 system should reflect the following procedure: the SSH channels should be left in the "sample" mode except when actually holding a value for A/D conversion; and the exit from a SSH A/D conversion sequence is an immediate return to the "sample" command.

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4.5 Programmable Gain — How and When to Use It

The ANDS5400 offers several versions of signal processor cards that have software programmable gain. These signal processors add flexibility and capability to any configuration, but their function and use must be understood to avoid unneccessary errors.

In a multiplexed data acquisition system it is generally recognized that high gain and high common-mode rejection are design goals that are best met by having individual amplifiers serve each channel of analog input. If high gain occurs after the multiplexing, the errors will be amplified by the multiplexing structure. In addition, the requirements for high common-mode rejection conflict with the characteristics of a large analog bus structure and those of a wide-bandwidth "shared" amplifier. For these reasons Analogic offers isoplexer and thermoplexer cards that have high gain and high common-mode rejection achieved through an "amplifier per channel" approach.

It is sometimes thought that, in place of a high resolution converter, a shared programmable gain amplifier can be used to add resolution and accuracy to the measurement of any input signal. This assumption is only partly true. A programmable gain amplifier acts like a "magnifying glass," providing a closer "view" of the signal, but the magnification is centered around zero and, thus, cannot be used on a signal whose value, when multipied by the gain, exceeds the full scale capability of the system. For example, If a 0.5 volt sine wave is riding on a 6 volt DC signal, only unity gain can be used to measure the result to avoid exceeding the 10 volt system limit. It is possible to construct an amplifier with programmble gain and programmble offsets that would allow the magnification of any portion of the input signal, but these techniques are much more expensive and cumbersome than adding resolution to the A/D converter.

Common-mode rejection is another potential problem area. The highest practical rejection available in a wide-bandwidth amplifier is about 80dB with respect to the input signal. With a unity gain signal processor operating in the differential mode, 2 volts of common-mode signal will affect the A/D reading by only 0.2 millivolts, which would be unnoticable even with a 15 bit converter. However, with a programmable gain of 64, the same input would add 12.8 millivolts to the A/D input, causing 25 counts of error in a 15 bit converter. Additional problem areas include noise, slew rate, and settling time errors, all of which are amplified by any gain placed before the A/D converter.

Despite these potential pitfalls of "shared" programmable gain amplifiers, Analogic still offers these products to ANDS5400 users because in many applications wide range programmable gain amplifiers offer the most flexible, cost-effective solution to low-level measurement requirements. Let's examine the two available programmable gain signal processors to see how they can serve in many applications.

4.5.1 AC260 Signal Processor

The AC260 with X1, X2, X4, X8 programmable gains, both single-ended and differential, under software control has a basic measurement time of 14 μsec plus the A/D converter time. The timing is split into two sections: the first 7 μsec are used for the auto-zero cycle to minimize the offset drift of the gain amplifier; the second 7 μsec are used for acquisition time. The total time is sufficient to limit the A/D converter's slew rate and settling time errors to a maximum of 2mV with gain equal to 8. The common-mode voltage cannot exceed that defined by:

$$[\text{SIG X GAIN}] + \text{CMV} < 11 \text{ volts}$$

The wide bandwidth design of the AC260 depends on tight control of noise sources for noise reduction.

4.5.2 AC261 Signal Processor

The AC261 with X1, X2, X4, X8, X16, X32 programmable gains, both single-ended and differential, under software control has a basic measurement time that depends on the gain chosen. The timing consists of acquisition time plus a 10 μsec auto-zero time that begins simultaneously with the A/D conversion time. Acquisition time varies from 7 μsec (X1) to 70 μsec (X32). The AC261's unity gain performance is faster than that of the AC260 because the auto-zero cycle "overlaps" the A/D conversion time. Acquisition time is sufficient to limit errors caused by slew rate and settling time to less than 1mV at the input of the A/D converter. The common-mode voltage cannot exceed that defined by:

$$\text{SIG} + \text{CMV} < 11 \text{ VOLTS}$$

The amplifier bandwidth of the AC261 is dependent on the gain chosen and, thus, is far less dependent on tight control of noise sources.

4.5.3 Comparison of AC260 and AC261 Signal Processors

In summary, the AC260 offers low-cost moderate gain programmability with a slight speed penalty and common-mode restriction; the AC261 offers wider gain programmability with varying throughputs dependent on gain (no speed penality at unity), normal common-mode restrictions, and low noise. Both units will increase the capability and flexibility of any system. To achieve the ultimate in performance, high gain stages must be on a "per channel" basis on the user cards; but, for a small loss in accuracy, economy and flexibility can be attained with the AC260 or AC261. Both units have been designed to minimize slew rate, settling time, offset drift, and noise errors; thus, with the proper choice of user cards and adequate control of input noise and common-mode voltages excellent results can be obtained with the AC260 or AC261.

4.6 Analog Output Connections

While it is very important to use the proper wiring and signal conditioning techniques to insure that the analog readings from the ANDS5400 are as accurate as possible, it is just as important to use proper techniques to insure that the analog outputs produced by the ANDS5400 reach their destination with the greatest accuracy. The ANDS5400 offers three types of analog output capability:

1) Standard voltage output: the output voltage is referenced to the system power return. (AC1814, AC1900 Series)

2) Remote sense voltage output: the output voltage is referenced to a a high-impedance sense line that can be used to minimize ground drop errors. (AC15XX)

3) Current output: the output current must return to system ground, but it is not affected by ground loops. (AC1330)

Each type of analog output capability has its own characteristics and should be handled accordingly. The first type produces a very accurate voltage that is referenced to the power return of the ANDS5400. If the user has to drive a truly floating load, this can best be done with a shielded twisted pair of wires with the shield grounded at the D/A converter end. Unfortunately, many times the load is not floating but is grounded to a local

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ground that differs by several hundred millivolts from the power return to the ANDS5400. In these instances, the best way to maintain the original D/A accuracy is to use a differential amplifier to sense the D/A output voltage, reject the common-mode voltage, and drive the load. This amplifier must be situated close to the load so that its output will be referenced to the load ground. The input to this amplifier will look just like a floating load and should be driven with the same wiring technique.

The AC15XX D/A converter uses the second type of analog output technique, one that allows for the removal of most of the errors associated with grounded loads. This technique is similar to the conception of "remote sensing" in power supply design. Each of the outputs of the card has a separate sense lead for the low side of the load, compensating for ground drops up to one volt. Three twisted wires with a shield connected at the AC15XX end of the link should be used with this card.

The third analog output technique is the current output, where the D/A converter generates a precise current that is eventually returned to the ANDS5400 power return. Since the accuracy of this technique involves the magnitude of the current generated, there is no dependence on the voltage drops (including ground drops) in the loop as long as they are less than the compliance voltage of the current generator. If a floating load is being driven, a simple twisted pair of wires are sufficient; and, if the load is grounded, only one wire is necessary provided that there is a solid return path between the load and system grounds. Current loops that do not use twisted pairs tend to pick up electro-magnetic noise, most of which will be controlled by the D/A output stage unless the noise has a high frequency.

All analog output techniques will benefit from some low pass filtering at the load to limit high frequency noise pickup interference. This filtering is most easily implemented within the differential amplifier design or by shunt capacitance across current driven loads.

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5
MAINTENANCE AND CALIBRATION

5.0 General

If the calibration procedures detailed in this chapter are carefully followed, the system's specifications will be valid for six months, at which time recalibration and standard maintenance are required. It is strongly recommended that the user purchase the Self-Test Card and Exerciser Program; the calibration procedures are more easily performed using them since the calibration of gains, offsets, etc. are performed in "remote" rather than "local" control.

The user's reasons for turning to this chapter will determine which of the following procedures to perform. If the system is being calibrated during the initial installation, be sure to read the "Performance Enhancements" chapter first then the "Theory of Calibration" and "Typical Calibration" sections of this chapter. To perform the routine six month maintenance and recalibration, read the "Theory of Calibration" and "Maintenance" sections of this chapter. If cards were added or replaced or if the system has been expanded, then only the new cards and/or chassis need be calibrated, so read the "Theory of Calibration" and "Typical Calibration" sections of this chapter. If the system was repaired, check the problem area first, then calibrate the overall system according to the "Theory of Calibration" and "Typical Calibration" sections. If the user notices or suspects a degradation from the original level of performance, then attempt to calibrate the system according to the "Theory of Calibration" section, and the problem should become apparent.

5.1 Warranty and Maintenance Agreements

Refer to the "Quality Conformance" chapter for the Standard Warranty. In addition, a Supplemental Warranty and an Extended Maintenance Agreement are available on a contract basis from Analogic.

5.1.1 Supplemental Warranty

The Supplemental Warranty Agreement is available only while the Standard Warranty is valid. It is designed for the customer who prefers to have warranty repairs done on site and wants the additional features of installation assistance, scheduled preventative maintenance, and an additional two visits at the customer's request. The Supplemental Warranty features:

1 Scheduled Installation Visit
1 Scheduled Preventative Maintenance Visit
2 Additional Visits at the Customer's Request
Engineering Modification and Updating
Coverage Flexibility
Financial Planning

The preventative maintenance visit is a scheduled check-out service call at the customer's site after the equipment is installed. This visit is typically scheduled six months after the installation. Two additional visits are provided at the customer's request during the time the Standard Warranty is valid. Our field service engineers are experienced professionals and fully trained in Analogic's product lines and are supported by Product Line and Design Specialists.

Under this agreement the customer's system is updated during the scheduled preventative maintenance visits according to Analogic's engineering changes, thus keeping the system technically comparable with later production models.

Basic coverage is five days per week, eight hours per day. The service begins on Monday at 8:00 a.m., and service hours are consecutive from 8:00 a.m. in increments of 8, 12, 16, or 24 hours per day. The work week can be extended to include Saturday and/or Sunday.

Budget planning and cost control are made easier by this agreement since the customer has a fixed maintenance cost for 12 months. Note that under the Supplemental Warranty all parts and material are covered under the original Standard Warranty.

To purchase this contract, call Analogic's Customer Service Department (the telephone number is listed in the address block at the end of the "Table of Contents").

5.1.2 Extended Maintenance Agreement

The Extended Maintenance Agreement is offered for those customers who want full Analogic Field Service support available at their request. This 12 month, renewable contract has four scheduled preventative maintenance visits and an unlimited number of remedial maintenance visits per year. The Extended Maintenance Agreement features:

2 Scheduled Preventative Maintenance Visits
Remedial Maintenance Visits
All Parts, Material and Labor
Engineering Modification and Updating
Coverage Flexibility
Financial Planning

Two preventative maintenance visits are scheduled during the 12 month period of this contract, and any time during that 12 months remedial visits are made at the customer's request.

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The customer's system is updated during the scheduled preventative maintenance visits according to Analogic's engineering changes, thus keeping the system technically comparable with later production models.

Basic coverage is five days per week, eight hours per day. The service week begins on Monday at 8:00 a.m., and service hours are consecutive from 8:00 a.m. in increments of 8, 12, 16 or 24 hours per day. The work week can be extended to include Saturday and/or Sunday.

Since the customer has a fixed maintenance cost for 12 months, it is easier to plan and control maintenance costs. This agreement covers all parts, material, and labor needed to complete repairs. Parts and material are typically available at the Field Service Office, which is backed up by a comprehensive inventory at the Field Service Headquarters. Our field service engineers are experienced professionals that are fully trained in Analogic's product lines and are supported by Product Line and Design Specialists.

5.2 Repair Technique

All repairs are performed using a board-swapping technique in the field; board repairs are performed at the factory on special purpose test equipment, using factory selected and factory tested components.

5.3 Calibration

5.3.1 Required Calibration Equipment

The following equipment is required for calibrating the ANDS5400:

1 Data Precision Model 8100 Secondary Voltage Standard, or equivalent
1 Data Precision Model 3500 5 1/2 digit digital voltmeter (DVM), or equivalent
1 465B Tektronix Oscilloscope, or equivalent
1 AC70 Internal Backplane Extender Board
2 AC71 User Card Backplane Extender Boards
IC Clips, Probes, etc.

5.3.2 Adjustment Locations

Refer to the appropriate data sheets in the "Drawings and Specifications" chapter for the adjustment locations on the power supply, A/D converter, signal processor, expansion cards, and user cards. See drawing D7-8635 in the "Expansion Cards" section of that chapter to make the adjustments on AC334-1 Board 1; on this board the even bus offset is set by R2; the odd by R5.

5.3.3 Theory of Calibration

5.3.3.1 Computer Aided Calibration

The "Theory of Calibration" procedures must be carried out in "local" control since Analogic cannot provide software support for every possible interface and computer combination. DEC PDP-11 and LSI-11 users can take advantage of Analogic's Exerciser and Self-Test Programs to simplify the calibration and performance verification procedures.

There are several advantages gained by using the Exerciser Program. Individual user card calibration is best performed with the Exerciser Program. This program works through the interface, thus including this important link in the calibration process. It uses simple keyboard entry commands rather than lengthy front panel "button pushing." It runs at computer speed, performing calibration under dynamic conditions and can thus be used for Sample-and-Hold calibration. The Exerciser Program expresses values in "real" terms, with octal, decimal, and voltage conversions. It can access all analog and digital I/O channels and can provide printed verification of the test results.

Similarly, the Self-Test Card provides many advantages. This card works through the interface and provides all necessary digital and analog sources required for system performance verification and system calibration. With a single command it performs complex tests (e.g. settling time, common-mode rejection, etc.). It can produce a complete printed data sheet of the system's digital and analog performance. Finally, Test 12 (Code Center Generation) coupled with an external digital voltmeter provides a simple technique for accurately and dynamically adjusting system gains and offsets.

Refer to the data sheets and specifications supplied with these programs for more detailed explanations of their implementation as calibration tools.

5.3.3.2 System Performance Verification

All calibration must be done in "local" control and all cards must remain installed and all connections intact except for the specific user card being tested.

5.3.3.2.1 Power Supply

Verify that the straps to PWR RTN, SIG RTN, and CHASSIS RTN are in place on the rear panel of the master chassis. Using the chassis as a ground point, measure the +15V, −15V, and +5V supply voltages on the user card backplane with a digital voltmeter (DVM) and with the oscilloscope, looking for the rated DC voltages within 3% and observing less than 100mV of ripple. If the optional AN3500 supply is installed, be sure to measure these voltages on slots J7 and J16 on the user card backplane, thereby checking all six supply outputs.

5.3.3.2.2 A/D Converter

Modify the internal backplane extender board according to Figures 5-1 and 5-2 to provide for the insertion of a short circuit and a voltage source directly into the ADC and the signal processor.

CAUTION: Prior to turning on the power, be sure S1 is in position 1, S2 in position 1, and S3 in position 1.

Remove the ADC, mate it with the AC70, and install the combination into C74. Short the ADC input by moving S1 to position 1, observe EOC, and adjust the timing on the series AC8000 converter as necessary. To adjust the offset, adjust the ADC offset potentiometer for 000000 output from the ADC.

To test the gain move S1 to positon 2, and apply 75% full scale input to verify that the output of the ADC is approximately correct: with a bipolar ADC the display should read 060000; with a unipolar unit the display should read 140000. Do not adjust the gain potentiometer at this point.

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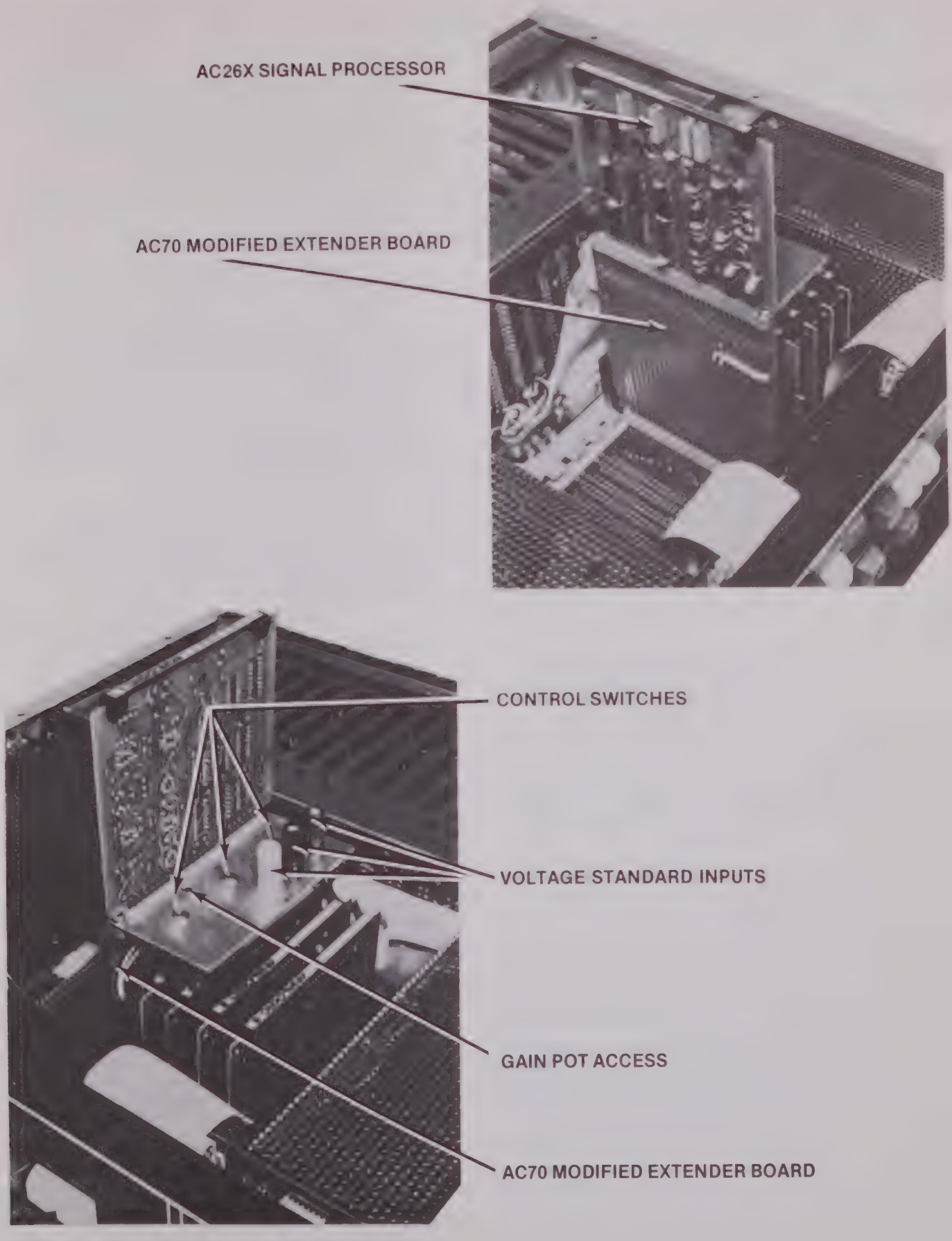

Figure 5-1. Modified Extender Board

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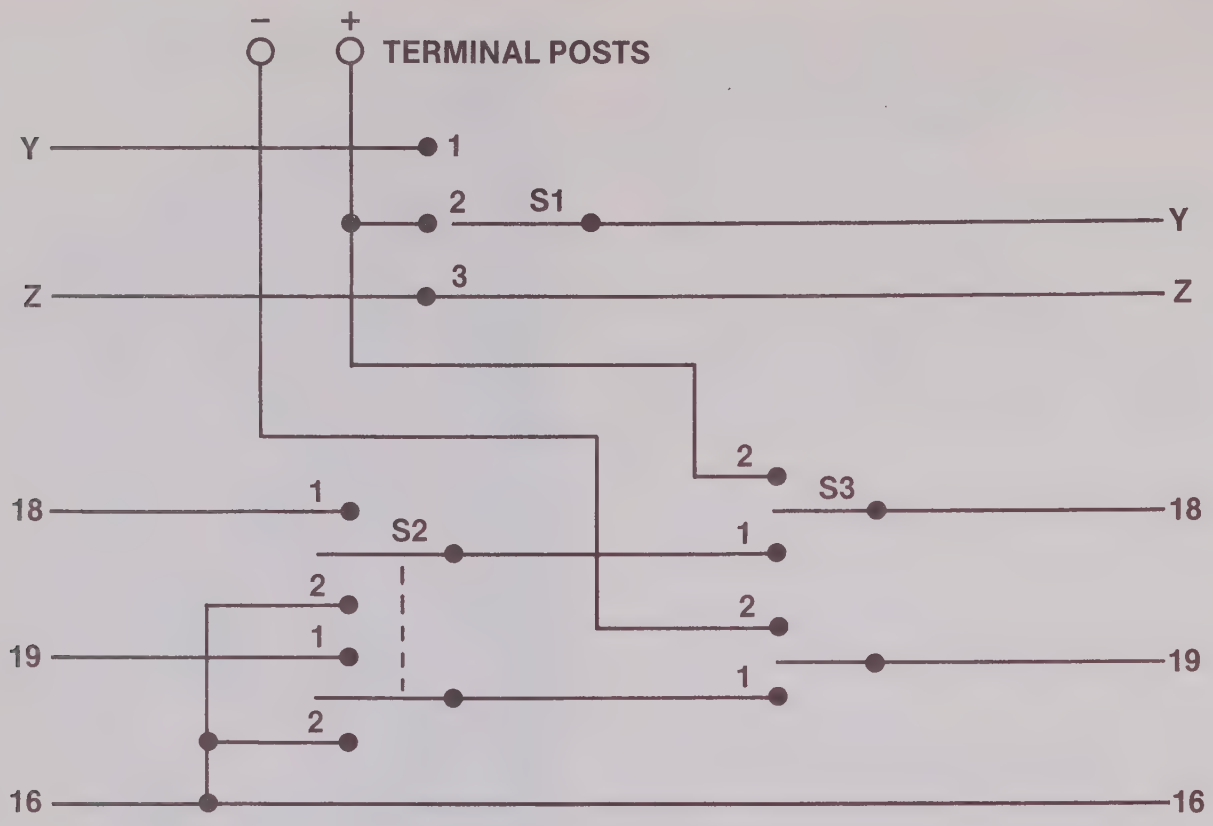

Figure 5-2. Modified Extender Board Schematic

5.3.3.2.3 Signal Processor

CAUTION: Prior to turning on the power, be sure S1 is in position 1, S2 in position 1, and S3 in position 1.

Unplug the signal processor, and mate it with AC70. Install the combination into C73, and adjust the timing of the signal processor according to the appropriate data sheet in Book Two. Short the signal processor inputs by moving S2 to position 2, and adjust the timing of the signal processor. Adjust its offset potentiometer to read 0 volts on the DATA display.

Move S3 to position 2, and apply 75% of positive full scale to the signal processor from the Secondary Voltage Standard. Adjust the gain potentiometer on the ADC to reflect the appropriate digital value on the DATA display: with a bipolar ADC the display should read 060000; with a unipolar unit the display should read 140000. See the individual data sheets for further calibration information. Reinstall the signal processor.

Shut off the power, and remove all the cards from the expansion chassis. Short pins 21, 22, and Y. Turn on the power, and load in range and address 00X000 (X ranges from 1-7, depending on the expansion chassis being adjusted). Press the analog button. Adjust R2 on AC334-1 on the expansion chassis being adjusted, and adjust the pot until zero volts is indicated on the analog voltage lites on the front panel. Then load 00X001 (X = chassis being adjusted), and adjust R5. Load 10X000, and verify that the answer is still zero. If zero does not appear on the analog voltage lites, repeat the last two steps. If zero still does not appear, call the Customer Service Department (the telephone number is listed in the address block at the end of the "Table of Contents").

5.3.3.2.4 Analog Input User Cards

Short all the channels to each other and to SIG RTN. Adjust the offsets on the individual cards according to the respective data sheets in Book Two. If there is a gain adjust on the card, apply a 3/4 full scale input of the card, and adjust the range according to the documentation in Book Two.

5.3.3.2.5 Analog Ouput User Cards

To calibrate the analog output user cards, follow the procedures detailed on the respective data sheets in Book Two.

5.3.3.2.6 Digital Input/Output User Cards

Normally no offset or range adjustment is required on the digital input/output user cards. However, DC6302 provides a high impedance comparator input for analog signals; therefore, an offset adjustment is required to establish the threshold at which triggering occurs. See the DC6300 data sheet in Book Two.

5.3.3.2.7 Special Considerations

Simulataneous Sample-and-Hold user cards are adjustable under computer operation to compensate for small pedestal offsets that occur during the sample-to-hold transition. See the corresponding data sheet in Book Two.

5.3.3.2.8 User Card Calibration

Special adjustments are required to calibrate the AC405X, AC407X, AC425X, AC427X, AC43XX input cards properly. Refer to the individual data sheets in Book Two for calibration procedures.

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5.4 Maintenance

5.4.1 Precautions

Preventative maintenance should be performed every six months. Remove any dust and clean all the contacts.

CAUTION: Some boards (particularly the signal processor and analog input cards) are sensitive to some cleaning solvents because they have polystyrene capacitors; therefore, use isopropol alcohol. Use non-abrasive cloths with isopropol alcohol to clean the contacts. Do not use abrasives, such as erasers or fiberglass; they will remove the gold plating from the contacts.

5.4.2 Disassembly Techniques

All assemblies, except for the power supplies, can be unplugged after the top cover is removed. To remove the power supply remove the six screws and 8 terminal strip connectors as shown in Figure 2-8 in the "Installation" chapter. Note that if the power supply needs repair, the whole power supply unit should be replaced. Do not attempt to correct the power supply to the component level.

5.5 Troubleshooting Strategy

If it is suspected that the ANDS5400 system is defective, it is helpful to follow a prescribed sequence of checks to define the problem most rapidly. Categorize the problem in one of the following areas:

1) Performance Degradation:
   (Calibrate system)
2) Specific User Card Trouble
   (Replace card)
3) Interface Problem
   (Substitute new interface cards)
4) Expansion Chassis Trouble
   (Check the power supply in the expansion chassis; replace AC334; replace cables or user cards)
5) Digital Failure
   (Trace to front panel or AC333 or AC334; replace)
6) Analog Failure
   (Replace AC333, AC334, signal processor, or ADC)

To categorize the problem properly, follow the detailed testing sequence described in sections 5.5.1 through 5.5.7.

5.5.1 Power Supply

Verify that the straps to PWR RTN, SIG RTN, and CHASSIS RTN are in place on the rear panel of the master chassis. Using the chassis as a ground point, measure the +15V, −15V, and +5V supply voltages on the user card backplane with a digital voltmeter (DVM) and with the oscilloscope, looking for the rated DC voltages within 3% and observing less than 100mV of ripple. If the optional AN3500 supply is installed, be sure to measure these voltages on slots J7 and J16 on the user card backplane, thereby checking all six supply outputs.

5.5.2 Local Control

Disconnect the cables going to the computer, but leave the interface cards in the chassis of the ANDS5400 system. Energize the unit; the system should warm up in the "remote" mode. Put the system in "local" control by momentarily pressing the REMOTE/LOCAL pushbutton. If this step cannot be be performed, there is a problem with the REMOTE/LOCAL circuitry on the front panel or with the "run" line coming from the interface cards.

Once the system is in "local," try to load random range and address combinations into the range and address registers with the ANALOG button and the front panel switches.

Next, as described in the "Architectural Overview" chapter, use the DIGITAL and IN buttons with an address of 7000 to readback the front panel switches on the DATA display. Try many switch settings to fully exercise the switches, digital bus, and the display lites. If any problems are encountered during these tests, remove all the user cards and expansion chassis connections to the system, leaving only the expansion cards (J17 and J18) in the user card backplane, and try the test again. If problems are still encountered, remove the expansion cards, and try again. Finally, remove the ribbon cable connecting the user card backplane to the internal backplane, remove the A/D converter, and remove the signal processor card. At this point, the system should have only the front panel and the interfaces installed. Try once more to load ranges and addresses, and try to readback the digiswitches. If this cannot be performed, either the front panel or interface cards are at fault. The interface cards perform a limited function when the system is in "local" control, basically serving to hold their control lines at a static level. Place each one of the interface cards on extender cards in turn, and check that they hold their control lines at the proper level when the system is in "local" control (as noted in the "Interface" section of the "Drawings and Specifications" chapter).

5.5.3 A/D Converter

Place the A/D converter on the modified extender card. Plug the combined cards into C74, and connect the analog input to the variable voltage standard. During "local" control press the ANALOG button, and vary the voltage over the input range of the converter, looking for the current codes on the front panel DATA lites. (Note that the requirements for driving the A/D input are very demanding, and the voltage standard does not have the necessary high speed output characteristics, so do not expect great precision during this check.)

5.5.4 Signal Processor

Place the signal processor on a modified extender card so that its inputs can be connected to the variable voltage standard. Connect the signal return and the ODD inputs to analog ground, and connect the EVEN input to the positive output of the voltage standard. Connect the voltage standard return lead to analog ground on the extender board. In "local" control set the front panel switches to 100000, and press the ANALOG button. Vary the voltage over the range of the ADC, and check for the correct results on the front panel DATA display. These results should reflect the input voltage with a high degree of accuracy. If the signal processor has programmable gain, vary the range register settings and voltage standard settings to exercise all the gains.

5.5.5 User Card Bus

Install an analog input card in any slot in the master chassis. Connect the voltage standard to the card's differential inputs with the low input and the voltage standard negative output tied to ground and the high input tied to the positive output of the standard.

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Address the card and channel, and verify that the ANDS5400 front panel data results reflect the voltage being applied. (e.g. for an AC4720 card installed in slot J3 use range and address code 100100). If problems occur, there may be a digital or analog fault. To eliminate the digital fault, observe pins A, B, C, and D on the connector into which the user card is plugged. All four of these address bus pins must be at a logical "1" to address the card. Observe pins 1, 2, 3, and 4 on the same connector. These pins select the channel on the card, and for the first channel these pins would all be low. Measure the voltages on the analog bus (pins 21 and Y) on the user card connector. The ODD bus should be at ground since the low input is tied to ground, and the EVEN bus should follow the voltage set on the standard.

If the proper voltages are present on the user card bus but are not present on the input to the signal processor, check the AC333 circuitry using the "Expansion Cards" section of the "Drawings and Specifications" chapter as a guide.

Digital checks are best performed using a write/read digital card like the DC6510. Install the card in any master chassis slot, address the card, and write a pattern on it; then read it back to verify the integrity of the data. Use patterns of all zeros, all ones, and alternating ones and zeros. If any problems are noted, check the address lines on the user card bus then the data lines. Both data and address bits are held statically on the bus until a button is pressed, thus simplifying the troubleshooting task.

If no problems are noted during the analog or digital checks on the user card bus, yet the fully installed system exhibits problems, there may be a faulty user card that loads down one of the address, data, or analog lines. To check for this, repeat the tests with all of the user cards installed. Remove user cards one at a time until the problem card is isolated. All digital levels on the user card bus are driven from CMOS devices and should thus have logic levels very close to ground and +5 volts. Any level higher that 0.5 volt and lower than 4.5 volts is indicative of a problem.

5.5.6 Expansion Chassis

The same user card bus checks can be performed in any expansion chassis using the appropriate addresses. Be sure to check the master chassis thoroughly before proceeding to the expansion chassis since all signals originate in the master chassis. The AC334 card is the heart of the expansion chassis and is thus the most likely problem source.

5.5.7 Interface

The ANDS5400 computer interface is checked in "remote" control by performing simple exercises like those outlined in section 5.5.5. Customers with DEC DMA interfaces for the PDP-11 or the LSI-11 can take advantage of Analogic's extensive interface diagnostic package to simplify the testing and troubleshooting task. These diagnostics exercise the interface in a logical section-by-section approach that can define problems in a minimum of time. Any other interface must be tested by the user with small user-written programs.

5.6 Spares Recommendation

A 10% spares set is recommended: for example, if there are ten or fewer of one type of user card, one spare is needed; if 11 to 20 of one type are used, then two spares are needed, and so forth.

With the following configuration:

ANDS5400-B-B-23A
1 AC260
1 AC27122D
5 AC4720
11 AC15622D

use this set of spares:

1 AN3007 (Power Supply)
1 AC470 (Interface)
1 AC471 (Interface)
1 AC260
1 AC27122D
1 AC333
1 AC4720
2 AC15622D

The size of this set of spares is typical regardless of the size of the configuration. This strategy provides a minimum MTTR (Mean Time To Repair) since the customer has the cards to repair the system. With a qualified technician the MTTR is usually less than one hour.

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6
SOFTWARE SUPPORT

6.0 General

Analogic offers a variety of software support packages for PDP-11 and LSI-11 users that aide in system installation, calibration, troubleshooting, performance verification, and writing application software. The packages listed below are complete stand-alone programs for PDP-11 or LSI-11 users in RT-11 compatible media.

6.0.1 Interface Diagnostic Program

This code and program, using simple commands and including CSR, interrupt, DMA, and PIO tests, provides an easy method to verify the proper performance of the computer interface.

6.0.2 Self-Test Card Program

This software package operates in conjunction with the AC3000 Self-Test Card to provide complete analog and digital testing of the ANDS5400 structure, including the printing of a performance data sheet. It is also useful for system alignment.

6.0.3 General Purpose Exerciser Program

The Exerciser Program allows the user to manipulate and read all ports (analog and digital) of any system installation. All command entries are in easy to use formats and are entered from the console keyboard with optional hardcopy capability. The program supports the user card interrupt structure and prints octal, decimal, or analog voltage results on command. This program is an excellent tool for installation debugging and allows rapid checks for noise, bad connections, and overall system status.

6.1 Driver Package for Custom Application Programming

The programs listed below are driver packages that simplify custom application programming by providing a standard software path for all hardware communication. All interface functions are supported, including DMA, user card interrupts, and master registers.

6.1.1 Assembly Language Driver

This complete, fully documented and commented driver package can be linked with a user written assembly language program to simplify and standardize hardware communication. This driver is used by the Exerciser package described in section 6.0.3.

6.1.2 ANALIB FORTRAN Library

This assembly language library can be linked with user written RT-11 FORTRAN programs to provide access to all ANDS5400 system capabilities and is fully documented and commented. This program is available only with the FOCUS 5000 System.

6.2 Diagnostic Programs

The Bridge Completion (Strain Gauge) Card Diagnostic, Frequency Counter Diagnostic, D/A Converter Diagnostic, and Contact Closure Diagnostic are complete diagnostic and test programs written for specific user cards. They provide the OEM user with the same extensive testing capability used by the Analogic test group and require a minimum of additional hardware. All programs produce printed records of test results and are supplied on RT-11 compatible media.

Analogic is continually creating additional software support programs for PDP-11 and LSI-11 users to enhance system capability and simplify application programming. For the latest information about Analogic's new offerings contact the Sales Department (the telephone number is listed in the address block at the end of the "Table of Contents").

6.3 "SL" Software Packages for LSI-11 Based Systems

The following software packages are available on single or double density DEC compatible floppy disc media from Analogic and provide a variety of capabilities aimed at making the user's task of system installation, performance verification, and software development easier and more efficient.

6.3.1 SL001 Self-Test Card Program

This software package operates in conjuncton with the AC3000 Self-Test Card to provide complete analog and digital testing of the ANDS5400 structure, including the printing of a performance data sheet. Also useful for system alignment, this unique program is available only through Analogic and provides the only truly dynamic data acquisition system self-test capability on the market. This program is provided only in object code and requires the – 18 Interface, LSI-11/2 System, AC3000 Self-Test Card, and RT-11.

6.3.2 SL002 Interface (– 18) Diagnostic

This Analogic program is a complete diagnostic for the – 18 interface for the LSI-11/2, and it includes operating instructions and program source listing. It requires the – 18 Interface, LSI-11/2 System, and RT-11.

6.3.3 SL005 DEC Fortran IV

This highly optimized and extended version of this mature language creates efficient machine code during compilation, allowing for high speed operation yet maintaining the simplicity of a high-level language. It requires an LSI-11 based system and an RT-11.

6.3.4 SL007 DEC RT-11

This single-user, disk-based real-time operating system from Digital Equipment Corporation has been designed

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for both program development and on-line applications use. It includes an interactive video editor, MACRO assembler, linker, and many other utilities for file and disc manipulation. RT-11 supports the generation and operation of FORTRAN programs as well as foreground/background operation for multiple program operation. It requires an LSI-11/2 based system.

6.3.5 SL010 – 18 Interface Driver

This is an Analogic program that greatly simplifies software development at the assembly language level for the LSI-11/2 DMA Interface. It is provided with a complete source listing and can be linked with any user written assembly language program since it is not dependent on the operating system. It is provided on an RT-11 format disc and requires a – 18 Interface, an LSI-11/2 System, and RT-11.

6.3.6 SL013 DAC Diagnostic and Test Program

This Analogic assembly language program was developed for the purpose of testing and calibrating D/A converters and is provided with a complete source listing. It requires a – 18 Interface, an LSI-11/2 based system, RT-11, Data Precision 3500 DVM, DC6510 and DC6000 Digital I/O Cards, and some external cabling.

6.3.7 SL014 Frequency Counter Diagnostic and Test Program

This is an Analogic assembly language program developed for the purpose of testing and exercising the DC63XX Card. This program is useful in developing efficient software to control and operate this complex I/O device and is provided with a complete source listing. It requires a – 18 Interface, an LSI-11/2 based system, RT-11, DC6300, and some external cabling.

6.3.8 SL015 Change-of-State (COS) Diagnostic and Test Program

This is an Analogic assembly language program developed for the purpose of testing and exercising the DC62XX Card. This program is useful in developing efficient software to control and operate the DC62XX change-of-state input card, is provided with a complete source listing, and requires a – 18 Interface, an LSI-11/2 based system, RT-11, DC6510, and some external cabling.

6.3.9 SL016 Bridge Completion (Strain Gauge) Card Diagnostic and Test Program

This is an Analogic assembly language program developed for the purpose of testing and calibrating the AC43XX Card. This program is useful in developing efficient software to control and operate this complex input device and is provided with a complete source listing. It requires a – 18 Interface, an LSI-11/2 based system, RT-11, and a precision D/A converter (AC1916), and some external cabling.

6.3.9 SL018 General Purpose Exerciser

The Exerciser program allows the user to manipulate and read all the ports (analog and digital) of any system installation. All command entries are in easy to use formats and are entered from the console keyboard with optional hardcopy capability. The program supports the user card interrupt structure and prints octal, decimal, or analog voltage results on command. This program is an excellent tool for installation debugging and allows rapid checks for noise, bad connections, and overall system status. It requires a – 18 Interface and an LSI-11/2 based system.

Note: The LSI-11/2 DMA Interface (– 18) is provided with SL002 and SL018. If the complete source listing of the driver program is required, the user must purchase SL010.

6.4 "SP" Software Packages for PDP-11 Based Systems

The following software packages are available on single or double density DEC compatible floppy disc media from Analogic and provide a variety of capabilities aimed at making the user's task of system installation, performance verification, and software development easier and more efficient.

6.4.1 SP001 Self-Test Program

This software package operates in conjuncton with the AC3000 Self-Test Card to provide complete analog and digital testing of the ANDS5400 structure including the printing of a performance data sheet. Also useful for system alignment, this unique program is available only through Analogic and provides the only truly dynamic data acquisition system self-test capability on the market. This program is provided only in object code and requires the – 31 Interface, PDP-11 Unibus based system, AC3000 Self-Test Card, and RT-11.

6.4.2 SP002 – 31 Interface Diagnostic

This Analogic program is a complete diagnostic for the – 31 interface for the PDP-11 Unibus based systems, and it includes operating instructions and program source listing. It requires the – 31 Interface, PDP-11 Unibus based system, and RT-11.

6.4.3 SP010 – 31 Interface Driver

This is an Analogic program which can greatly simplify software development at the assembly language level for the PDP-11 Unibus based systems and is provided with a complete source listing. This driver can be linked with any user written assembly language program since it is not dependent on the operating system. It is provided on RT-11 format disc and requires the – 31 Interface, PDP-11 Unibus based system, and RT-11.

6.4.4 SP013 DAC Diagnostic and Test Program

This is an Analogic assembly language program developed for the purpose of testing and calibrating D/A converters. It is provided with a complete source listing. It requires a – 31 Interface, a PDP-11 Unibus based system, RT-11, Data Precision 3500 DVM, DC6500 and DC6000 Digital I/O Cards, and some external cabling.

6.4.5 SP014 Frequency Counter Diagnostic and Test Program

This is an Analogic assembly language program developed for the purpose of testing and exercising the DC63XX Card. This program is useful in developing efficient software to control and operate this complex I/O device and is provided with a complete source listing. It requires a – 31 Interface, a PDP-11 Unibus based system, RT-11, a DC6300, and some external cabling.

6.4.6 SP015 Change-of-State (COS) Diagnostic and Test Program

This is an Analogic assembly language program developed for the purpose of testing and exercising the DC62XX Card. This program is useful in developing efficient software to control and operate the DC62XX change-of-state input card. It is provided with a complete source listing and requires a – 31 Interface, a PDP-11 Unibus based system, RT-11, a precision D/A converter (AC1916), and some external cabling.

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6.4.7 SP016 Bridge Completion (Strain Gauge) Card Diagnostic and Test Program

This is an Analogic assembly language program developed for the purpose of testing and calibrating the AC43XX Card. This program is useful in developing efficient software to control and operate this complex input device and is provided with a complete source listing. It requires a −31 Interface, a PDP-11 Unibus based system, RT-11, a precision D/A converter (AC1916), and some external cabling.

6.4.8 SP018 General Purpose Exerciser

The Exerciser program allows the user to manipulate and read all the ports (analog and digital) of any system installation. All command entries are in easy to use formats and are entered from the console keyboard with optional hardcopy capability. The program supports the user card interrupt structure and prints octal, decimal, or analog voltage results on command. This is an excellent tool for installation debugging and allows rapid checks for noise, bad connections, and overall system status. It requires a −31 interface, a PDP-11/ Unibus based system, and RT-11.

Note: The PDP-11 DMA Interface is provided with SP002 and SP018. If the complete source listing for the driver program (SP010) is required, it must be purchased by the user.

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7
DRAWINGS AND SPECIFICATIONS

7.0 General

The "Drawings and Specifications" chapter, containing a comprehensive collection of descriptions, slot connections, mechanical drawings, system schematics, specifications, and data sheets of the ANDS5400 component parts, is conveniently divided into the following sections: "Mechanical," "Cables," "Internal Backplane," "Interfaces," "Signal Processors — ADC," "Front Panel Display and Control," "User Card Backplane," "Expansion Cards," and "Power Supplies." This chapter provides the appropriate information to install, operate, and, if necessary, to troubleshoot the ANDS5400. Each section of this chapter contains an index of the data sheets, drawings, and schematics in that section.

The "Mechanical" section includes the mechanical drawings of not only the master chassis and expansion chassis, but also the internal backplane, internal backplane extender board, and other components. The power supply charts, schematics, and a wiring table of the internal backplane appear in the "Internal Backplane" section.

The "Interface" section provides a general description of the slot connections, data sheets, schematics, cable assemblies, and assembly drawings for the various ANDS5400 computer interfaces. The next section of this chapter includes the slot connections, data sheets, and schematics for the signal processor and A/D converter.

The "Front Panel Display and Control" section explains the selection of the analog or digital input modes, "local" or "remote" control, and the "dynamic" mode of operation. An important feature of this section is an explanation of the addressing system.

The slot connections, assembly drawings, schematics, and a wiring table of the user card backplane for the master card expansion chassis appear in the next section.

The "Expansion Cards" section provides an in-depth description of the sequence of signals involved in the operation of the expansion cards and includes the appropriate schematics. The final section contains the schematics and data sheets for the AN3007 power supply.

Refer to Book Two for the schematics, descriptions, specifications, and the theory of operations of the individual user cards.

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Section 7.1
Mechanical Assembly Drawings

Card Number	Drawing Number	Title
—	C7-2369 (2 sheets)	Master Chassis Top Assembly
—	C3-1503	Outline ANDS5400 System
AC70	D7-7450	User Card Extender Board Assembly
AC71	D7-7451	Internal Backplane Extender Board Assembly
AC72	D7-7455	ADC Chain Custom Card Assembly
AC73	D7-8606	Custom User Board Assembly
AC80	C7-1539	User Card Interface Connector Assembly
AC81	C7-1596	Thermoplexer Interface Connector Assembly

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
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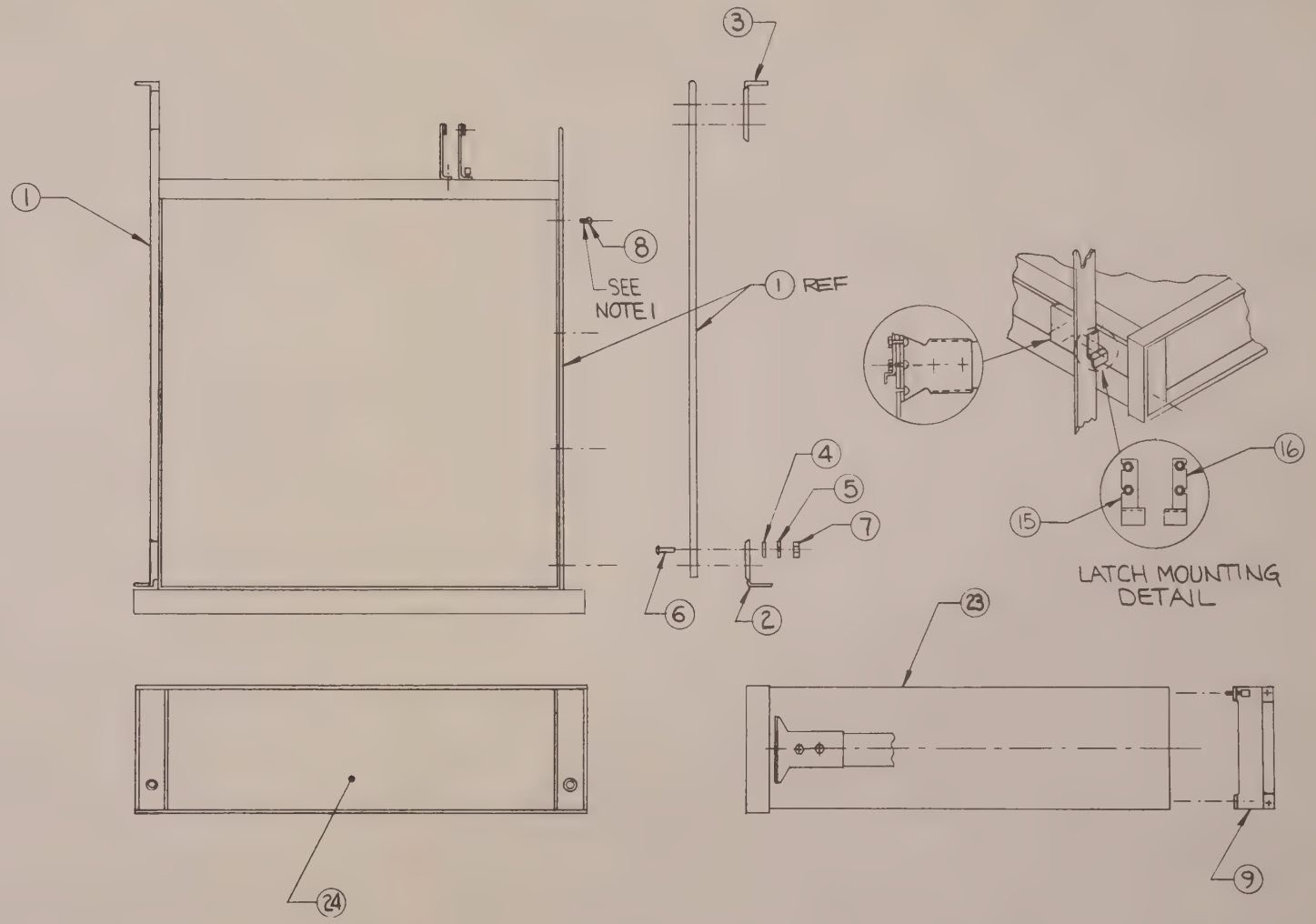
SIZE C | 7-2369 | REV 1



NOTES

1. RECOMMEND USE OF A THREAD SEALING COMPOUND
2. ITEMS 2,3,4,5,6,7,8,12,15 & 16 ARE SHIPPED IN A PLASTIC BAG, (ITEM 18) WITHIN A SECURELY TAPED MANILA MAILING ENVELOP INSIDE THE INNER BOX, SEE SHEET 2.

PLIO-3800	ANDS 5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± ANGLES .XXX ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	[illegible]	22NOV78
CHECKED	[illegible]	6DEC78
ENGINEER	J. Muller	4-5-79
ENGINEERING MGR.	[illegible]	4-5-79
QUALITY CONTROL		
PRODUCTION		
WEIGHT		

ANALOGIC. WAKEFIELD, MASS. 01880

TOP ASSEMBLY
(ANDS 5400)

CODE IDENT NO	SIZE		REV
31814	C	7-2369	1
SCALE NONE		SHEET 1 OF 2	

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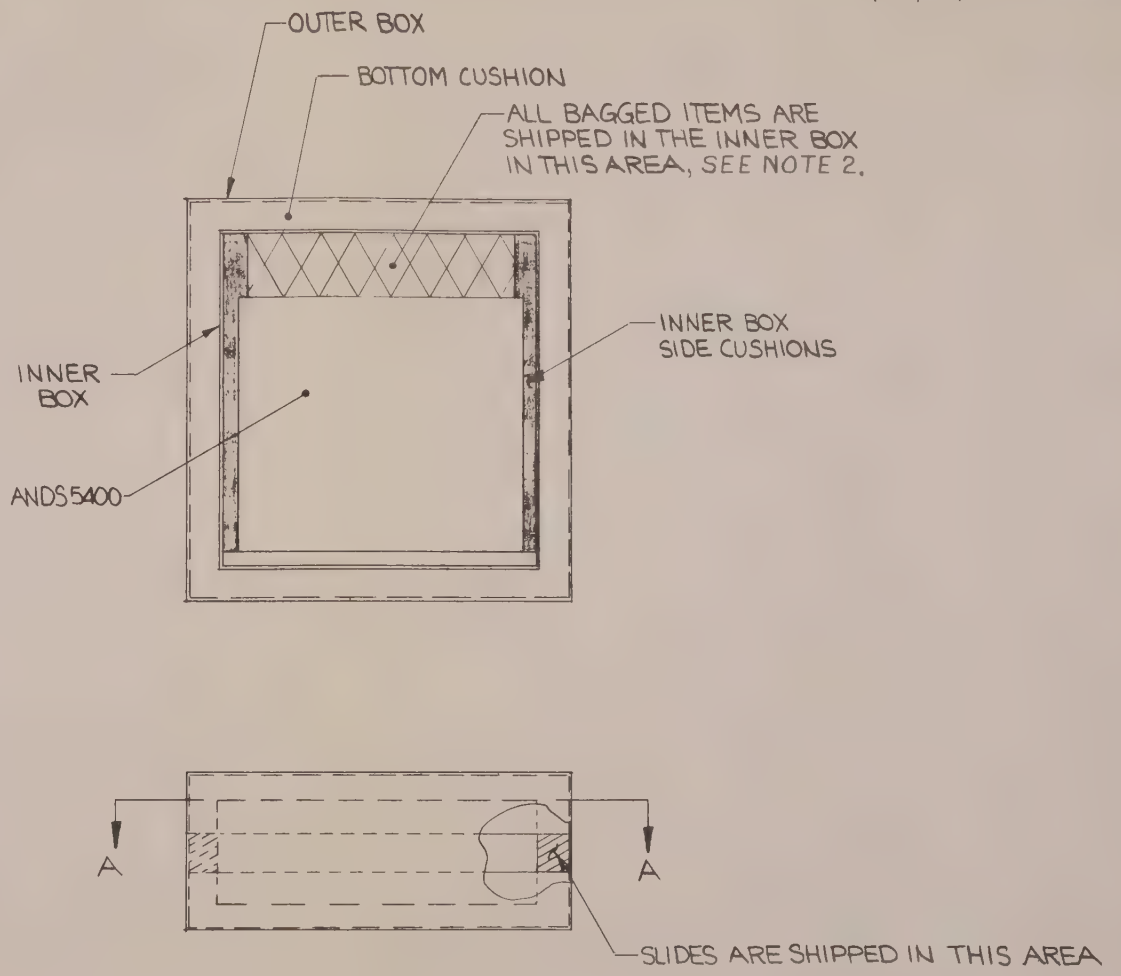
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C | 7-2369 | REV 1



HARDWARE SHIPPING LOCATIONS

PL10-3800	ANDS 5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± .XX ± .XXX ±
ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	R S Buntin	3DEC78
CHECKED		6DEC78
ENGINEER	L. Mullin	4-5-79
ENGINEERING MGR.	R W Thomas	4-5-79
QUALITY CONTROL		
PRODUCTION		
WEIGHT		

ANALOGIC. WAKEFIELD, MASS. 01880

TOP ASSEMBLY (ANDS5400)

CODE IDENT NO	SIZE		REV
31814	C	7-2369	1
SCALE NONE		SHEET 2 OF 2	

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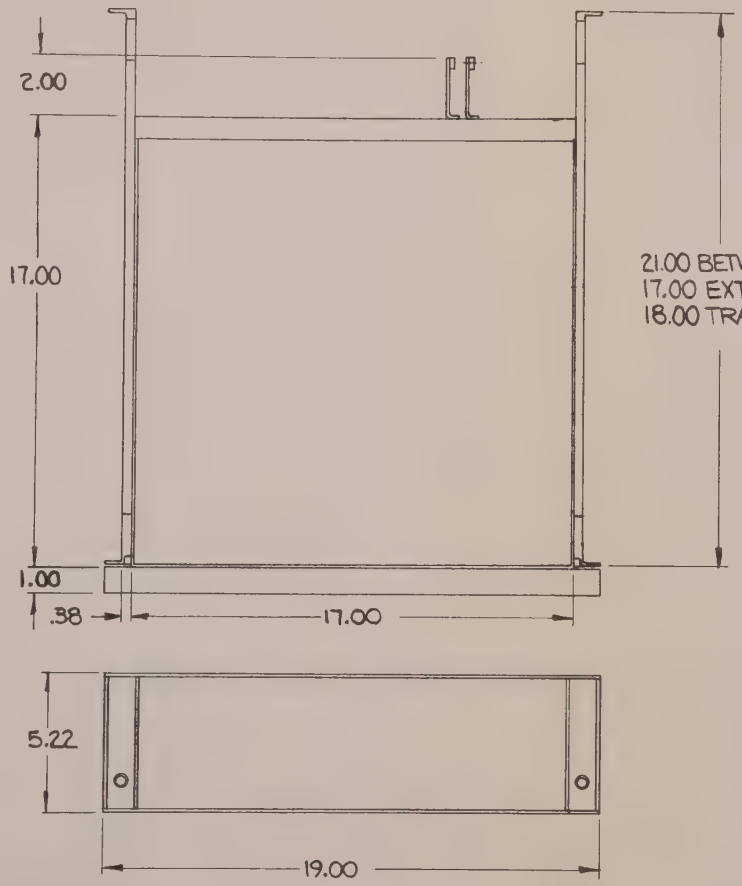
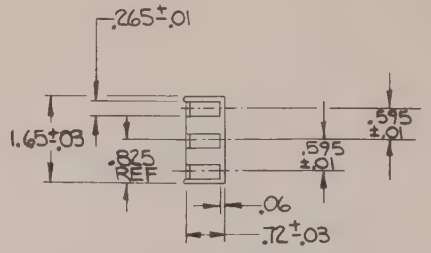
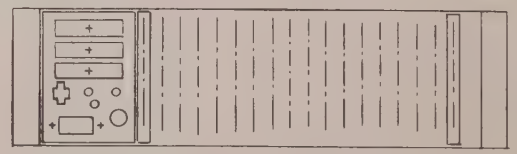
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C | 3-1503 | REV 0

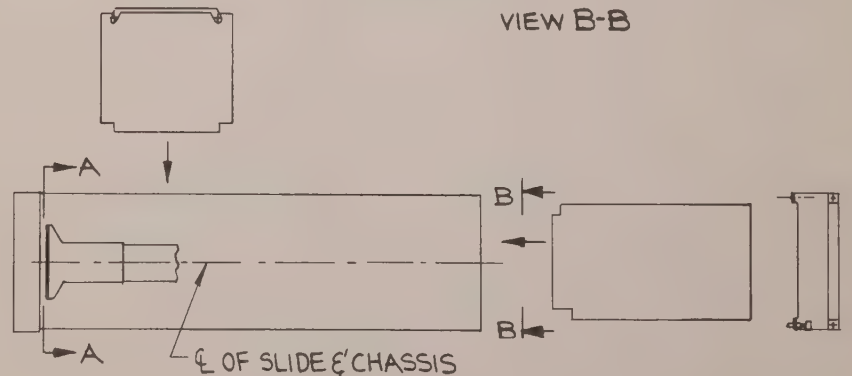




SECTION A-A



VIEW B-B



PLIO-3806	AND5 5450
PLIO-3800	AND5 5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± .XXX ±
ANGLES ±

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

		DATE
DRAWN	Ruby Lantin	22 NOV 78
CHECKED	[illegible]	6 DEC 78
ENGINEER	T. Mullen	4-5-79
ENGINEERING MGR.	[illegible]	4-5-79
QUALITY CONTROL		
PRODUCTION		
WEIGHT		

ANALOGIC, WAKEFIELD, MASS. 01880

OUTLINE ANDS 5400 SYSTEM

CODE IDENT NO	SIZE		REV
31814	C	3-1503	0

SCALE NONE SHEET 1 OF 1

D L M INC.

REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPLS	DATE	
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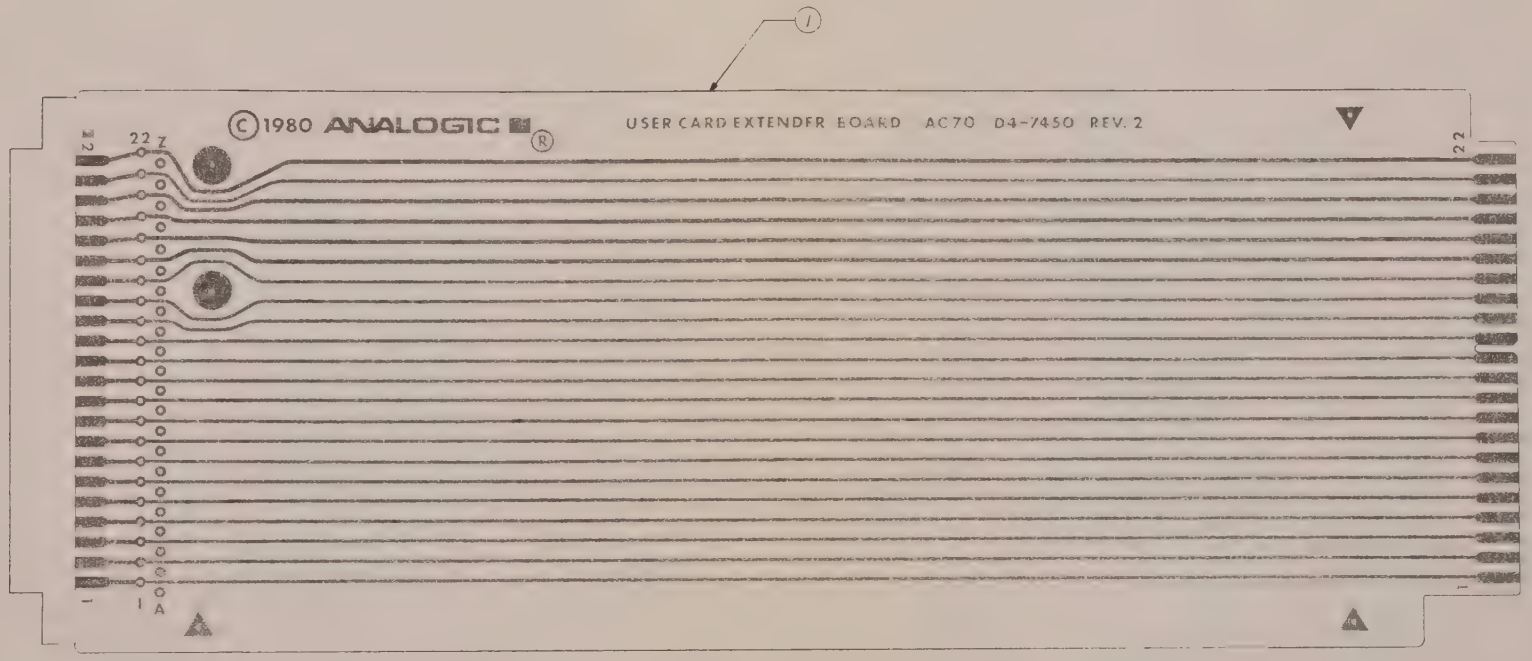
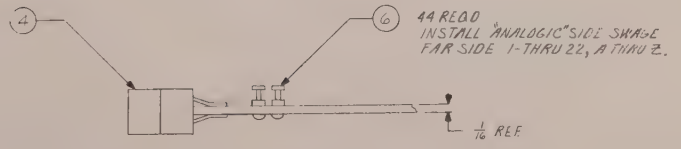
D 7-7450 REV 2



COMPONENT SIDE



NOTES:
1. ASSEMBLE IN ACCORDANCE WITH A2-1027.

PL10-7450	AC 70				
NEXT ASSY	USED ON				
APPLICATION					

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		DATE
DRAWN	B Ross	3-5-76
CHECKED	[illegible]	8/17/76
DESIGNER	[illegible]	8-17-76
ENGINEER	E. DINOWITZ	8-19-76
APPROVED	R.F. POWELL	8-19-76
RELEASED	R PEAKE	8-19-76
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

ASSEMBLY
USER CARD EXTENDER BOARD
AC 70

CODE IDENT NO.	SIZE		REV
31814	D	7-7450	2
SCALE 2:1	ACCOUNT NO.		SHEET 1 of 1

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REVISIONS					
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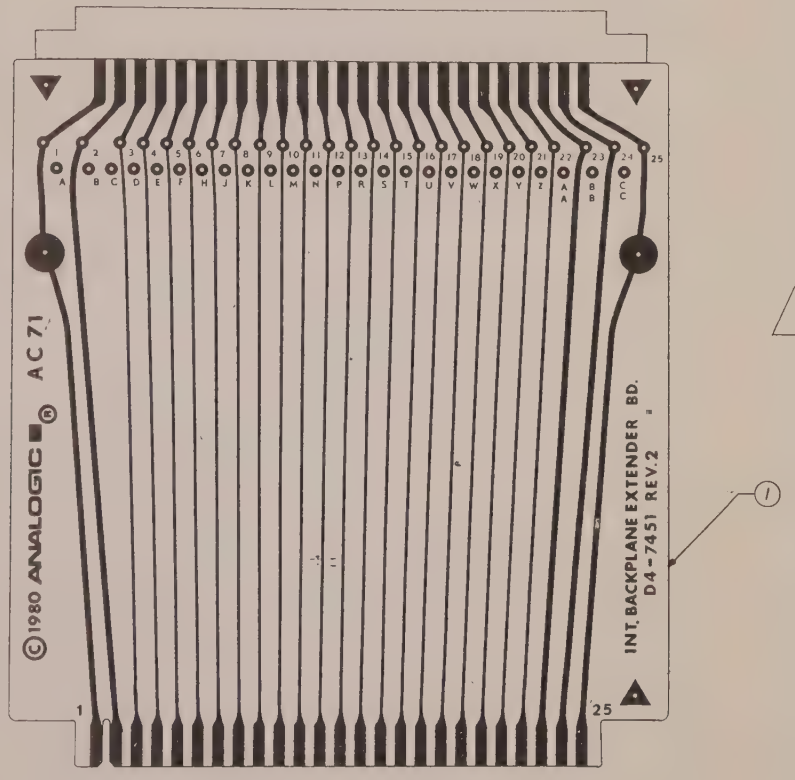
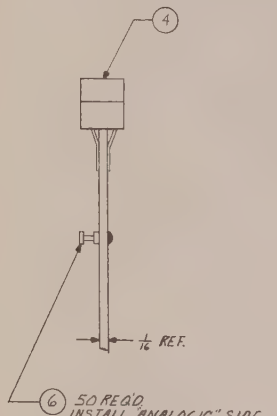
D 7-7451 REV 2





1

NOTES:
1. ASSEMBLE IN ACCORDANCE WITH A2-1027.

COMPONENT SIDE

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN K. Stenger		11-6-75
CHECKED R. Cellucci		11-14-75
DESIGNER E. Winkler		8-17-76
ENGINEER E. DINAWITZ		8-19-76
APPROVED R.F. POWELL		8-19-76
RELEASED R. PEARE		8-19-76
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

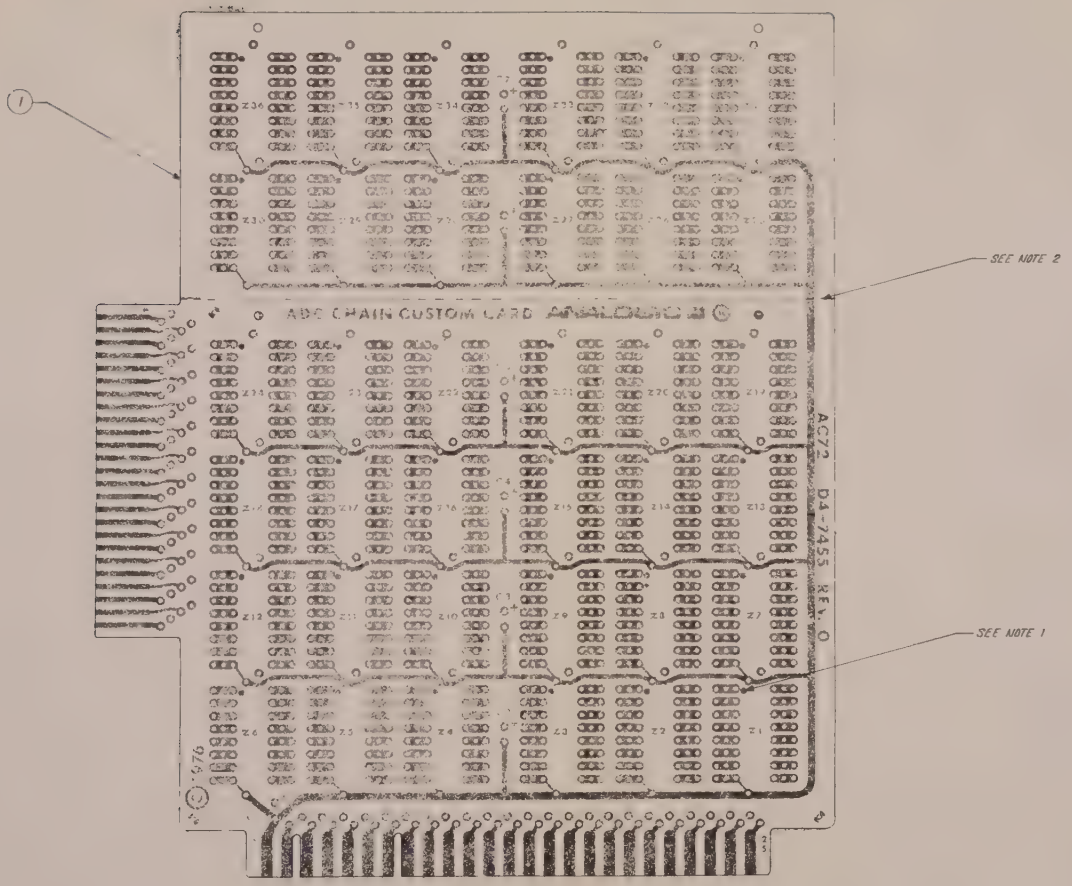
ASSEMBLY
INTERNAL BACKPLANE EXTENDER BD.
AC 71

PL10-7451	AC 71
NEXT ASSY	USED ON
APPLICATION	

CAGE IDENT NO 31814 | SIZE D | DWG NO 7-7451 | REV 2
SCALE 2:1 | ACCOUNT NO | SHEET 1 OF 1

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

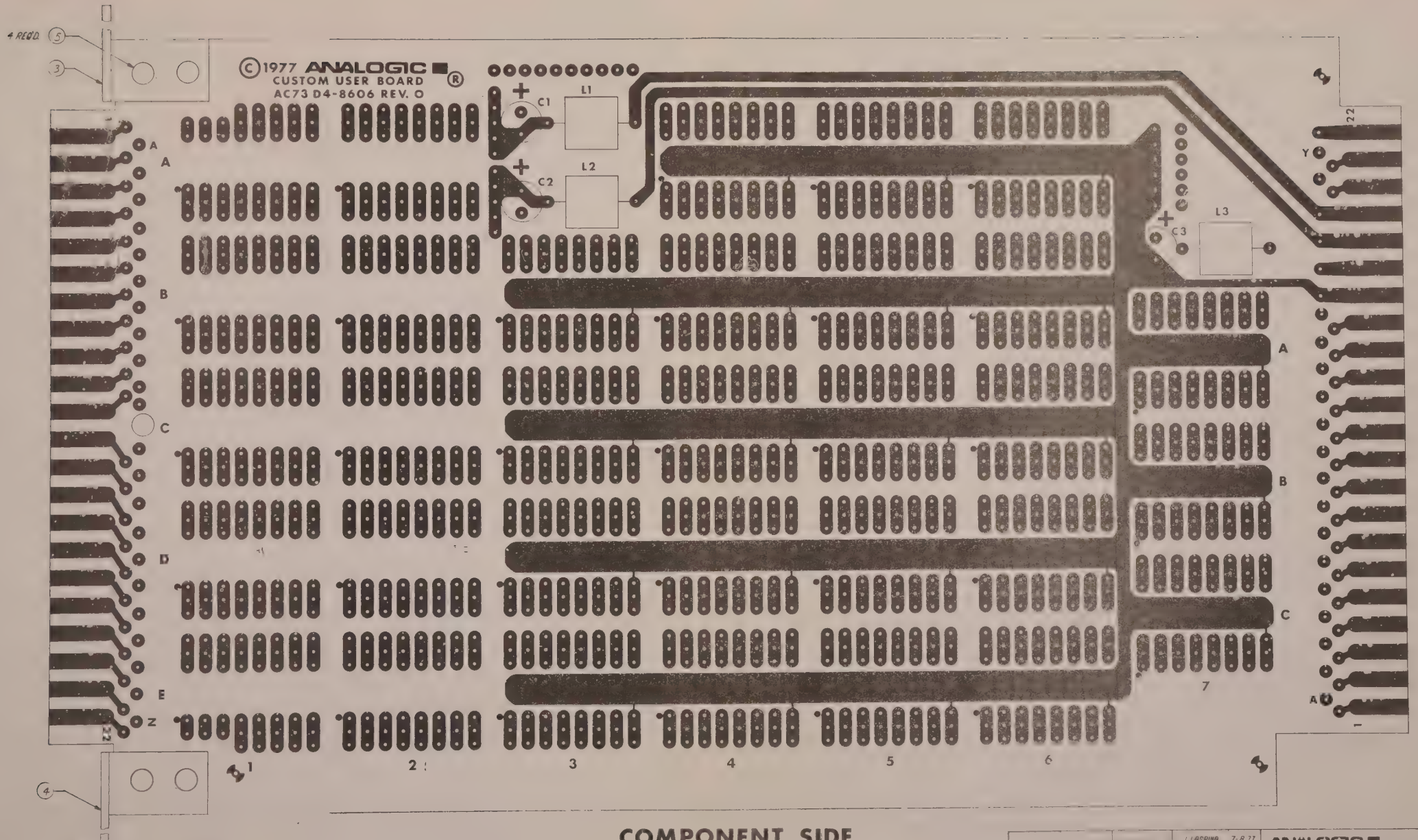
SIZE D 7-7455 REV. 0 △



NOTES:
1. DOT INDICATES PIN 1 OF INTEGRATED CIRCUIT.
2. CUT BOARD FROM NOTCH TO NOTCH AS SHOWN WHEN USING 24 OR LESS I.C.'s.
3. ASSEMBLE IN ACCORDANCE WITH A2-1027.

COMPONENT SIDE

SALES ORDER	AC72	B. ROSS 2-2-76	ANALOGIC NAKEFIELD, MASS. 01880
NEXT ASSY	USED ON	APPROVED	ASSEMBLY ADC CHAIN CUSTOM CARD AC72
APPLICATION		RELEASED	CODE IDENT NO. 31814 SIZE D 7-7455 REV 0
		WEIGHT	SCALE 2:1 ACCOUNT NO SHEET 1 OF 1



COMPONENT SIDE

NOTES:
1. ASSEMBLE IN ACCORDANCE WITH A2-1027.
2. DOT INDICATES PIN 1 OF I.C.'S.
3. HAND SOLDER ONLY. DO NOT WAVE SOLDER.

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PLID-8606 AC73

J. LASPINA 7-8-77

ANALOGIC

ASSEMBLY
CUSTOM USER BOARD
AC73

31814 D 7-8606 REV O

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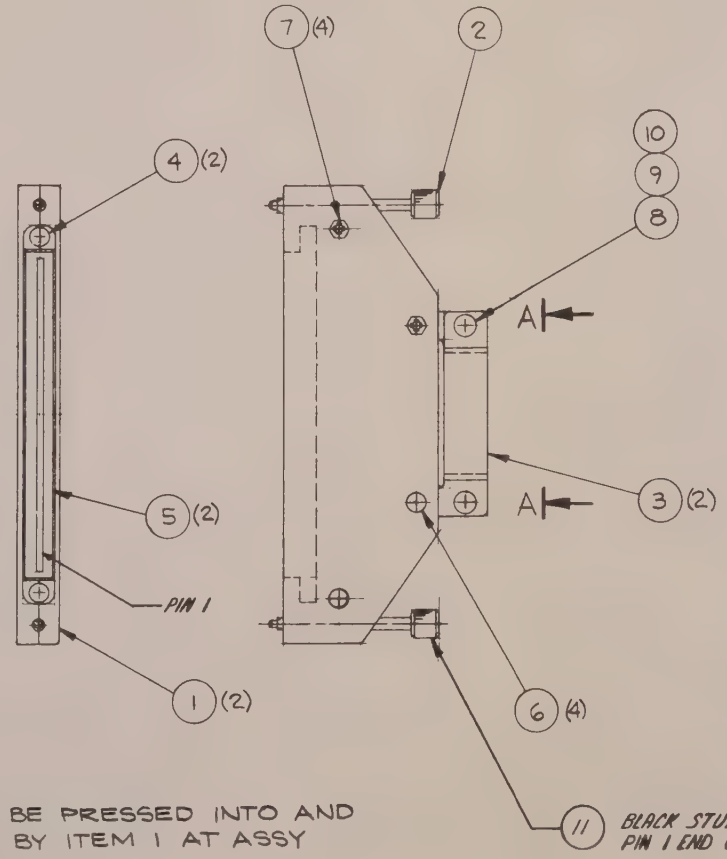
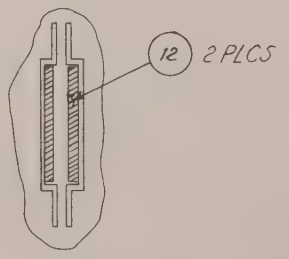
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR	DATE
1	4087	SEE E.C.O.	J.L.	[illegible]	8-7-77
2	4-0172	ADD "AC 80" TO TITLE BLOCK	J.L.	[illegible]	1-23-78
J	4-0286	SEE ECO	[illegible]	[illegible]	2/17/78

SIZE C | 7-1539 | REV 3





VIEW A-A

NOTES
1. ITEM 7 WILL BE PRESSED INTO AND CAPTIVATED BY ITEM 1 AT ASSY USING ITEM 6

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-2039	AN5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	R. Sussin	30 JAN 76
CHECKED	RET	6 AUG 76
DESIGNER	R. Sussin	30 JAN 76
ENGINEER	RW Hamm	8-6-76
APPROVED	[illegible]	9/9/76
RELEASED	[illegible]	[illegible]
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CONNECTOR ASSY
AC 80 (USER CARD INTERFACE)

CODE IDENT NO	SIZE		REV
31814	C	7-1539	3
SCALE 1/1	ACCOUNT NO.	SHEET 1 OF 1	

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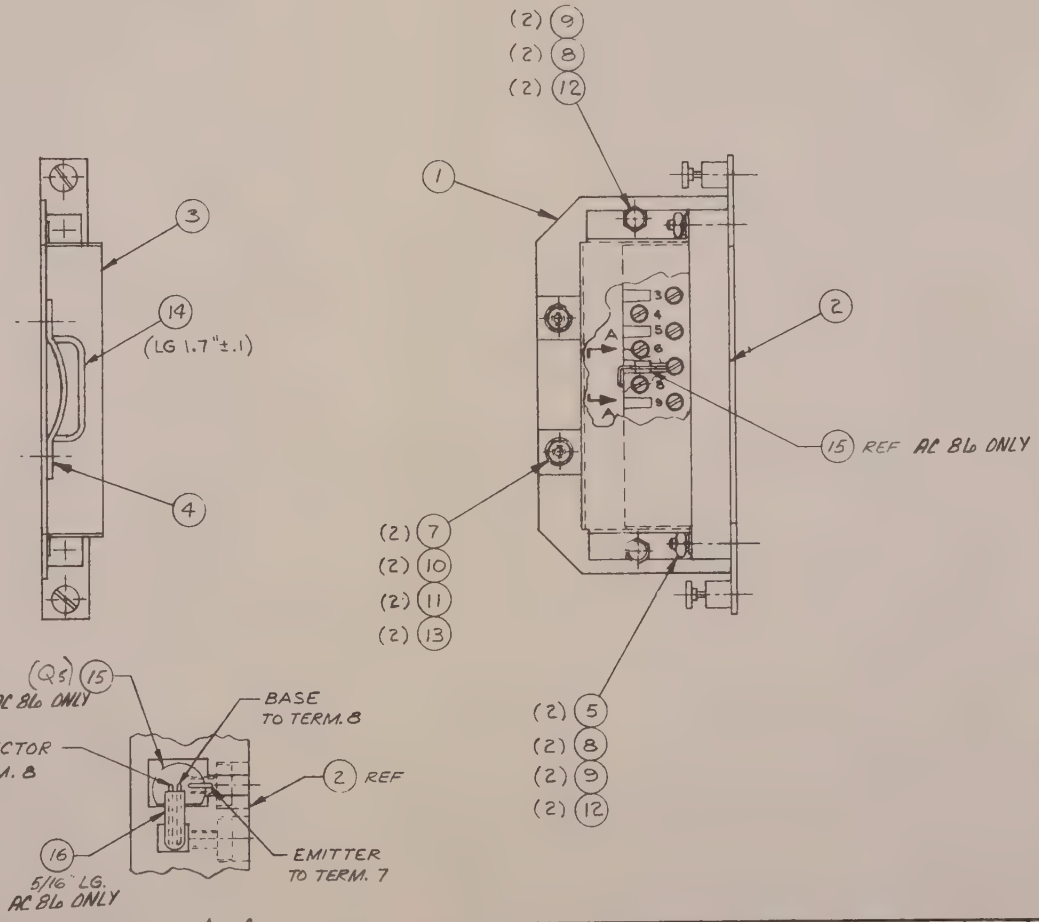
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1		VIEW A-A ADDED TO SHOW TRANSISTOR LOCATION	[illegible]		6 24 77
2	4-0172	ADD "AC85 AC86" TO TITLE BLOCK ADD "AC86 ONLY" TO ITEMS 15,16	JL	[illegible]	1-23-78
3	4-49	SEE ECO	[illegible]	[illegible]	[illegible]

SIZE C | 7-1596 | REV 3



VIEW A-A
SCALE: NONE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± XX ± ANGLES XXX ±

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

DRAWN	N. Carter 8-11-77
CHECKED	R. Swain 24MAY77
ENGINEER	[illegible]
ENGINEERING MGR.	[illegible]
QUALITY CONTROL	[illegible]
PRODUCTION	[illegible]
WEIGHT	

ANALOGIC WAKEFIELD, MASS. 01880

CONNECTOR ASSY
[illegible] AC85/AC86
(15 CONTACT)

CODE IDENT NO	31814
SIZE	C
	7-1596
REV	3
SCALE	1/1
SHEET	1 OF 1

P.I.C. 2171	AC 4250→56
NEXT ASSY	USED ON
APPLICATION	

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Section 7.2
Cable Assemblies

Card Number	Drawing Number	Title
—	C7-2363	W3 Cable Assembly
—	C7-2358	W4 Cable Assembly
—	C7-2359	W5 Cable Assembly
—	C7-2365	W8 Cable Assembly
—	C7-2366	W9 Cable Assembly
—	C7-2360	W10 Cable Assembly
—	C7-2376	ANDS5400 Analog Expansion Cable Assembly
—	C7-2377	ANDS5400 Digital Expansion Cable Assembly

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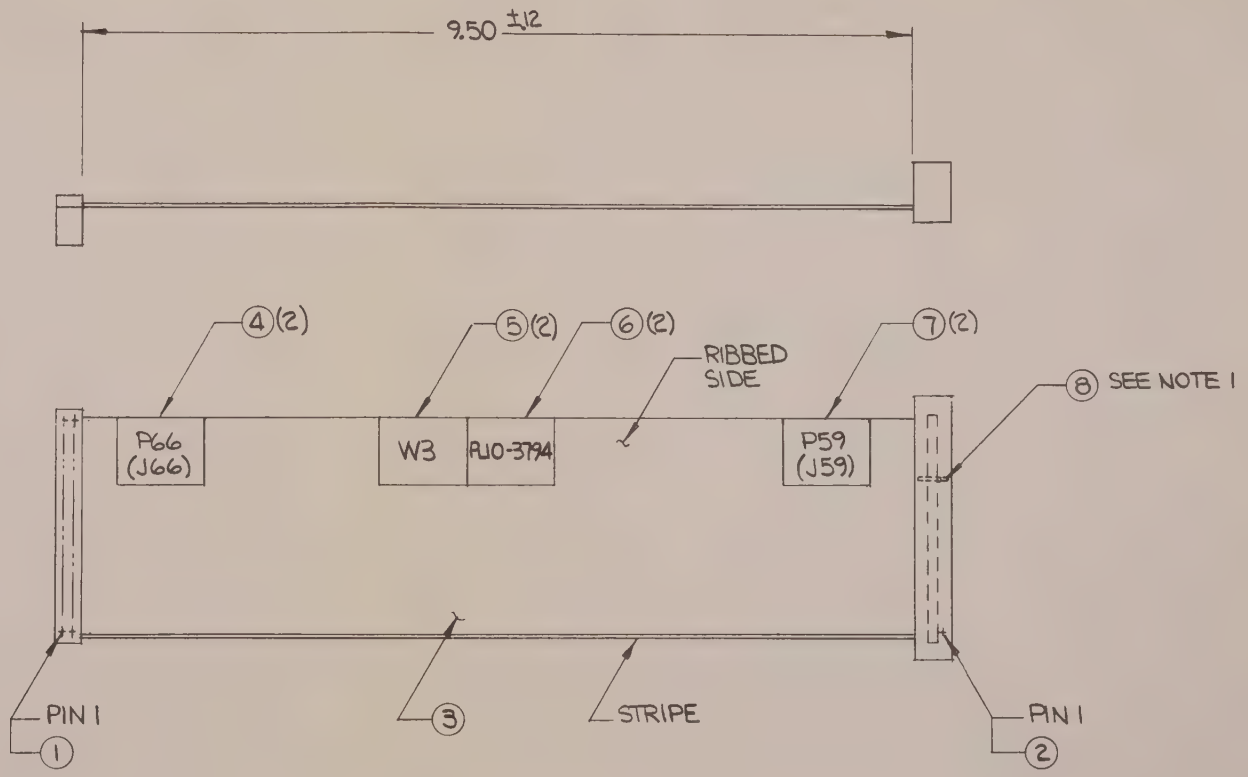
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C 7-2363 REV O



NOTES:

1. INSTALL ITEM 8 IN ITEM 2 BETWEEN POS. 36 & 38.

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .X ± .XX ± .XXX ± ANGLES ±	DRAWN R. Curtin	DATE 7DEC78	ANALOGIC. WAKEFIELD, MASS. 01880
			CHECKED R. Curtin	7DEC78	
		MATERIAL	ENGINEER L. Mullen	4-5-79	CABLE ASSEMBLY (W3)
		FINISH	ENGINEERING MGR. T. Wilson	4-5-79	
			QUALITY CONTROL		
PLO-3794	AND35400	APPLICABLE SPECIFICATIONS	PRODUCTION		CODE IDENT NO 31814 / SIZE C / 7-2363 / REV O
NEXT ASSY	USED ON		WEIGHT		SCALE 1/1 / SHEET / OF
APPLICATION					

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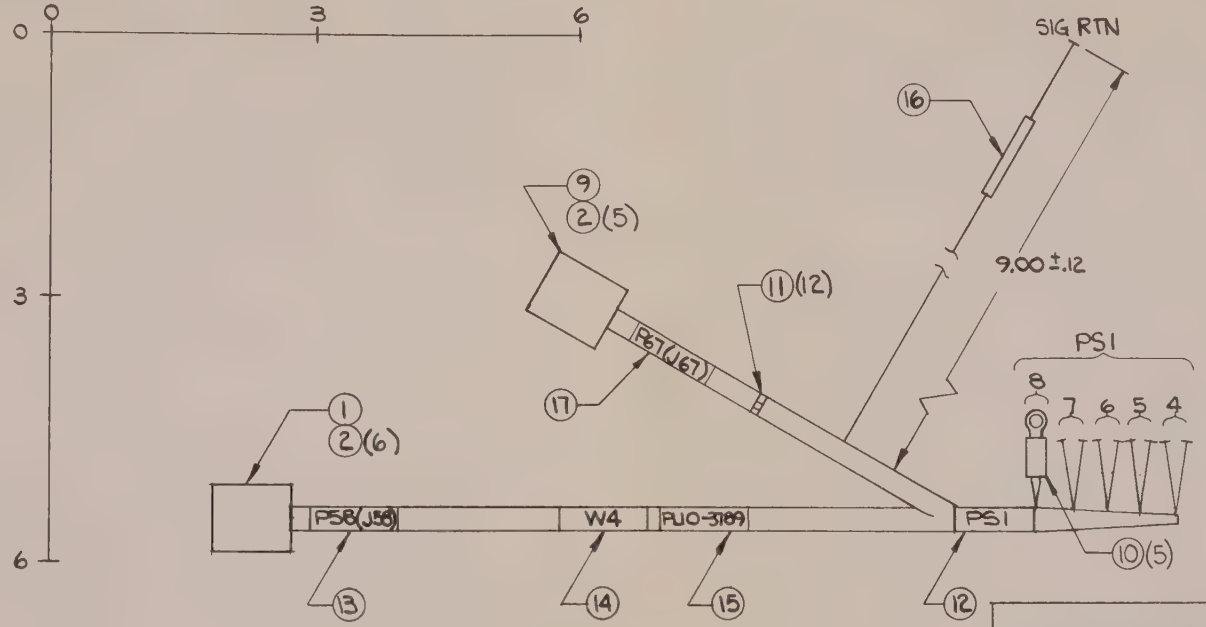
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPL'S	DATE

SIZE C 7-2358 REV O



WIRE LIST					
WIRE NO.	ITEM NO.	COLOR	FROM	TO	FUNCTION
1	3	BRN	P58-5	PS1-8	-15V
2	3	BRN	P67-9		
3	4	RED	P58-3	PS1-7	±15V RTN
4	4	RED	P67-8		
5	5	ORN	P58-1	PS1-6	+15V
6	5	ORN	P67-7		
7	6	YELL	P58-4	PS1-5	+5V RTN
8	6	YELL	P67-2		
9	7	GRN	P58-2	PS1-4	+5V
10	7	GRN	P67-1		
11	8	BLK	P58-6	SIG RTN	SIG RTN

NOTES:
1. STRIP ALL LEADS BACK .19 $^{+.02}_{-.00}$
2. DRAWING IS TO SCALE, USE AS A MANUFACTURING TEMPLATE. BEFORE STARTING FABRICATION, CHECK SCALES ON BLUEPRINT TO INSURE THAT COPY IS WITHIN .062 OF ORIGINAL
3. TOOLING REQD:
   CRIMPING - AMP# 90242-2
   INSERTION - AMP# 455830-1
   EXTRACTION - AMP# 453258-1
   AMP# 455822-2

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS X± .XX± .XXX± ANGLES	DRAWN W.S. Curtis	DATE DEC 78	ANALOGIC, WAKEFIELD, MASS. 01880
			CHECKED R. Swain	7DEC78	CABLE ASSEMBLY (W4)
		MATERIAL	ENGINEER J. Mullen	4-5-79	
		FINISH	ENGINEERING MGR.	4-5-79	
			QUALITY CONTROL		
PLIO-3189	AN05400	APPLICABLE SPECIFICATIONS	PRODUCTION		CODE IDENT NO 31814 / SIZE C / 7-2358 / REV O
NEXT ASSY	USED ON		WEIGHT		SCALE 1/1 / SHEET 1 OF 1
APPLICATION					

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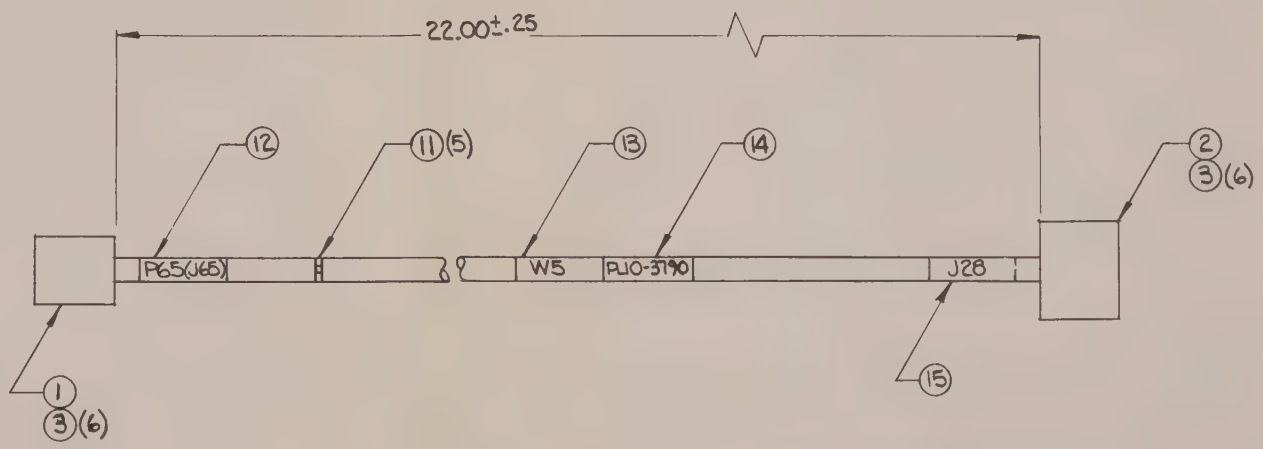
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C 7-2359 REV O



WIRE LIST					
WIRE NO.	ITEM NO.	COLOR	FROM	TO	FUNCTION
1	5	BRN	P65-1	J28-1	DIG GND
2	6	RED	P65-2	J28-2	RDY TO MSR
3	7	ORN	P65-3	J28-3	RDY TO HOLD
4	8	YELL	P65-4	J28-4	TRIGGER
5	9	GRN	P65-5	J28-5	HOLD
6	10	BLU	P65-6	J28-6	DIG GND

NOTES

1. STRIP LEADS BACK .19 $^{+.02}_{-.00}$
2. TOOLING REQD:
   CRIMPING - AMP# 90242-2
   INSERTION - AMP# 455830-1
   EXTRACTION - AMP# 453258-1
   AMP# 455822-2
   AMP# 453468-2

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS X ± XX ± XXX ± ANGLES ±	DRAWN	DATE 1DEC78	ANALOGIC, WAKEFIELD, MASS. 01880
		MATERIAL	CHECKED	7DEC78	CABLE ASSEMBLY (W5)
		FINISH	ENGINEER	4-5-79	
			ENGINEERING MGR.	4-5-79	
			QUALITY CONTROL		
PJO-3790	AND55400	APPLICABLE SPECIFICATIONS	PRODUCTION		CODE IDENT NO 31814 / SIZE C / 7-2359 / REV O
NEXT ASSY	USED ON		WEIGHT		SCALE 1/1 / SHEET 1 OF 1
APPLICATION					

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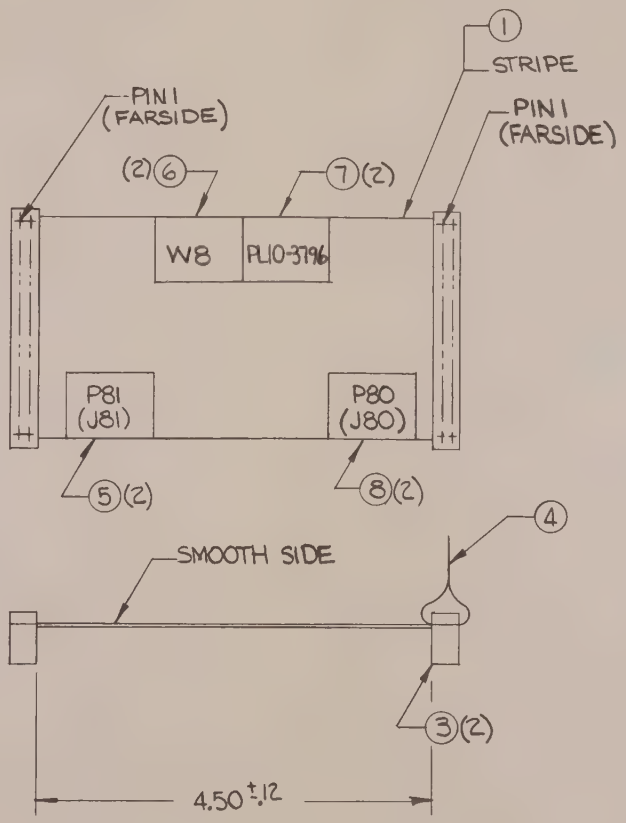
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
#					

SIZE C 7-2365 REV O



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS X ± .XX ± ANGLES .XXX ±	DRAWN	DATE 1DEC78	ANALOGIC. WAKEFIELD, MASS. 01880
			CHECKED	6DEC78	
		MATERIAL	ENGINEER	4-5-79	CABLE ASSEMBLY (W8)
		FINISH	ENGINEERING MGR.	4-5-79	
			QUALITY CONTROL	4-21-79	
PL10-3796	AND'S 5400	APPLICABLE SPECIFICATIONS	PRODUCTION	4-22-79	CODE IDENT NO 31814 / SIZE C / 7-2365 / REV O
NEXT ASSY	USED ON		WEIGHT		SCALE 1/1 / SHEET 1 OF 1
APPLICATION					

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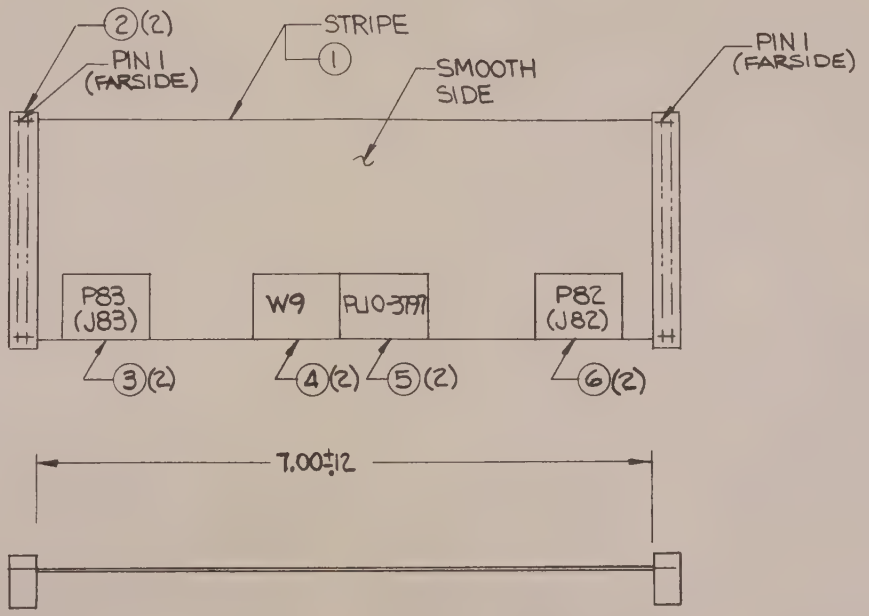
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
M					

SIZE C 7-2366 REV O



PLO-3797	ANDS 5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± ANGLES .XXX ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN	Ed Cyntio	DATE 12EC78
CHECKED	R. Swain	60EC78
ENGINEER	L. Mullen	4-5-79
ENGINEERING MGR.	[illegible]	4-5-79
QUALITY CONTROL	H.P. Swain	4-1-80
PRODUCTION	[illegible]	4-22-80
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY (W9)

CODE IDENT NO	SIZE		REV
31814	C	7-2366	O
SCALE 1/1		SHEET 1 OF 1	

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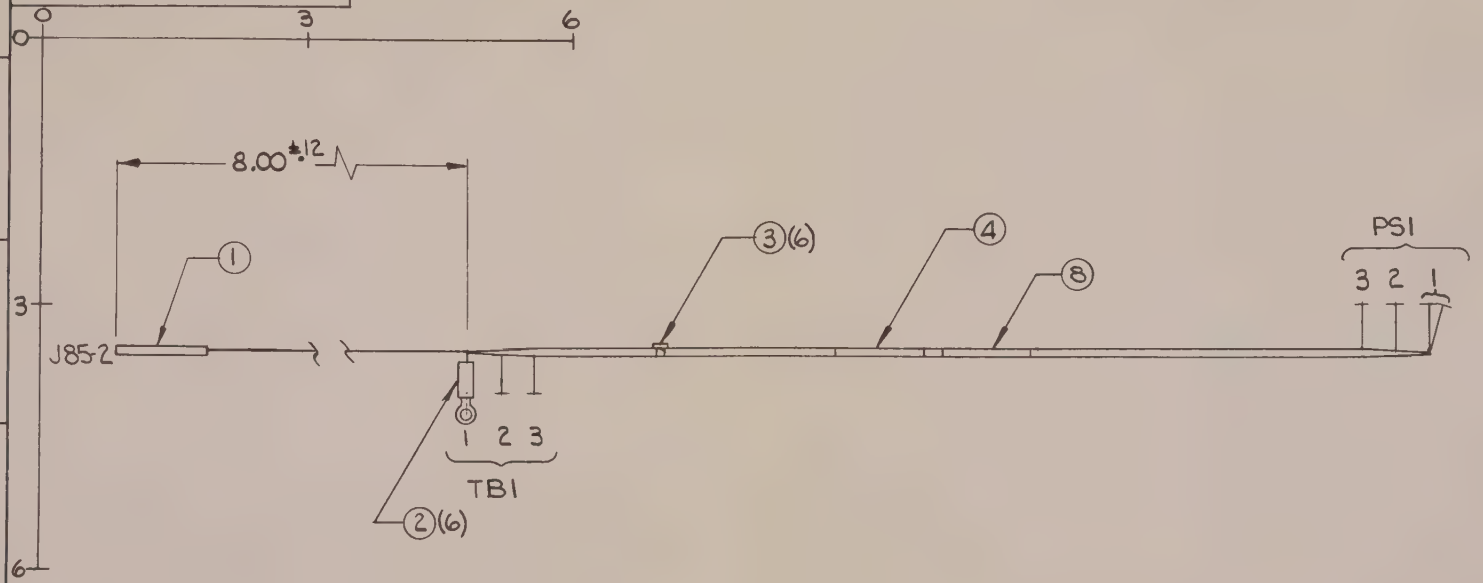
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C | 7-2360 | REV O



WIRE LIST

	WIRE NO.	ITEM NO.	COLOR	FROM	TO	FUNCTION
TWIST	1	5	BLK	PS1-1	TB1-1	A.C. HIGH
	2	9	RED	PS1-1	J85-2	
	3	6	WHT	PS1-2	TB1-2	AC LOW
	4	7	GRN	PS1-3	TB1-3	CHASSIS GND

NOTES:

1. STRIP LEADS BACK .19 $^{.03}_{.00}$
2. DRAWING IS TO SCALE, USE AS A MANUFACTURING TEMPLATE. BEFORE STARTING FABRICATION, CHECK SCALES ON BLUEPRINT TO INSURE THAT COPY IS WITHIN .06 OF ORIGINAL
3. TOOLING REQD:
   CRIMPING - AMP# 90123-2

PLIO-3791	AND5 5450
PLIO-3791	AND5 5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± .XXX ±
ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN		DEC 78
CHECKED		6DEC78
ENGINEER	L. Muller	4-5-79
ENGINEERING MGR.	K. Wilson	4-5-79
QUALITY CONTROL		
PRODUCTION		
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY
(W10)

CODE IDENT NO	SIZE		REV
31814	C	7-2360	O
SCALE 1/1		SHEET 1 OF 1	

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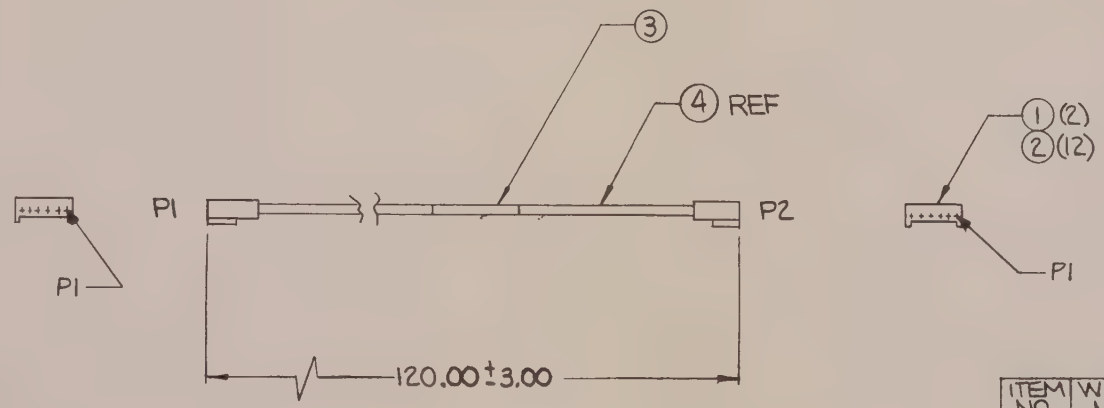
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1	4-645	SEE E.C.O.	R.B.	L.M.	3/28/80
2	4-738	SEE E.C.O.	R.B.	D.P.	6-4-80
3	4-760	SEE E.C.O.	R.B.	D.P.	6-30-80

SIZE C | 7-2376 | REV 3



ITEM NO.	WIRE NO.	COLOR	FROM	TO
4	1A	SHLD.	P1-1	P2-1
	1B	BLK.	P1-2	P2-2
	2A	SHLD.	P1-3	P2-3
	2B	RED	P1-4	P2-4
	3A	SHLD.	P1-5	P2-5
	3B	CLEAR	P1-6	P2-6

NOTES

1. TOOLING REQD

CRIMPING - MOLEX ORDER NO. 11-01-0037
MOLEX MODEL NO. HTR-2262-A
EXTRACTION - MOLEX ORDER NO. 11-03-0019
MOLEX MODEL NO. HT-2759
INSERTION - NONE

PL10-3809	AND55450
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± XX ± ANGLES XXX ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN	Betty Preston	DATE 4APR79
CHECKED		5APR79
ENGINEER		4-5-79
ENGINEERING MGR.		4-6-79
QUALITY CONTROL		
PRODUCTION		
WEIGHT		

ANALOGIC. WAKEFIELD, MASS. 01880

CABLE ASSEMBLY
(AND55450 ANALOG EXP)

CODE IDENT NO	SIZE		REV
31814	C	7-2376	3
SCALE 1/1		SHEET 1 OF 1	

D. L. M. INC.

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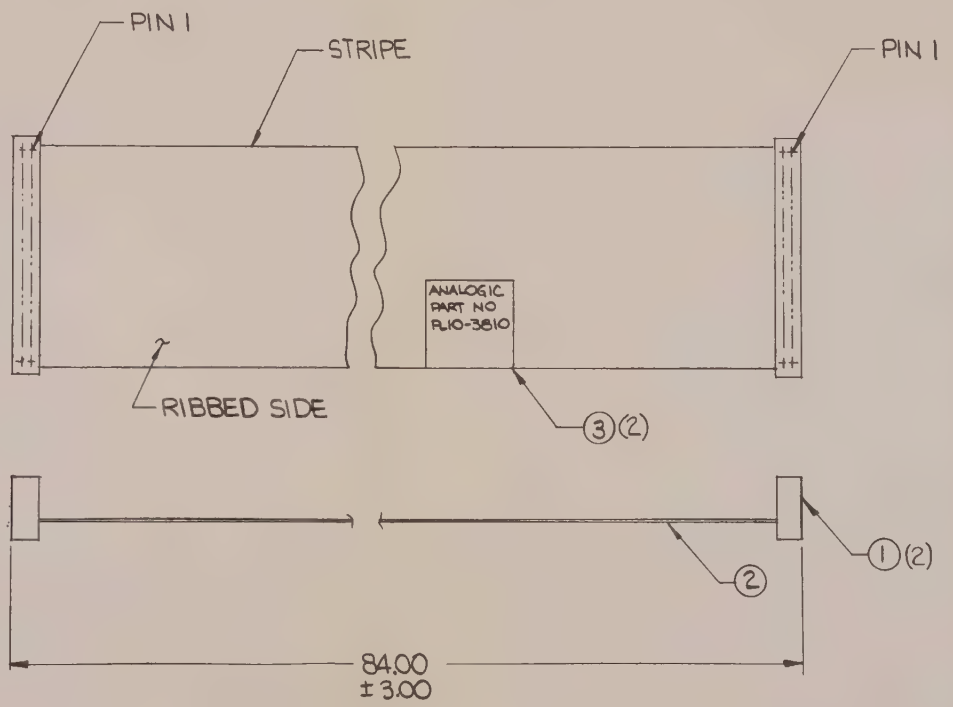
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C 7-2377 REV O



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS X± .XX± .XXX± ANGLES	DRAWN Ruby Rentas	DATE 5APR79	ANALOGIC, WAKEFIELD, MASS. 01880
			CHECKED A.T. Bailey	5APR79	CABLE ASSEMBLY (AND5450 DIGITAL EXP)
		MATERIAL	ENGINEER L. Mullen	4-5-79	
		FINISH	ENGINEERING MGR. R.W. Hum	4-5-79	
			QUALITY CONTROL		
PL10-3810	AND5450	APPLICABLE SPECIFICATIONS	PRODUCTION		CODE IDENT NO 31814 / SIZE C / 7-2377 / REV O
NEXT ASSY	USED ON		WEIGHT		SCALE 1/1 / SHEET 1 OF 1
APPLICATION					

B L H INC.

7.3 Internal Backplane

7.3.0 General

Following the general description of the standard AN3007 and optional AN3500 power supplies is the index of the appropriate drawings and schematics for this section.

7.3.1 Power Distribution

+15, −15, and +5 volt power is supplied to the user cards on the pins listed in the "Internal Backplane" section of the "Architectural Overview" chapter. The ±15 volt return line (power supply center) is called ANALOG GROUND, the +5 volt return line DIGITAL GROUND. The power drawn from the supplies is returned through their respective grounds. ANALOG GROUND is a current carrying line used in the distribution of power to analog components and should not be confused with the low input used during analog measurements. ANALOG and DIGITAL grounds are connected together at a few selected places in the system, but they are not connected together on the user cards as this would create powerful noisy ground loops.

In a system without the optional AN3500 power supply, a single supply provides power for the entire system. The power available for the user cards is shown in Tables 7-1, 7-2, 7-3, and 7-4.

Table 7-1 Single Supply Master Chassis

Supply Voltage	Power Available	Front Panel Current	Interface, SP, A/D	Exp. Card Current	Current Available For All User Cards
+ 5V	5.0A	1.0A	1.2A	1.0A	1.8A
+15V	1.0A	0A	0.3A	0.1A	0.6A
−15V	1.0A	0A	0.3A	0.1A	0.6A

Average Current Available Per User Card: +5V = 0.112 A
+15V = 0.037 A
−15V = 0.037 A

Table 7-2 Single Supply Expansion Chassis

Supply Voltage	Power Available	Exp. Card Current	Current Available For All User Cards
+ 5V	5.0A	1.0A	4.0A
+15V	1.0A	0.1A	0.9A
−15V	1.0A	0.1A	0.9A

Average Current Available Per User Card: + 5V = 0.25 A
+15V = 0.056 A
−15V = 0.056 A

7.3.2 Optional Power Supply

When more current than that provided by the standard supply is required, the AN3500 must be installed. Refer to the "Installation" chapter for instructions. The additional supply is not connected in parallel with the original unit; the power distribution lines are cut so that each supply powers a portion of the system enclosure. In the master chassis the AN3500 supplies +5V power for slots J1 through J12 and ±15V power for J1 through J8; the original supply carries the rest. In an expansion chassis the AN3500 supplies power for slots J1 through J8, and the standard supply powers J9 through J16 and the expansion cards.

Note: The currents listed in Tables 7-3 and 7-4 are average currents. Individual user cards might exceed these averages, so calculate the actual power consumption carefully.

Table 7-3 Dual Supply In The Master Chassis

Average Current Available Per User Card: (Slots J1-J8)	+5V = 0.416 A +15V = 0.125 A −15V = 0.125 A
Average Current Available Per User Card: (Slots J9-J12)	+5V = 0.416 A +15V = 0.075 A −15V = 0.075 A
Average Current Available Per User Card: (Slots J13-J16)	+5V = 0.450 A +15V = 0.075 A −15V = 0.075 A

Table 7-4 Dual Supply In An Expansion Chassis

Average Current Available Per User Card: (Slots J1-J8)	+5V = 0.625 A +15V = 0.125 A −15V = 0.125 A
Average Current Available Per User Card: (Slots J9-J16)	+5V = 0.500 A +15V = 0.112 A −15V = 0.112 A

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Section 7.3
Internal Backplane

Card Number	Drawing Number	Title
—	D5-8664	Internal Backplane Wiring Table
—	D7-8664	Internal Backplane ANDS5400 Assembly
—	D4-8664	Internal Backplane ANDS5400 Machining

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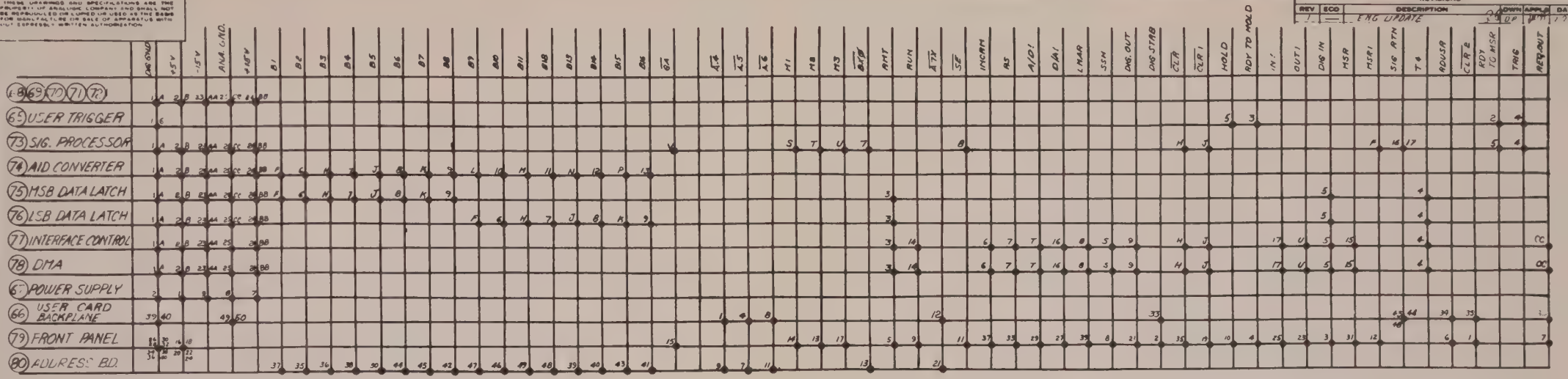
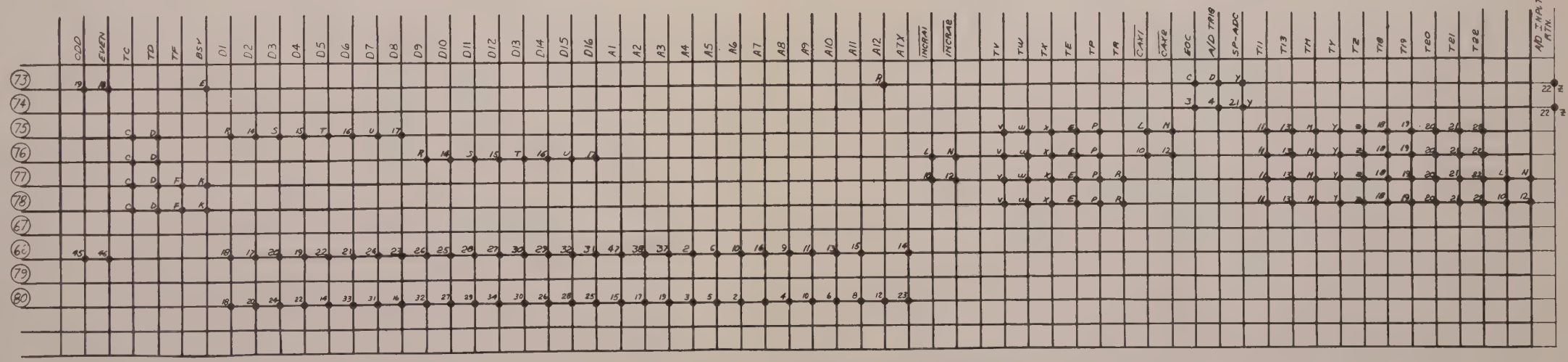
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APP'D	DATE
1	—	ENG UPDATE	DP		1-23-79

D 5-8664 3


GND
+5V
-15V
ANA GND
+15V
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16
A17 A18 A19 A20
H1 H2 H3 BASE
AMT RUN ATX SE INCRM RS A/D1 D/A1 LMAR SSM DIG OUT DIG STAB CLR CLR1 HOLD RDY TO HOLD IN1 OUT1 DIG IN MSR MSR1 SIG ATN T0 ADVSR CLR E RDY TO MSR TRIG REQUEST
(68) (69) (70) (71) (72)
(65) USER TRIGGER
(73) SIG. PROCESSOR
(74) AID CONVERTER
(75) MSB DATA LATCH
(76) LSB DATA LATCH
(77) INTERFACE CONTROL
(78) DMA
(67) POWER SUPPLY
(66) USER CARD BACKPLANE
(79) FRONT PANEL
(80) ADDRESS BD.


GDD EVEN TC TD TF BSY D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 ATX INCRAT INCRAE TV TW TX TE TP TR CAYT CATE EOC A/D TRIG SP-ADC T11 T13 TH TY T2 T18 T19 T20 T21 T22 AD INPUT ATN
(73) (74) (75) (76) (77) (78) (67) (66) (79) (80)

REV	ECO	DESCRIPTION	DWN	APP'S	DATE
2	4376	SEE E.C.O	DP	[illegible]	4-25-80
3	4 MB 4754	SEE EC.O'S	DP	[illegible]	6-30-80

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PKD-8664	MDS 5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

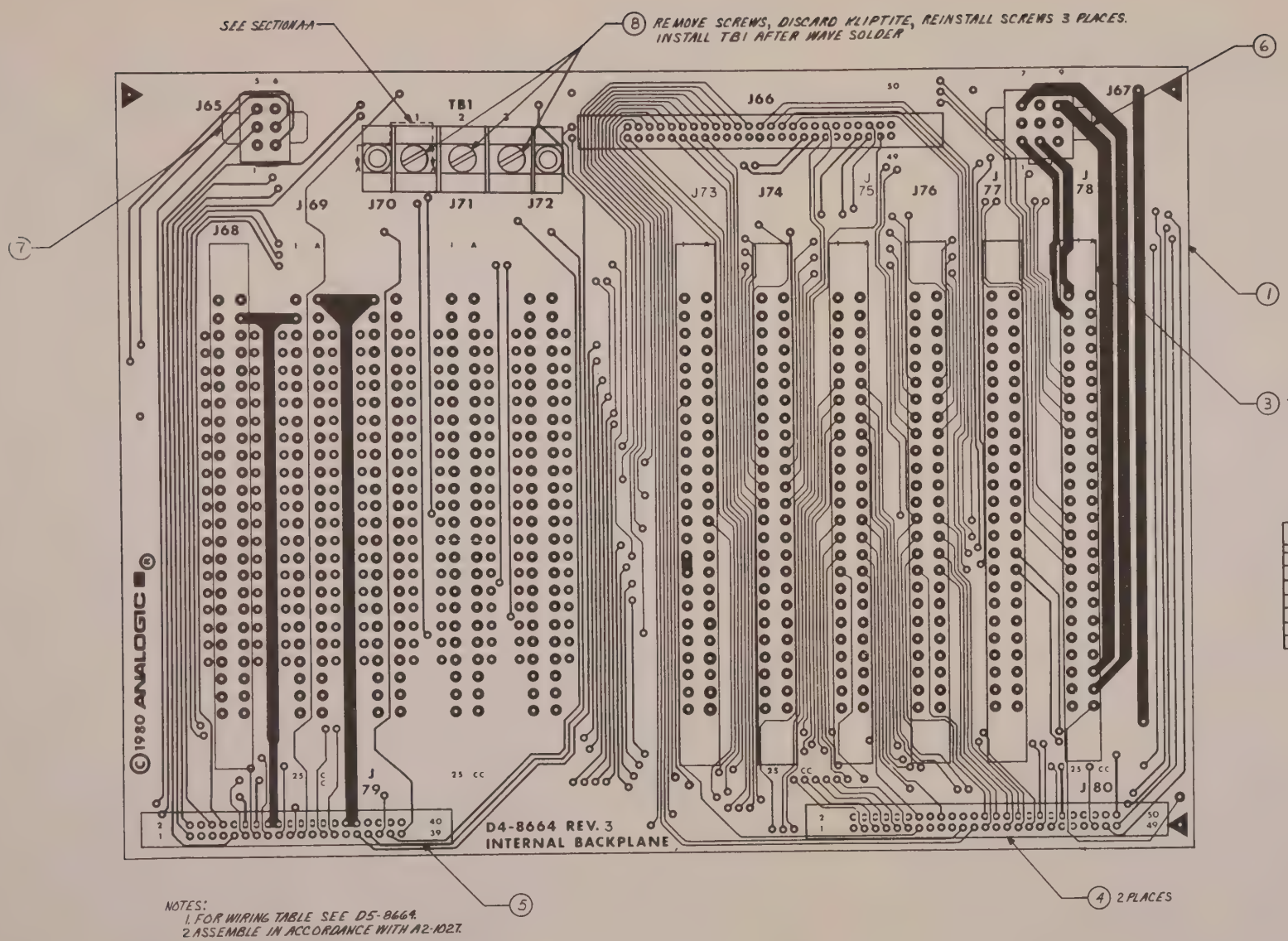
APPLICABLE SPECIFICATIONS

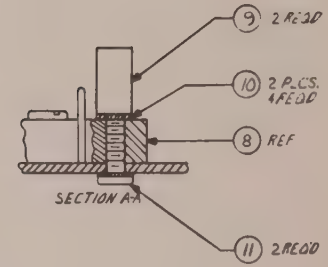
DRAWN		DATE 3-23-79
CHECKED	K. Lee	3-23-79
DESIGNED	L. Mullen	4-5-79
ENGINEER	[illegible]	4-5-79
APPROVED	W. J. Jean	4-1-80
RELEASED	[illegible]	4-21-80

ANALOGIC WAKEFIELD, MASS 01880

WIRING TABLE
INTERNAL BACKPLANE

CODE IDENT NO	DWG	REV
31814	D 5-8664	3
SCALE	ACCOUNT NO	SHEET 1 OF 1





KEYING CHART	
CONNECTOR	LOCATION
J 78	A AND K
J 77	A AND F
J 76	A AND L
J 75	A AND H
J 74	A AND D
J 73	A AND E

NOTES:
1. FOR WIRING TABLE SEE D5-8664.
2. ASSEMBLE IN ACCORDANCE WITH A2-1027.

COMPONENT SIDE

REVISIONS					
REV	ECO	DESCRIPTION	DRAWN	APPROVED	DATE
2	3376	SEE ECO			
3	4140	SEE ECO			

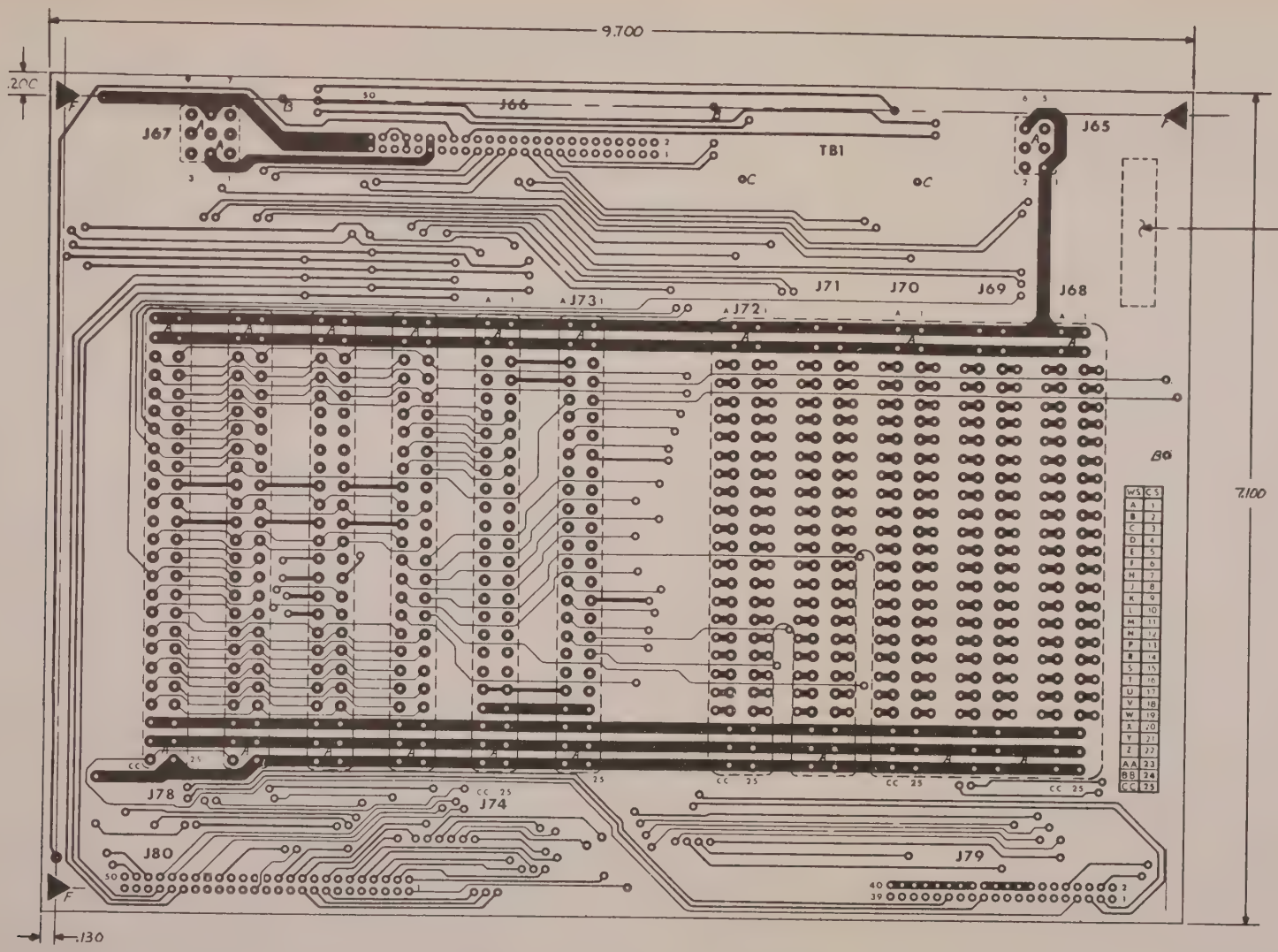
D 7-8664 3

		DRAWN D POHW	DATE 11-21-78
		CHECKED R ROSS	3-23-79
		ENG MFR L. MULLER	4-5-79
		ENGINEERING MGR R.W. HAYENER	4-5-79
		QUALITY CONTROL H.G. ARAMIAN	4-21-80
		PRODUCTION K. KIMBALL	4-21-80
		WEIGHT	
PL10-8664 AND5 5400		APPLICABLE SPECIFICATIONS	
NEXT ASSY	USED ON		
APPLICATION			

ANALOGIC WAKEFIELD MASS 01880

ASSEMBLY
INTERNAL BACKPLANE
AND5 5400

CODE IDENT NO	SIZE	REV
31814	D	3
SCALE 2:1		SHEET 1 OF 1



REVISIONS				
REV	ECO	DESCRIPTION	DRAWN/APPD	DATE
2	4-576	SEE ECO	RP OP/MA	4-25-80
3	4-MB	SEE ECO	RP OP/MA	5-30-80

D 4-8664

NOTES:
1. MATERIAL: GLASS EPOXY (FR4) DOUBLE SIDED, 2 OZ. COPPER, GREEN. .062 THICK.
2. FINISH SOLDER TIN PLATE 60/40 WITH THICKNESS .0005 TO .0010
3. FOR ASSEMBLE SEE D7-8664.
4. FABRICATE PER A2-1040.
5. P.C. BOARD MANUFACTURER WILL BE UL APPROVED AND WILL MARK THEIR UL CODE IDENTIFICATION AND THE FLAMMABILITY RATING EITHER UL-94V-01 OR UL-94-02 (DEPENDING ON MATERIAL USED). THESE MARKINGS WILL BE PUT ON THE WIRING SIDE OF THE BOARD IN THE AREA DESIGNATED.
6.

HOLE	QTY.	SIZE	COMMENTS
UNMARKED	AR	.036-.042 DIA.	AFTER PLATING
A	765	.053-.060 DIA.	AFTER PLATING
B	3	.125 DIA.	DO NOT PLATE
C	2	.156 DIA.	DO NOT PLATE
F	3	.125 DIA.	DO NOT PLATE

WIRING SIDE

	SEE NOTE 1	D. POHJU 11-27-78	ANALOGIC ■ WAKEFIELD MASS. 01880
	SEE NOTE 2	R. ROSS 11-29-78	MACHINING
		L. MULLER 4-5-78	INTERNAL BACKPLANE ANDS 5400
PL10-8664 ANDS 5400		R.W. HAVERNER 4-5-78	
NEXT ASSY. USED ON	A2-1040	H. GARMAHIAN 4-1-80	31814 D 4-8664 REV 3
APPLICATION		K. KIMBALL 4-22-80	SCALE 2:1 SHEET 1 of 4

ZERO-LEVEL INTERFACE

DIGITAL STATUS/CONTROL FOR AN5400

GENERAL DESCRIPTION

The Zero Level Interface extends and buffers internal AN5400 digital control signals and makes them available in TTL-compatible form for customer manipulation. Incorporation of the Zero Level Interface results in maximum flexibility for custom designed user interfaces by providing direct control of the "raw" signals within the AN5400. A typical block diagram of a system using the Zero Level Interface is shown in Figure 1.

The Zero Level Interface physically consists of three plug-in cards using slots 75, 76 and 77 in the AN5400 master chassis. Internal cabling connects the cards to a 50 pin connector mounted on the rear panel of the AN5400. The 48 signals available on this connector are grouped as shown in Figure 1.

The 48 signal lines are available in standard unterminated form, or optionally as a terminated bus structure, as shown in Figures 2 and 3, respectively. The standard unterminated form can drive and can be driven by standard TTL/DTL and is recommended for cabling distances of 7 feet or less. The Optional terminated form can be used for distances of 60 feet or less when mated with similar terminations as shown in Figure 4.

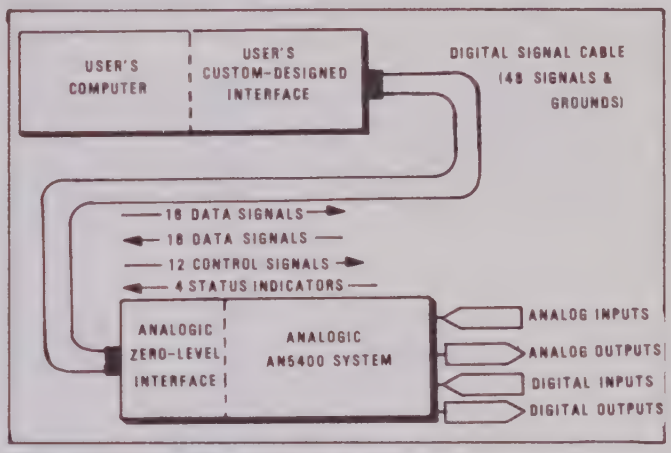


Figure 1. Typical block diagram of system connections of 48 signals and grounds.

A functional listing of the 48 digital signals, in a condensed form, is shown in Table 1.

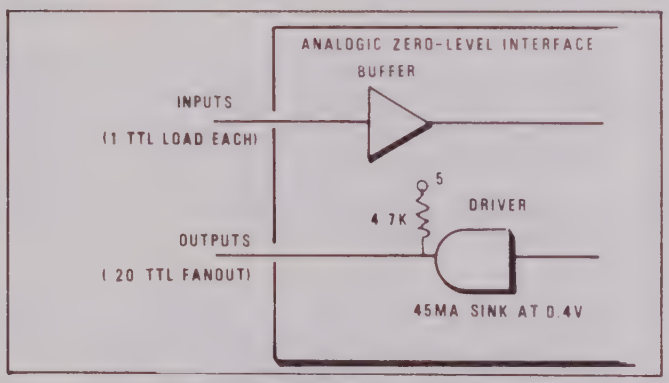


Figure 2. Standard unterminated input configuration.

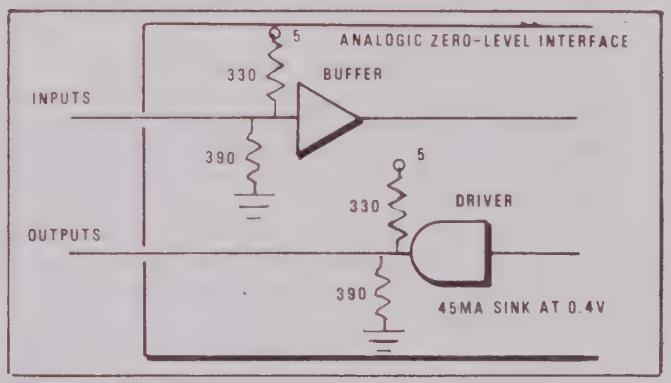


Figure 3. Optional terminated input configuration.

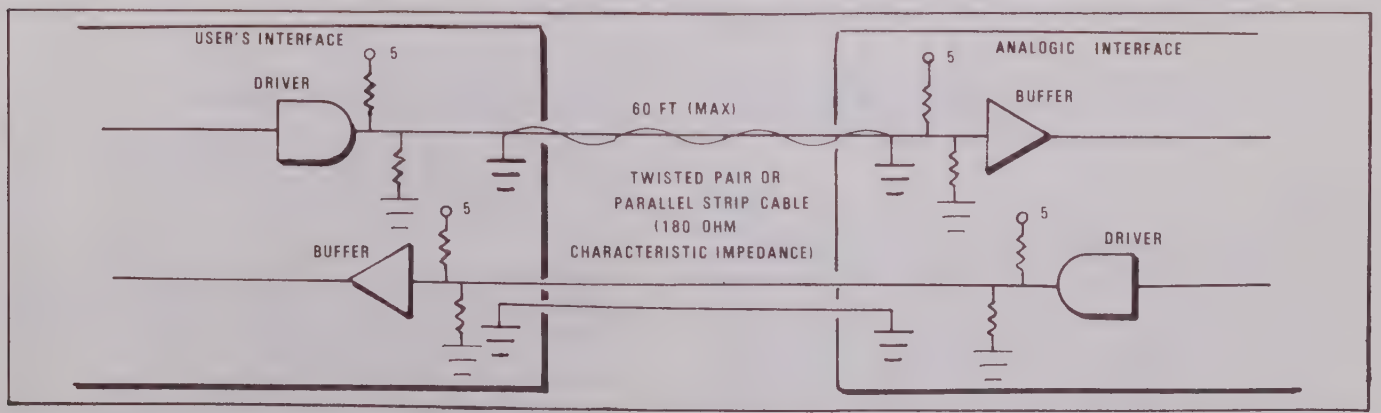


Figure 4. Optional terminated configuration for interface connections up to 60 feet apart.

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. . . The Digitizers

Table 1
Functional Identification of 48 Digital Signals To and From Analogic Zero-Level Interface

SIGNAL NAME	FUNCTIONAL DESCRIPTION	TYPE
BOD 1– BOD 16	16 Parallel data lines from user	Data
BID 1– BID 16	16 Parallel data lines to user	Data
BRUN	"Run" signal from interface, can lock out front panel	Control
BINCRM	Increments address register	
BRS	Loads range register	
BCLR	General clearing function	
BCLR1	Limited clearing function	
BDIGOUT	Load pulse for output modules	
BLMAR	Load address register	
BMSR	Initiates A/D measurement	
BA/D	Causes A/D address decoding	
BD/A	Causes D/A address decoding	
BOUT	Puts digital bus in "out" mode	
BIN	Puts digital bus in "in" mode	
BBSY	High during A/D measurement	Status
BRMT	High in "remote" operation	
BDIGIN	High when bus is in "in" mode	
BSSH	High when S & H amplifiers are "ready to hold"	

DETAILED SIGNAL DESCRIPTIONS

("OUT" refers to a flow from the user's computer to the AN5400; "IN" refers to flow from the AN5400 to the user's computer. See Figure 1.)

DATA SIGNALS (16 Lines IN, 16 Lines OUT)

BOD 1 — BOD 16

Buffered Output Data lines from the user to the AN5400. Sixteen parallel lines that can load range information when used in conjunction with BRS, or load address information when used with BLMAR, or load user output modules (such as D/A converters) when used with BDIG OUT. When used to load range or address data the lines are formatted as below:

When using the lines to load user output modules (with a 12-bit D/A converter as an example) the lines are formatted as below:

BID 1 — BID 16

Buffered Input Data to the user from the AN5400. Sixteen parallel lines that are connected to the A/D converter digital output when the internal 5400 digital buss is in the "out" mode, or to the digital buss itself when it is in the "in" mode. Thus these lines can be used either to read the A/D converter or to read information from a user digital input module. When reading the A/D converter (using a 14-bit converter as an example) the lines are formatted as below:

When reading digital data from a user digital input module the lines are simply formatted as below:

CONTROL SIGNALS (12 LINES OUT)

The AN5400 System can be operated in either local control with the front panel switches and pushbuttons, or in remote control by manipulation of the Zero Level Interface signal lines. While in remote control the front panel switches and pushbuttons are disconnected and will have no effect on the system, similarly while in local control the Zero Level Interface control lines and data lines (BOD 1 — BOD 16) are disconnected from the AN5400 and do not affect local operation. To prevent inadvertant pulses from occuring while switching from local to remote operation, control signals should be normally held low. Thus with the exception of BRUN which may be held high or low, all control signals should be positive going pulses.

BRUN

This signal can be used to prevent switching to local control. If the AN5400 is in remote control and BRUN is held high, the system cannot be switched into local control with the front panel pushbutton.

BINCRM

This is a positive pulse that increments the address register to address the next higher channel. The address register will increment by 1 if the range register has been set for single-ended operation, or will increment by two if set for differential operation. Incrementation begins after the falling edge of the pulse. Minimum pulse width = 400nsec.

BRS

This is a positive pulse that loads the data present on the digital bus (BOD 1 — BOD 4) into the range register. Loading occurs on the falling edge of BRS. Information on the data lines must be held constant for 300nsec before and after the falling edge of this signal. Minimum pulse width = 400nsec.

BCLR

This is a positive pulse that performs a general clearing and resetting operation throughout the AN5400. This pulse causes A/D address decoding, puts the internal digital bus in the "out" mode, clears the range register, clears the address register, clears the user digital output modules, and appears on the connectors for all user modules. Clearing takes place while this pulse is high. Minimum pulse width = 400nsec.

BCLR1

This is a positive pulse that performs a limited clearing operation within the AN5400 without disturbing any register contents. This pulse resets BSSH and resets busy (BBSY). Clearing takes place while this pulse is high. Minimum pulse width = 300nsec.

BDIGOUT

This is a positive pulse that causes the registers on the addressed user output module to be loaded with the information on the digital data bus . Minimum pulse width = 300nsec.

BLMAR

This is a positive pulse that loads the data present on the digital bus (BOD 5 — BOD 16) into the address register. Loading occurs on the falling edge of this signal. Information on the data lines must be held constant for 300nsec before and after the fall of BLMAR. Minimum pulse width = 400nsec.

BMSR

This is a positive pulse that initiates an A/D measurement sequence. The sequence begins on the rising edge of BMSR. Minimum pulse width — 400nsec, maximum pulse width — 10usec.

BA/D

This is a positive pulse that causes the register to be decoded in the "A/D" format according to the patch plug within the AN5400. This decoded address is applied to the address bus for the user modules. Normally, the "A/D" mode addresses 32 channels per card. Minimum pulse width = 300nsec.

BD/A

This is a positive pulse that causes the address register to be decoded in the "D/A" format according to the patch plug within the AN5400. This decoded address is applied to the address bus for the user modules. Normally, the "D/A" mode addresses 4 channels per card. Minimum pulse width = 300nsec.

BOUT

This is a positive pulse that puts the internal AN5400 digital bus into the "out" mode. In the "out" mode data lines BOD 1 — BOD 16 are connected to the internal digital bus and data lines BID 1 — BID 16 are connected to the A/D output lines. Minimum pulse width = 300nsec.

BIN

This is a positive pulse that puts the internal AN5400 digital bus into the "in" mode. In this mode data lines BOD 1 — BOD 16 are disconnected from the internal digital bus while the lines from a previously addressed user digital input module are connected to the internal digital bus . Additionally, data lines BID 1 — BID 16 are disconnected from the A/D converter and connected to the internal digital bus . Minimum pulse width = 300nsec. Maximum settling time of new data on BID 1 — BID 16 = 3usec.

STATUS SIGNALS (4 LINES IN)

BBSY

Buffered BuSY Signal. This signal goes high when a measurement sequence is begun and falls when the measurement is complete. Valid data will exist on the A/D output lines after the fall of BBSY.

BRMT

Buffered ReMoTe Signal. This signal is high when the system is in remote control and is a reflection of the "remote" indicator light on the AN5400 display panel.

BDIGIN

Buffered DIGital INput Signal. This signal is high when the AN5400 internal digital buss is in the "in" mode. When this signal is low the digital buss is in the "out" mode.

BSSH

Buffered Simultaneous Sample & Hold Signal. This signal is high when the Simultaneous Sample & Hold Amplifiers (AN5400 System Option) are in the "ready to hold" state. BSSH is particularly useful as an indicator when an external signal is used to place the SSH's into hold.

Table 2
ZERO-LEVEL INTERFACE PIN CONNECTIONS
(50 PIN MALE)

SOURCE AN5400 INTERFACE PCB	50-PIN CONNECTOR	SIGNAL NAME	SOURCE	PIN	SIGNAL
—	1	DIG GND	76-8	26	BID16
75-16	2	BOD8	76-7	27	BID15
75-15	3	BOD7	76-6	28	BID14
75-14	4	BOD6	76-5	29	BID13
75-13	5	BOD5	76-4	30	BID12
75-12	6	BOD4	76-3	31	BID11
75-11	7	BOD3	76-2	32	BID10
75-10	8	BOD2	76-1	33	BID9
75-9	9	BOD1	77-16	34	BDIGIN
75-8	10	BID8	77-15	35	BSSH
75-7	11	BID7	77-14	36	BBSY
75-6	12	BID6	77-13	37	BRMT
75-5	13	BID5	77-12	38	BRS
75-4	14	BID4	77-11	39	BDIGOUT
75-3	15	BID3	77-10	40	BIN
75-2	16	BID2	77-9	41	BOUT
75-1	17	BID1	77-8	42	BD/A
76-16	18	BOD16	77-7	43	BA/D
76-15	19	BOD15	77-6	44	BMSR
76-14	20	BOD14	77-5	45	BLMAR
76-13	21	BOD13	77-4	46	BINCRM
76-12	22	BOD12	77-3	47	BCLR1
76-11	23	BOD11	77-2	48	BCLR
76-10	24	BOD10	77-1	49	BRUN
76-9	25	BOD9	—	50	DIG GND

GENERAL OPERATING CONSIDERATIONS

While in local operation, the AN5400 will not respond to any control signals supplied to the zero level interface. Similarly while in remote operation the front panel controls will be inoperative.

During the measurement sequence, while BBSY is high, it is advisable to keep all digital lines in a static condition to avoid influencing the Analog signals within the 5400.

Certain pairs of control signals are complimentary, i.e.: one signal sets a flip-flop while another signal resets the same flip-flop. These pairs of signals, if applied simultaneously, would give indeterminate results. The signals that must not be applied together are as follows:

BCLR and BINCRM, BCLR and BRS, BCLR and BLMAR, BCLR and BMSR, BCLR and BD/A, BCLR and BIN, BCLR and B DIGOUT, BCLR1 and B DIGOUT, BCLR1 and BMSR, BINCRM and BLMAR, BD/A and BA/D, BOUT and BIN.

Some signals can be paired together and applied simultaneously. In fact, this is an advisable technique to simplify the interface and increase the digital throughput rate. Suggested pairs of signals are: BRS and BLMAR, BCLR and BCLR1, BA/D and B OUT, (OR) BD/A and B OUT. Larger groups may also be formatted; e.g.; BLMAR, BRS, BA/D and BOUT may be applied together.

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BUFFERED CONTROL INTERFACE for the ANDS5400

INTERFACE DESCRIPTION

The Buffered Control Interface extends and buffers internal ANDS5400 digital control signals and data lines, making them available in TTL-compatible form for customer manipulation. Incorporating the Buffered Control Interface results in maximum flexibility for user designed computer interfaces by providing direct control of the "raw" signals within the ANDS5400. Figure 1 shows a block diagram of a typical system using this interface.

This interface physically consists of three printed circuit boards that plug into slots 75, 76 and 77 of the ANDS5400 Master Chassis. Internal cabling connects these boards to three connectors mounted on the rear of the Master Chassis.

The 49 signals available on the connectors are classified as data, control, and status, as listed in Table 1. These signal lines are available in either unterminated form or as a terminated bus structure, as shown in Figures 2 and 3, respectively. The unterminated form can drive, and can be driven by, standard TTL/DTL, and is recommended for cabling distances of 7 feet or less. The terminated form can be used for distances of up to 60 feet when mated with similar terminations on the user interface, as shown in Figure 3.

NOTE

Nomenclature Convention: When applied to external communication, *out* refers to a flow from the user's computer to the ANDS5400; *in* refers to flow from the ANDS5400 to the user's computer.

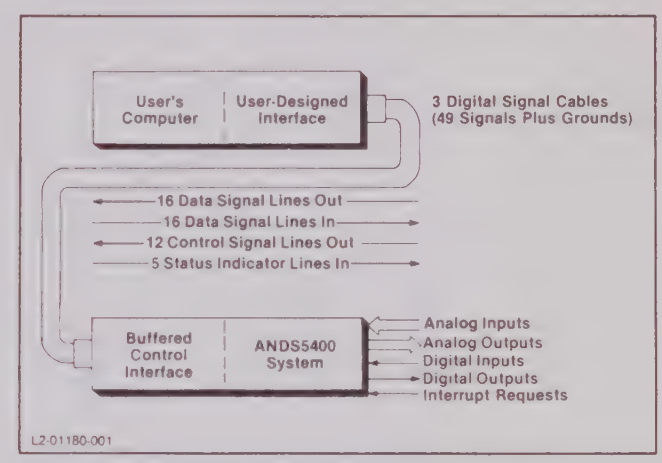

Figure 1. Typical System Block Diagram

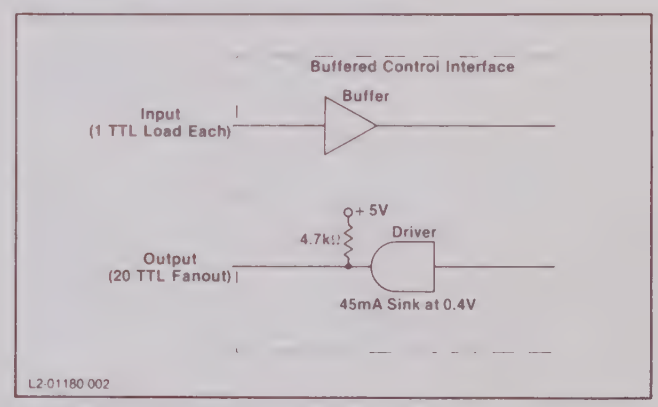

Figure 2. Unterminated Input Configuration

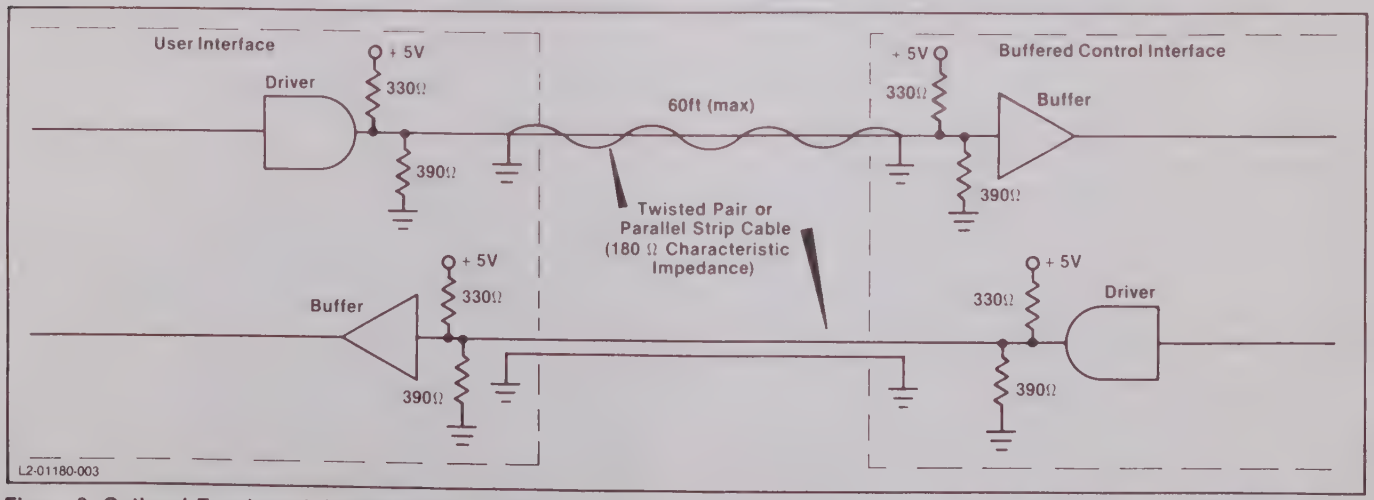

Figure 3. Optional Terminated Configuration for Interface Connections up to 60 feet Apart

TABLE 1. Summary of Buffered Control Interface Signals*		
Signal Name	**Functional Description**	**Type**
BOD 1-BOD 16	16 Parallel data lines from user	Data Out
BID 1-BID 16	16 Parallel data lines to user	Data In
BCLR	General clearing function	Static Controls
BCLR1	Limited clearing function	
BRUN	"Run" signal from interface, can lock out front panel	
BA/D	Sets decoding of the address register to be in the "A/D" format	Address Decoding Controls
BD/A	Sets decoding of the address register to be in the "D/A" format	
BRS	Loads range register	Address Register & Range Register Controls
BLMAR	Loads address register	
BINCRM	Increments address register	
BIN	Puts internal ANDS5400 digital bus into the "in" mode	Digital Bus Controls
BOUT	Puts internal ANDS5400 digital bus into the "out" mode	
BMSR	Initiates A/D measurement	A/D Control
BDIGOUT	Load pulse for output modules	D/A & Digital Output Control
BBSY	High during A/D measurement	Status In
BRMT	High in "remote" operation	
BDIGIN	High when internal ANDS5400 digital bus is in the "in" mode	
BSSH	High when S & H amplifiers are "ready to hold"	
54RQST	High when user card requests service	

*For connector pinout, see Table 2.

SIGNAL DESCRIPTIONS

DATA SIGNALS (16 Lines In, 16 Lines Out)

BOD 1 — BOD 16

Buffered Output Data lines from the user to the ANDS5400. Sixteen parallel lines that can load range information when used in conjunction with BRS, or load address information when used with BLMAR, or load user output modules (such as D/A converters) when used with BDIGOUT. When used to load range or address data the lines are formatted as below:

When loading user output modules (for example, when using a 12-bit D/A converter) the lines are formatted as below:

BID 1 — BID 16

Buffered Input Data to the user from the ANDS5400. Sixteen parallel lines that are connected to the A/D converter's digital output when the internal ANDS5400 digital bus is in the "out" mode, or to the digital bus itself when it is in the "in" mode. Thus these lines can be used either to read the A/D converter or to read information from a user digital input module. When reading the A/D converter (using a 14-bit converter as an example) the lines are formatted as follows:

When reading digital data from a user digital input module the lines are formatted as below:

CONTROL SIGNALS (12 Lines Out)

The ANDS5400 System can be controlled either locally (via the front panel switches and pushbuttons) or remotely via the Buffered Control Interface. When the system is in remote control, the front panel controls are disconnected and do not affect operation. Status and data, however, are still available to the front panel. Similarly, when the system is under local control, the Buffered Control Interface control lines and data output lines (BOD 1 — BOD 16) are disconnected from the ANDS5400 and do not affect local operation.

To prevent inadvertant pulses from occuring while switching from local to remote operation, control signals should be normally held low. **Thus with the exception of BRUN,** which may be held high or low, **all other control signals**

should be positive going pulses. Timing and operation of each control signal are described in separate paragraphs below.

BCLR
This is a positive pulse that performs a general clearing and resetting operation throughout the ANDS5400. This pulse puts the internal digital bus into the "out" mode, and selects subsequent decoding of the address register to be in the A/D format (equivalent to transmitting both BOUT and BA/D simultaneously). It also clears the range and address registers, clears the user digital output modules (where enabled) and appears on the connectors for all user modules. Clearing takes place while this pulse is high. Minimum pulse width = 400ns.

BCLR1
This is a positive pulse that performs a limited clearing operation within the ANDS5400 without disturbing any register contents. This pulse resets BSSH and resets busy (BBSY). Clearing takes place while this pulse is high. Minimum pulse width = 300ns.

BRUN
This signal can be used to prevent switching to local control. If the ANDS5400 is in remote control and BRUN is held high, the system cannot be switched into local control with the front panel pushbutton.

BA/D
This is a positive pulse that causes the ANDS5400 address register to be decoded in the "A/D" format. Normally, the "A/D" mode addresses 32 channels per module. Minimum pulse width = 300ns. Rising edge is active.

BD/A
This is a positive pulse that causes the address register to be decoded in the "D/A" format. This format addresses up to four output channels per module. It is also used for addressing digital inputs. Minimum pulse width = 300ns; rising edge active.

BRS
This is a positive pulse that latches the data present on the output lines (BOD 1 — BOD 4) into the ANDS5400 range register. Loading occurs on the falling edge of BRS. Information on the data lines must be held constant for 300nsec before and after the falling edge of this signal. Minimum pulse width = 400ns.

BLMAR
This is a positive pulse that latches the data present on output lines BOD 5 — BOD 16 into the address register. Loading occurs on the falling edge of this signal. Data on the lines must be held constant for 300ns before and after the fall of BLMAR. Minimum pulse width = 400ns.

BINCRM
This is a positive pulse that increments the address register to address the next higher channel. This register will increment by 1 if the range register has been set for single-ended operation, or will increment by two if set for differential operation. Incrementing occurs after the falling edge of this pulse. Minimum pulse width = 400ns.

BIN
This is a positive pulse that puts the internal ANDS5400 digital bus into the "in" mode. This mode is used for reading digital data. In this mode data lines BOD 1 — BOD 16 are disconnected from the internal digital bus while the lines from the previously addressed user digital input module are connected to the internal digital bus. Additionally, data lines BID 1 — BID 16 are disconnected from the A/D converter and connected (via the interface) to the internal digital bus. Minimum pulse width = 300ns. Maximum settling time of new data on BID 1 — BID 16 = 3μs after the rising edge.

BOUT
This is a positive pulse that puts the internal ANDS5400 bus into the "out" mode. This mode is used for writing digital data and for reading analog data. In the "out" mode, data lines BOD1 — BOD16 are connected (via the interface) to either the internal digital bus or the address and range registers, while data lines BID1 — BID16 are connected to the A/D output. Minimum pulse width = 300ns; rising edge is active.

BMSR
This is a positive pulse that initiates an A/D measurement sequence. The sequence begins on the rising edge of BMSR. Minimum pulse width = 400ns, maximum pulse width = 10μs.

BDIGOUT
This is a positive pulse that causes data present on BOD1 — BOD16 to be applied to the interal ANDS5400 digital bus (while being buffered by the interface), and then loaded into registers on the currently addressed user output module. Loading occurs on the rising edge of BDIGOUT. Information on the BOD lines must be held constant for 300ns before and after this edge. Minimum pulse width = 300ns.

STATUS SIGNALS (5 Lines In)

BBSY
Buffered Busy Signal. This signal goes high when an A/D measurement sequence is begun and falls when the measurement is complete. Valid A/D data will exist after the fall of BBSY.

BRMT
Buffered Remote Signal. This signal is high when the system is in remote control and is a reflection of the "remote" indicator light on the ANDS5400 display panel.

BDIGIN
Buffered Digital Input Signal. This signal is high when the ANDS5400 internal digital data bus is in the "in" mode. When this signal is low the bus is in the "out" mode.

BSSH
Buffered Simultaneous Sample & Hold Signal. This signal is high when the Simultaneous Sample & Hold Amplifiers (ANDS5400 System Option) are in the "ready to hold" state. BSSH is particularly useful as an indicator when an external signal is used to place the SSH's into hold.

54RQST
This line goes high within 5μs after a user card generates an interrupt request, remaining high until the user services the request. Refer to the ANDS5400 software documentation for reading the interrupt vectors.

If multiple requests are pending, *i.e.* other cards interrupt before the line goes low or more than one card interrupts simultaneously, the line will go low for a minimum of 1μs as each request is serviced. The rising edge of the request line is used to initiate each new interrupt. Single or multiple requests can be handled without program modification.

To determine if there are other interrupts pending, the user must either command the BOUT mode or change the address. It is recommended that the data from the interrupting card always be read immediately. This act of servicing the interrupt automatically changes the address and reenables the ability to read other interrupts that may be pending.

OPERATION NOTES

Upon powering up, the ANDS5400 will be initialized in the remote mode. BCLR and BCLR1 should both be sent prior to operation.

During an A/D measurement sequence, while BBSY is high, it is advisable to keep all digital lines in a static condition to avoid influencing the analog signals within the ANDS5400.

Some signals can be paired and applied simultaneously. In fact, this is an advisable technique to simplify the interface and increase the throughput rate. Suggested pairs of signals are: BRS and BLMAR, BCLR and BCLR1, BD/A and BLMAR, BA/D and BOUT, or BD/A and BOUT. Larger groups may also be formatted, *e.g.*, BLMAR, BRS, BA/D and BOUT may by applied together, or BLMAR, BD/A and BOUT may be applied together.

Certain pairs of control signals should not be applied simultaneously, *e.g.*, if one signal sets a flip-flop while another resets the same flip-flop. The signals that should not be applied simultaneously are as follows:

This Control Signal	Not Simultaneous With Any of These
BCLR	BINCRM BRS BLMAR BMSR BD/A BIN BDIGOUT
BD/A	BA/D

This Control Signal	Not Simultaneous With Any of These
BCLR1	BDIGOUT BMSR
BINCRM	BLMAR
BOUT	BIN BDIGOUT
BMSR	BLMAR BA/D BRS

TABLE 2. Rear Panel Connections*

J22				J23				J24			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	BID 1	2	BID 2	1	BID 9	2	BID 10	1	54RQST	2	BRUN
3	BID 3	4	BID 4	3	BID 11	4	BID 12	3	BCLR	4	BCLR1
5	BID 5	6	BID 6	5	BID 13	6	BID 14	5	BINCRM	6	BLMAR
7	BID 7	8	BID 8	7	BID 15	8	BID 16	7	BMSR	8	BA/D
9	BOD 1	10	BOD 2	9	BOD 9	10	BOD 10	9	BD/A	10	BOUT
11	BOD 3	12	BOD 4	11	BOD 11	12	BOD 12	11	BIN	12	BDIGOUT
13	BOD5	14	BOD 6	13	BOD 13	14	BOD 14	13	BRS	14	BRMT
15	BOD 7	16	BOD 8	15	BOD 15	16	BOD 16	15	BBSY	16	BSSH
17	Digital Ground	18	Digital Ground	17	Digital Ground	18	Digital Ground	17	BDIGIN	18-34	Digital Ground
19	Digital Ground	20	Digital Ground	19	Digital Ground	20	Digital Ground				

*Unterminated option: all inputs are standard TTL voltage with 1 unit load; all outputs are standard TTL with 20 unit fanout.
Terminated option: termination elements for inputs and outputs are as defined in Figure 3.

Interconnection Note

Ribbon mass termination mating connectors for J22, J23, and J24 are supplied. Most applications will require a transition from ribbon cable to some other form of wiring before connecting to the computer. *Potential cross coupling of signals can be minimized* by implementing this transition **as close to the computer** as possible. When operating over long distances (10 to 60 feet), cross coupling may be further minimized by the use of twisted pairs (one lead from each pair should be grounded).

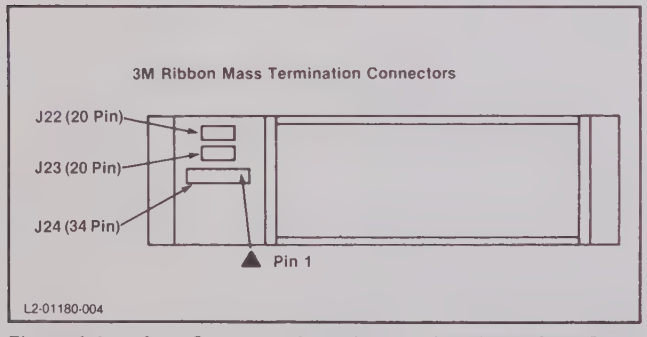

Figure 4. Interface Connector Locations on ANDS5400 Rear Panel

ORDERING GUIDE

For an **ANDS5400** System, complete with a Buffered Control Interface, simply specify

ANDS5400 — □ — **B** — □

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7.4 Interfaces

7.4.0 General

This section presents information on the following interfaces: General Purpose Interface, – 35 2 Byte 8 Bit General Purpose Interface, Buffered Control Interface, IEEE 488-1975 Digital Interface, Nova PIO/DMA Interface, PDP-11 PIO/DMA Interface, LSI-11 PIO/DMA Interface, and Asynchronous Serial Line Interface. It is recommended that regardless of the customer's interface that the user read the "General Interface Operation" section of this chapter first.

Section 7.4.2 lists the interface slot connections and is followed by the index of the data sheets, drawings, and schematics for each specific interface.

7.4.1 Interface Operation Overview

The ANDS5400 is compatible with virtually any computer or microprocessor available today because of its four basic methods of interfacing: control line manipulation, general purpose handshake, direct memory access, and serial/byte handshake.

Control line manipulation is accomplished through the – 19 A/B Buffered Control Line (BCL) Interface. The AC470's are data buffers located in slots J75 and J76 that receive and transmit the upper and lower 8 bits of the input/output data words, respectively. The AC463, a control card located in slot J77, accepts discrete control signals generated in the user designed interface and buffers them prior to their use in the ANDS5400 system. This type of interface is the most complex to implement because the user must design hardware to generate all the control signals required by the system; however, it provides the greatest speed and flexibility through its discrete level of control. Full details on this interface are found on the – 19 A/B Interface data sheet. Note that the user designs and provides an interface, which is normally located in the host computer's I/O cage, and the cables that are required to connect that interface to the ANDS5400.

The General Purpose Interface (GPI) is found by the majority of users to be the easiest interface to implement. The AC470's, located in slots J75 and J76, are data buffers for the input/output data words. Via the ANDS5400 interface bus structure, the AC471, a control card installed in slot J77, detects and decodes the upper four bits of the input data word from the computer. These bits contain an Operation Code (Op Code) that directs a specific operation within the ANDS5400 as described in the General Purpose Interface data sheet. The result of the decoding operation is the generation of the control signals required to perform the activity directed. The GPI is equivalent to a buffered control line interface preceded by a complex decoder that generates the required control signals. As with the – 19 Interface, the user provides the cables from the computer and a 16 bit parallel I/O card in the computer I/O cage. The complete details of the operation of this interface are found in the GPI Data Sheet. With minor modifications the interface is used to support the – 23 A/B, – 24 A/B, – 25 A/B, – 26 A/B, – 27 A/B, – 28 A/B, – 29 A/B, – 32 A/B, and – 34 A/B products.

A version of the GPI is the – 35 A/B 2 Byte 8 Bit Interface. The – 35 Interface involves the modification of all three of the cards in the General Purpose Interface, enabling the unit to receive and transmit the 16 bit data in two eight bit bytes and providing the necessary byte handshake and enable lines. Details on the operation of the – 35 Interface are found in the – 35 Interface Application Note.

There are two types of Direct Memory Access (DMA) interfaces, those for Digital Equipment Corporation (DEC) computers and those for Data General (DG) computers. Despite hardware differences, both types of interfaces basically operate in the same manner.

The – 02 Nova/Eclipse, the – 18 LSI-11, and the – 31 PDP-11 Interfaces are programmed input/output (PIO) and Direct Memory Access devices. The DEC units include a – 19 Interface in the ANDS5400, and cables from the ANDS5400 to the Analogic supplied I/O board(s) in the host computer, (and exerciser and diagnostic software on floppy disc). The – 31 Interface includes two I/O boards, the AC473, which is a PIO board that encompasses the basic interface control logic and control line generation, and the AC472, which is the DMA controller. These boards plug into the computer bus. The – 18 Interface includes a single I/O board, the DC7010, which encompasses both PIO and DMA functions.

The Data General DMA Interface includes four boards mounted within the ANDS5400 system. The user supplies a standard cable available from Data General that attaches to the bus extension connector or a paddle board bus extender. The boards within the system perform the following functions: the AC403's in slots J75 and J76 perform the data latch/buffering function similar to that performed by the AC470; the AC404 board in slot J77 provides control logic and generates the required control signals to drive the system; and the AC405, located in slot J78, performs both PIO and DMA handshake functions with the computer bus.

The Serial/Byte Interfaces are the – 13 IEEE 488-1975 standard bus interface, and the – 30, – 36, and – 37 Serial Line Units for RS232, RS422, and 20mA current loop communication paths, respectively. These interfaces are markedly slower than the previous interfaces due to protocol overhead, but they provide relatively simple communication paths to the host computer.

The serial line interfaces consist of four cards. The AC477, located in slot J78, provides the signal conditioning/buffering required on the reception/transmission lines; these lines are brought out to a standard EIA 25-pin receptacle at the rear of the system. The AC475 in slot J76 contains a UART chip for serial reception and transmission of data. The data is split on the UART card. The actual "data" is directed to the AC414 in slot J75 for buffering and storing data, and the command information is directed to the AC476 in slot J77 for decoding and generating the control signals for the system operation directed for the computer.

The – 13 IEEE Interface is comprised of three cards: the AC407, located in slot J75, latches and buffers the upper 8 bits of data; the AC408, located in slot J76, latches and buffers the lower 8 bits of data; the AC409 in slot J77 decodes command information from the protocol transmitted with the data, generates the control signals for the ANDS5400, and provides the required handshake with the IEEE bus.

To summarize, slots J75 and J76 are data buffer slots, which in most cases have bidirectional logic that supports the MSB and LSB data bytes, respectively. Slot J77 generates the control signals and maintains handshake with the computer interface. J78, when used, performs special tasks unique to the interface requirements.

7.4.2 Slot Connections

The following charts list the pin names and connections for the four interface slots J75, J76, J77, and J78. All of the various interfaces available for the system use

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slots J75, J76, and J77; slot J78 is used only for the most complex designs. Generally, the four slots are used as follows:

J75 — MSB DATA LATCH — This slot receives the 8 most significant bits of the A/D converter and communicates with the 8 most significant bits of the bidirectional digital bus.

J76 — LSB DATA LATCH — This slot receives the 8 least significant bits of the A/D converter and communicates with the 8 least significant bits of the bidirectional digital bus.

J77 — INTERFACE CONTROL — This slot has access to all of the control lines and status indicators that coordinate system transactions.

J78 — DMA CONTROL — Basically, this slot is the same as J77 but is used only for complex designs that cannot fit on three cards.

There are two kinds of tie lines that allow communication between the interface cards: 18 general purpose tie lines connect across all four interface slots; 8 inter-slot tie lines bridge across adjacent slots. These lines are not connected to any part of the system other than the interface slots and are used by the various interfaces for card-to-card communication.

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7.4.2.1 J75 (MSB Data Latch) Slot Connections

INT = Interface
SP = Signal Processor
J28 = J28 Connector On Rear Panel Of System
ADC = A/D Converter
FP = Front Panel
UC = User Card Backplane
PS = Power Supply
RMT = Remote Control

Signal Name	Conn.	To	From	Function
DIG.GND.	J75-1		PS	Digital Ground
+5	J75-2		PS	+5 Volt Power
RMT	J75-3		FP	High When System In "Remote" Control
T4	J75-4	(Slot 76,77,78)		General Purpose Tie Line "4"
DIG IN	J75-5		FP	High When Dig Bus In "In" Mode
B2	J75-6		ADC	A/D Converter Bit 2
B4	J75-7		ADC	A/D Converter Bit 4
B6	J75-8		ADC	A/D Converter Bit 6
B8	J75-9		ADC	A/D Converter Bit 8
	J75-10			Not Used
T11	J75-11	(Slot 76,77,78)		General Purpose Tie Line "11"
	J75-12			Not Used
T13	J75-13	(Slot 76,77,78)		General Purpose Tie Line "13"
D2	J75-14	UC	UC	ANDS5400 Bidirectional Digital Bus Bit 2
D4	J75-15	UC	UC	ANDS5400 Bidirectional Digital Bus Bit 4
D6	J75-16	UC	UC	ANDS5400 Bidirectional Digital Bus Bit 6
D8	J75-17	UC	UC	ANDS5400 Bidirectional Digital Bus Bit 8
T18	J75-18	(Slot 76,77,78)		General Purpose Tie Line "18"
T19	J75-19	(Slot 76,77,78)		General Purpose Tie Line "19"
T20	J75-20	(Slot 76,77,78)		General Purpose Tie Line "20"
T21	J75-21	(Slot 76,77,78)		General Purpose Tie Line "21"
T22	J75-22	(Slot 76,77,78)		General Purpose Tie Line "22"
−15	J75-23		PS	−15 Volt Power
+15	J75-24		PS	+15 Volt Power
ANA. GND.	J75-25		PS	Analog Ground
DIG. GND.	J75-A		PS	Digital Ground
+5	J75-B		PS	+5 Volt Power
TC	J75-C	(Slot 76,77,78)		General Purpose Tie Line "C"
TD	J75-D	(Slot 76,77,78)		General Purpose Tie Line "D"
TE	J75-E	(Slot 76,77,78)		General Purpose Tie Line "E"
B1	J75-F		ADC	A/D Converter Bit 1
B3	J75-H		ADC	A/D Converter Bit 3
B5	J75-J		ADC	A/D Converter Bit 5
$\overline{B7}$	J75-K		ADC	A/D Converter Bit 7
$\overline{CAX1}$	J75-L		76-10	Inter-slot Tie Line
$\overline{TM}$	J75-M	(Slot 76,77,78)		General Purpose Tie Line "M"
$\overline{CAX2}$	J75-N		76-12	Inter-slot Tie Line
TP	J75-P	(Slot 76,77,78)		General Purpose Tie Line "P"
D1	J75-R	UC	UC	ANDS5400 Bidirectional Digital Bus Bit 1
D3	J75-S	UC	UC	ANDS5400 Bidirectional Digital Bus Bit 3
D5	J75-T	UC	UC	ANDS5400 Bidirectional Digital Bus Bit 5
D7	J75-U	UC	UC	ANDS5400 Bidirectional Digital Bus Bit 7
TV	J75-V	(Slot 76,77,78)		General Purpose Tie Line "V"
TW	J75-W	(Slot 76,77,78)		General Purpose Tie Line "W"
TX	J75-X	(Slot 76,77,78)		General Purpose Tie Line "X"
TY	J75-Y	(Slot 76,77,78)		General Purpose Tie Line "Y"
TZ	J75-Z	(Slot 76,77,78)		General Purpose Tie Line "Z"
−15	J75-AA		PS	−15 Volt Power
+15	J75-BB		PS	+15 Volt Power
ANA. GND.	J75-CC		PS	Analog Ground

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7.4.2.2 J76 (LSB Data Latch) Slot Connections

Signal Name	Conn.	To	From	Function
DIG. GND.	J76-1		PS	Digital Ground
+5	J76-2		PS	+5 Volt Power
RMT	J76-3		FP	High When In "Remote"
T4	J76-4		(Slot 75,77,78)	General Purpose Tie Line "4"
DIG IN	J76-5		FP	High When Dig Bus In "In" Mode
B10	J76-6		ADC	A/D Converter Bit 10
B12	J76-7		ADC	A/D Converter Bit 12
B14	J76-8		ADC	A/D Converter Bit 14
B16	J76-9		ADC	A/D Converter Bit 16
CAX1	J76-10		75-L	Inter-slot Tie Line
T11	J76-11		(Slot 75,77,78)	General Purpose Tie Line "11"
CAX2	J76-12		75-N	Inter-slot Tie Line
T13	J76-13		(Slot 75,77,78)	General Purpose Tie Line "13"
D10	J76-14	UC	UC	ANDS5400 Bidirect'nal Digital Bus Bit 10
D12	J76-15	UC	UC	ANDS5400 Bidirect'nal Digital Bus Bit 12
D14	J76-16	UC	UC	ANDS5400 Bidirect'nal Digital Bus Bit 14
D16	J76-17	UC	UC	ANDS5400 Bidirect'nal Digital Bus Bit 16
T18	J76-18		(Slot 75,77,78)	General Purpose Tie Line "18"
T19	J76-19		(Slot 75,77,78)	General Purpose Tie Line "19"
T20	J76-20		(Slot 75,77,78)	General Purpose Tie Line "20"
T21	J76-21		(Slot 75,77,78)	General Purpose Tie Line "21"
T22	J76-22		(Slot 75,77,78)	General Purpose Tie Line "22"
−15	J76-23		PS	−15 Volt Power
+15	J76-24		PS	+15 Volt Power
ANA. GND.	J76-25		PS	Analog Ground
DIG. GND.	J76-A		PS	Digital Ground
+5	J76-B		PS	+5 Volt Power
TC	J76-C		(Slot 75,77,78)	General Purpose Tie Line "C"
TD	J76-D		(Slot 75,77,78)	General Purpose Tie Line "D"
TE	J76-E		(Slot 75,77,78)	General Purpose Tie Line "E"
B9	J76-F		ADC	A/D Converter Bit 9
B11	J76-H		ADC	A/D Converter Bit 11
B13	J76-J		ADC	A/D Converter Bit 13
B15	J76-K		ADC	A/D Converter Bit 15
INCRA1	J76-L		77-10	Inter-slot Tie Line
TM	J76-M		(Slot 75,77,78)	General Purpose Tie Line "M"
INCRA2	J76-N		77-12	Inter-slot Tie Line
TP	J76-P		(Slot 75,77,78)	General Purpose Tie Line "P"
D9	J76-R	UC	UC	ANDS5400 Bidirect'nal Digital Bus Bit 9
D11	J76-S	UC	UC	ANDS5400 Bidirect'nal Digital Bus Bit 11
D13	J76-T	UC	UC	ANDS5400 Bidirect'nal Digital Bus Bit 13
D15	J76-U	UC	UC	ANDS5400 Bidirect'nal Digital Bus Bit 15
TV	J76-V		(Slot 75,77,78)	General Purpose Tie Line "V"
TW	J76-W		(Slot 75,77,78)	General Purpose Tie Line "W"
TX	J76-X		(Slot 75,77,78)	General Purpose Tie Line "X"
TY	J76-Y		(Slot 75,77,78)	General Purpose Tie Line "Y"
TZ	J76-Z		(Slot 75,77,78)	General Purpose Tie Line "Z"
−15	J76-AA		PS	−15 Volt Power
+15	J76-BB		PS	+15 Volt Power
ANA. GND.	J76-CC		PS	Analog Ground

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7.4.2.3 J77 (Interface Control) Slot Connections

Signal Name	Conn.	To	From	Function
DIG.GND.	J77-1		PS	Digital Ground
+5	J77-2		PS	+5 Volt Power
RMT	J77-3		FP	High When System Is In "Remote"
T4	J77-4	(Slot 75,76,78)		General Purpose Tie Line "4"
DIG IN	J77-5		FP	High When Digital Bus In "In" Mode
INCRM	J77-6	FP		Increments Address Register
RS	J77-7	FP		Range Strobe, Loads Range Register
LMAR	J77-8	FP		Loads Address Register
DIG OUT	J77-9	FP		Loads Digital Data Into User Cards
INCRA1	J77-10		76-L	Inter-slot Tie Line
T11	J77-11	(Slot 75,76,78)		General Purpose Tie Line "11"
INCRA2	J77-12		76-N	Inter-slot Tie Line
T13	J77-13	(Slot 75,76,78)		General Purpose Tie Line "13"
RUN	J77-14	FP		Locks Front Panel In "Remote"
MSR	J77-15	FP		Starts A/D Conversion
D/A!	J77-16	FP		Selects D/A Address Decoding
IN!	J77-17	FP		Puts Dig Bus In "In" Mode
T18	J77-18	(Slot 75,76,78)		General Purpose Tie Line "18"
T19	J77-19	(Slot 75,76,78)		General Purpose Tie Line "19"
T20	J77-20	(Slot 75,76,78)		General Purpose Tie Line "20"
T21	J77-21	(Slot 75,76,78)		General Purpose Tie Line "21"
T22	J77-22	(Slot 75,76,78)		General Purpose Tie Line "22"
−15	J77-23		PS	−15 Volt Power
+15	J77-24		PS	+15 Volt Power
ANA. GND.	J77-25		PS	Analog Ground
DIG. GND.	J77-A		PS	Digital Ground
+5	J77-B		PS	+5 Volt Power
TC	J77-C	(Slot 75,76,78)		General Purpose Tie Line "C"
TD	J77-D	(Slot 75,76,78)		General Purpose Tie Line "D"
TE	J77-E	(Slot 75,76,78)		General Purpose Tie Line "E"
TF	J77-F		78-F	Inter-slot Tie Line
CLR	J77-H	FP		Does General Clearing Operation
CLR1	J77-J	FP		Does Limited Clearing Operation
BSY	J77-K		SP	High During A/D Conversion
T78-10	J77-L		78-10	Inter-slot Tie Line
TM	J77-M	(Slot 75,76,78)		General Purpose Tie Line "M"
T78-12	J77-N		78-12	Inter-slot Tie Line
TP	J77-P	(Slot 75,76,78)		General Purpose Tie Line "P"
TR	J77-R		78-R	Inter-slot Tie Line
SSH	J77-S		FP	High During External SSH
A/D!	J77-T	FP		Selects A/D Address Decoding
OUT!	J77-U	FP		Puts Dig Bus In "Out" Mode
TV	J77-V	(Slot 75,76,78)		General Purpose Tie Line "V"
TW	J77-W	(Slot 75,76,78)		General Purpose Tie Line "W"
TX	J77-X	(Slot 75,76,78)		General Purpose Tie Line "X"
TY	J77-Y	(Slot 75,76,78)		General Purpose Tie Line "Y"
TZ	J77-Z	(Slot 75,76,78)		General Purpose Tie Line "Z"
−15	J77-AA		PS	−15 Volt Power
+15	J77-BB		PS	+15 Volt Power
REQ OUT	J77-CC		UC	High During User Card Interrupt

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7.4.2.4 J78 (DMA Control) Slot Connections

Signal Name	Conn.	To	From	Function
DIG.GND.	J78-1		PS	Digital Ground
+5	J78-2		PS	+5 Volt Power
RMT	J78-3		FP	High When System Is In "Remote"
T4	J78-4	(Slot 75,76,77)		General Purpose Tie Line "4"
DIG IN	J78-5		FP	High When Digital Bus In "In" Mode
INCRM	J78-6	FP		Increments Address Register
RS	J78-7	FP		Range Strobe, Loads Range Register
LMAR	J78-8	FP		Loads Address Register
DIG OUT	J78-9	FP		Loads Digital Data Into User Cards
T78-10	J78-10		77-L	Inter-slot Tie Line
T11	J78-11	(Slot 75,76,77)		General Purpose Tie Line "11"
T78-12	J78-12		77-N	Inter-slot Tie Line
T13	J78-13	(Slot 75,76,77)		General Purpose Tie Line "13"
RUN	J78-14	FP		Locks Front Panel In "Remote"
MSR	J78-15	FP		Starts A/D Conversion
D/A!	J78-16	FP		Selects D/A Address Decoding
IN!	J78-17	FP		Puts Dig Bus In "In" Mode
T18	J78-18	(Slot 75,76,77)		General Purpose Tie Line "18"
T19	J78-19	(Slot 75,76,77)		General Purpose Tie Line "19"
T20	J78-20	(Slot 75,76,77)		General Purpose Tie Line "20"
T21	J78-21	(Slot 75,76,77)		General Purpose Tie Line "21"
T22	J78-22	(Slot 75,76,77)		General Purpose Tie Line "22"
−15	J78-23		PS	−15 Volt Power
+15	J78-24		PS	+15 Volt Power
ANA. GND.	J78-25		PS	Analog Ground
DIG. GND.	J78-A		PS	Digital Ground
+5	J78-B		PS	+5 Volt Power
TC	J78-C	(Slot 75,76,77)		General Purpose Tie Line "C"
TD	J78-D	(Slot 75,76,77)		General Purpose Tie Line "D"
TE	J78-E	(Slot 75,76,77)		General Purpose Tie Line "E"
$\overline{TF}$	J78-F		77-F	Inter-slot Tie Line
$\overline{CLR}$	J78-H	FP		Does General Clearing Operation
$\overline{CLR1}$	J78-J	FP		Does Limited Clearing Operation
BSY	J78-K		SP	High During A/D Conversion
	J78-L			Not Used
TM	J78-M	(Slot 75,76,77)		General Purpose Tie Line "M"
	J78-N			Not Used
TP	J78-P	(Slot 75,76,77)		General Purpose Tie Line "P"
TR	J78-R		77-R	Inter-slot Tie Line
SSH	J78-S		FP	High During External SSH
A/D!	J78-T	FP		Selects A/D Address Decoding
OUT!	J78-U	FP		Puts Dig Bus In "Out" Mode
TV	J78-V	(Slot 75,76,77)		General Purpose Tie Line "V"
TW	J78-W	(Slot 75,76,77)		General Purpose Tie Line "W"
TX	J78-X	(Slot 75,76,77)		General Purpose Tie Line "X"
TY	J78-Y	(Slot 75,76,77)		General Purpose Tie Line "Y"
TZ	J78-Z	(Slot 75,76,77)		General Purpose Tie Line "Z"
−15	J78-AA		PS	−15 Volt Power
+15	J78-BB		PS	+15 Volt Power
REQ OUT	J78-CC		UC	High During User Card Interrupt

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Interface Index

Interface Number	Title and Requirements	Slot
– 02	Nova DMA/PIO Interface	
	Control Card AC404	(J77)
	DMA Card AC405	(J78)
	Data Latch Cards AC403	(J75 and J76)
– 13	IEEE 488-1975 Standard Bus Interface	
	Control Card AC409	(J77)
	MSB Data Latch Card AC407	(J75)
	LSB Data Latch Card AC408	(J76)
– 18	LSI-11 DMA/PIO Interface	
	DC7010 DMA Interface 1 Quad Slot in Q Bus Backplane	
	Buffered Control Line Interface	(See – 19 Interface)
– 19A/B	Buffered Control Line Interface	
	Control Card AC463	(J77)
	Data Latch Cards AC470	(J75 and J76)
– 23 A/B to – 29 A/B, and – 32 A/B, – 34 A/B, and – 35 A/B	General Purpose Interface	
	Control Card AC471	(J77)
	Data Latch Cards AC470	(J75 and J76)
– 30, – 36, and – 37	Serial Line Interface	
	Control Card AC476	(J77)
	UART Card AC475	(J76)
	Data Latch Card AC474	(J75)
	R/T Card AC477	(J78)
– 31	PDP-11 DMA/PIO Interface	
	AC472 PIO and AC473 DMA Cards 2 Quad Slots in Unibus Backplane	
	Buffered Control Line Interface	(See – 19 Interface)

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Section 7.4
Interfaces

Card Number	Drawing Number	Title
—	—	– 02 DMA/PIO Nova Interface Data Sheet
AC403-XX	D5-7500	Nova Data Latch Schematic
AC403-XX	D7-7500	Nova Data Latch Board Assembly
AC404	D5-7501	Nova Control Board Schematic
AC404	D7-7501	Nova Control Board Assembly
AC405	D5-7502	Novatrol 80 Schematic
AC405	D7-7502	Novatrol 80 Assembly
—	C7-2300	Nova Interface W2 Connector Assembly (– 02 Interface)
—	C5-8604	Novatrol Cable Board No. 1 Wiring Table
—	C4-8604	Novatrol Cable Board No. 1 Drilling
—	C5-8605	Novatrol Cable Board No. 2 Wiring Table
—	C4-8605	Novatrol Cable Board No. 2 Drilling
—	—	– 18 DEC LSI-11 Interface Data Sheet
DC7010	D5-8612 (2 sheets)	LSI-11 Interface Board Schematic
DC7010	D7-8612	LSI-11 Interface Board Assembly
—	—	– 19 Buffered Control Interface Data Sheet
AC463	C5-8639	– 19 Interface Control Card Schematic
AC463	D7-8639	– 19 Interface Control Card Assembly
AC470-XX	C5-8678	Universal Interface Data Card Schematic
AC470	D7-8678	Universal Interface Data Card Assembly
—	C7-2352	W2 Interface Cable Assembly (– 19 Interface)
—	C7-2342	Interface, Internal 20 Conductor Cable Assembly
—	C7-2343	Interface, Internal 20 Conductor Cable Assembly
—	—	General Purpose Interface Data Sheet
AC471	C5-8679	Parallel Interface Control Card Schematic
AC471	D7-8679	Parallel Interface Control Card Assembly
—	C7-2387	W2 Interface Cable Assembly (– 23 A/B etc. Interfaces)
—	C7-2389	Cable Assembly
—	C7-2390	Cable Assembly

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Section 7.4
Interfaces (Continued)

Card Number	Drawing Number	Title
—	—	– 30, – 36 and – 37 Asynchronous Serial Line Interfaces Data Sheet
AC474	C5-8682	Data Latch Board Serial Line Interface Schematic
AC474	D7-8682	Data Latch Board Serial Line Interface Assembly
AC475	C5-8683	Asynchronous Serial Line Interface UART Card Schematic
AC476	C5-8684	Asynchronous Serial Line Interface Control Card Schematic
AC476	D7-8684	Asynchronous Serial Line Interface Control Card Assembly
AC477	C5-8685	Asynchronous Serial Line Interface R/T Card Schematic
AC477	D7-8685	Asynchronous Serial Line Interface R/T Card Assembly
—	C7-2308	W2 Connector Interface (ASI) Cable Assembly (– 30 etc. Interfaces)
—	—	– 31 DMA/PIO PDP-11 Interface Data Sheet
AC473	D5-8681 (2 sheets)	PDP-11 PIO Interface with 54 RQST Schematic
AC473	D7-8681	PDP-11 PIO Interface with 54 RQST Assembly
AC472	D5-8680 (2 sheets)	PDP-11 DMA Interface with 54 RQST Schematic
AC472	D7-8680	PDP-11 DMA Interface with 54 RQST Assembly
—	C7-2395	PDP-11 Interface External 34 Conductor P4 Cable Assembly
—	C7-2394	PDP-11 Interface External 20 Conductor P3 Cable Assembly
—	C7-2393	PDP-11 Interface External 20 Conductor P2 Cable Assembly
—	—	– 13 IEEE 488-1975 Interface Data Sheet
AC407	C5-7516	IEEE – MSB Schematic
AC407	D7-7516	IEEE – MSB Assembly
AC408	C5-7517	IEEE – LSB Schematic
AC408	D7-7517	IEEE – LSB Assembly
AC409	D5-7518	IEEE Control Schematic
AC409	D7-7518	IEEE Control Assembly
—	C7-2307	W2 IEEE Connector Interface Cable Assembly (– 13 Interfaces)

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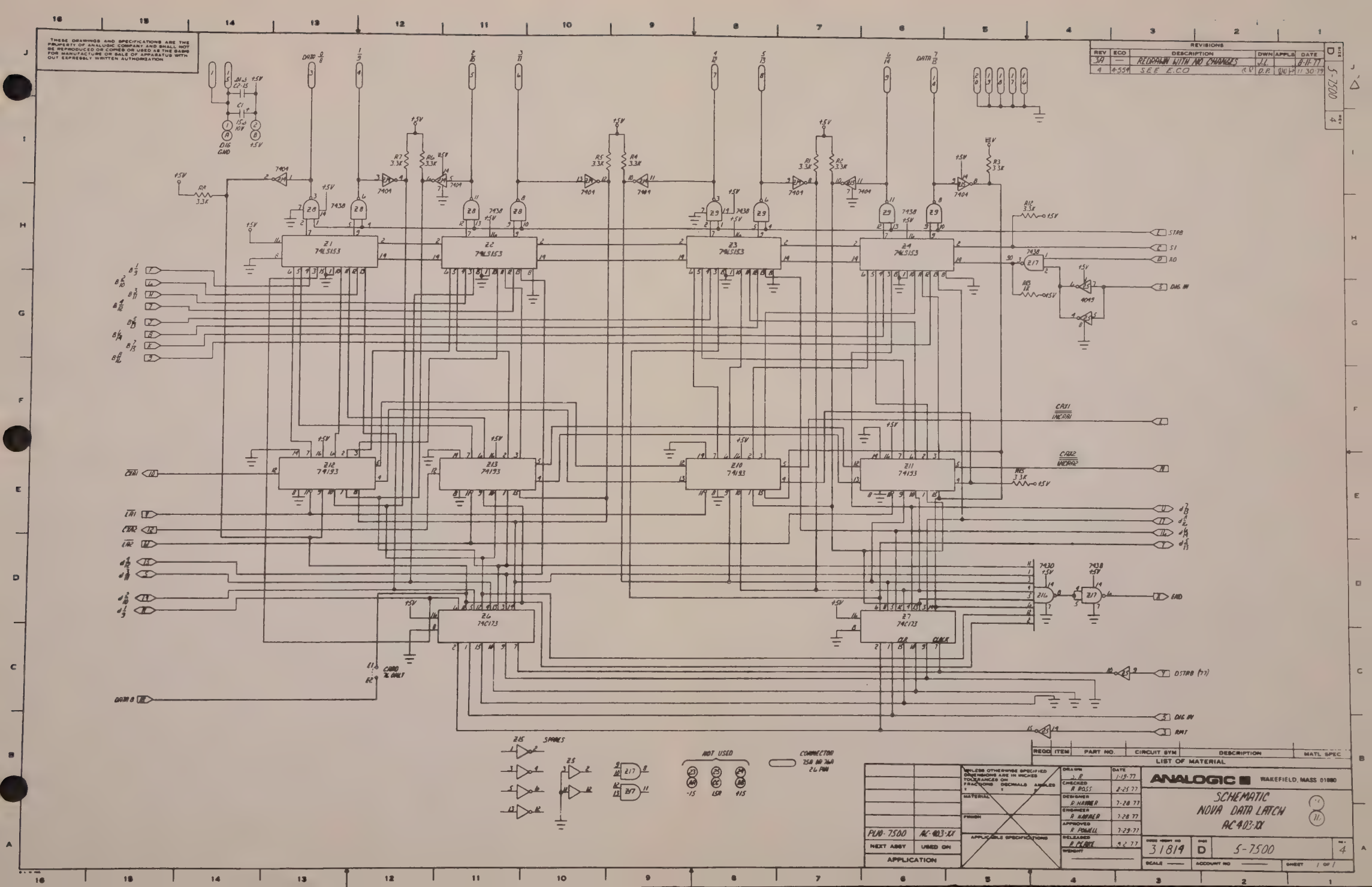
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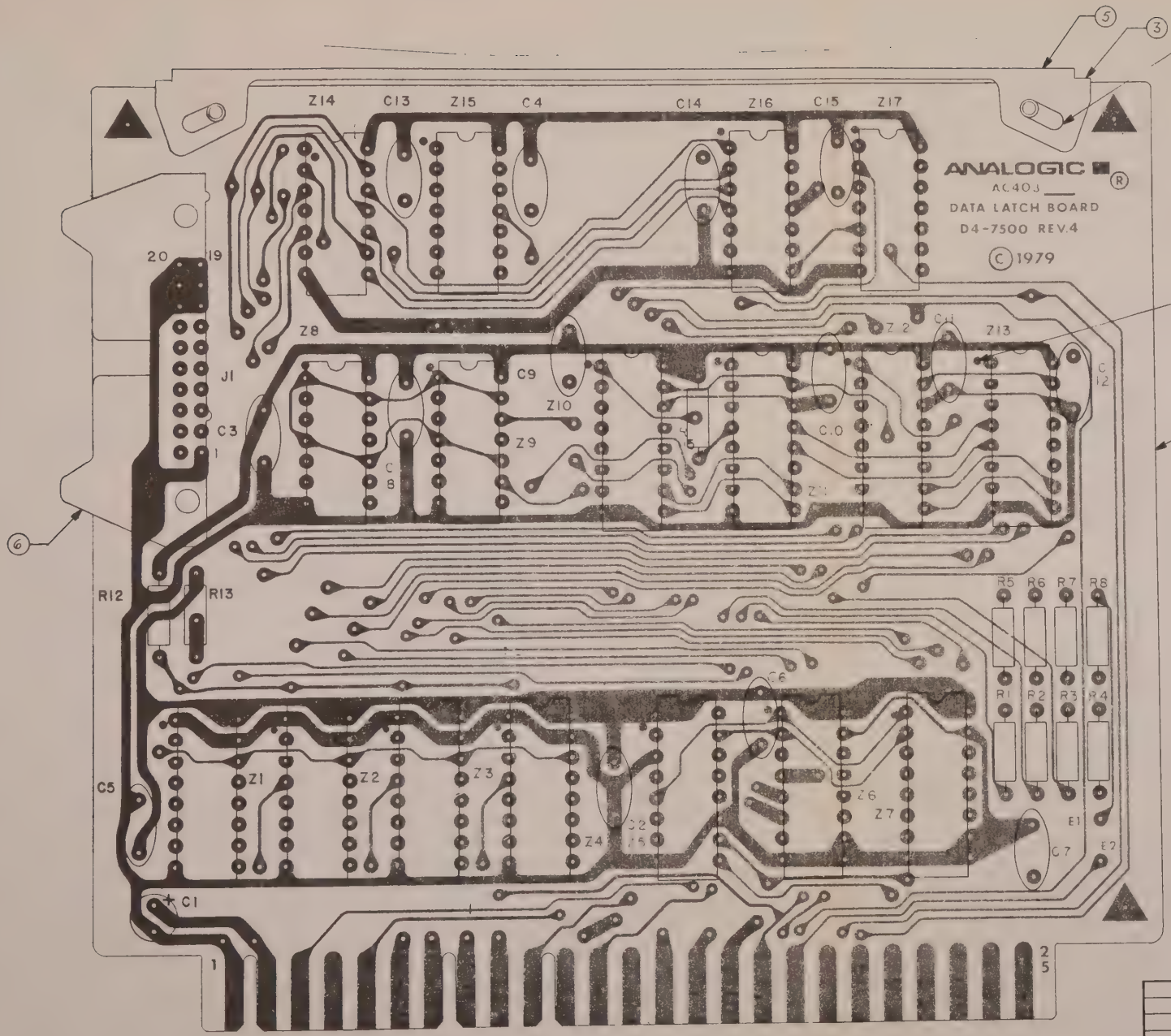
REVISIONS
REV ECO DESCRIPTION DWN APPR DATE
SA — REDRAWN WITH NO CHANGES JL 2-11-77
4 4-554 SEE E.C.O. JL DR 11 30 79
SIZE D 5-7500 REV 4
21 74LS153
22 74LS153
23 74LS153
24 74LS153
212 74193
213 74193
210 74193
211 74193
26 74C173
27 74C173
7404
7409
7438
7430
217
4049
214
STRB
S1
S0
DIG IN
CAY1 INCAR1
CAY2 INCAR2
CARRY
BAD
DSTRB (T1)
DIG IN
RMT
CARRY OUT
DATA 0
SPARES
NOT USED
CONNECTOR 25D RC 26A 26 PIN
PLN0-7500
AC-403-XX
NEXT ASSY
USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN J. R. 1-19-77
CHECKED R. ROSS 2-25-77
DESIGNER P. HAMMER 1-28-77
ENGINEER R. HAMFELD 1-28-77
APPROVED R. POWELL 3-29-77
RELEASED R. CLARK 9-2-77
WEIGHT
ANALOGIC WAKEFIELD, MASS 01880
SCHEMATIC
NOVA DATA LATCH
AC403-XX
SIZE D 5-7500 REV 4
SCALE — SHEET 1 OF 1
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL

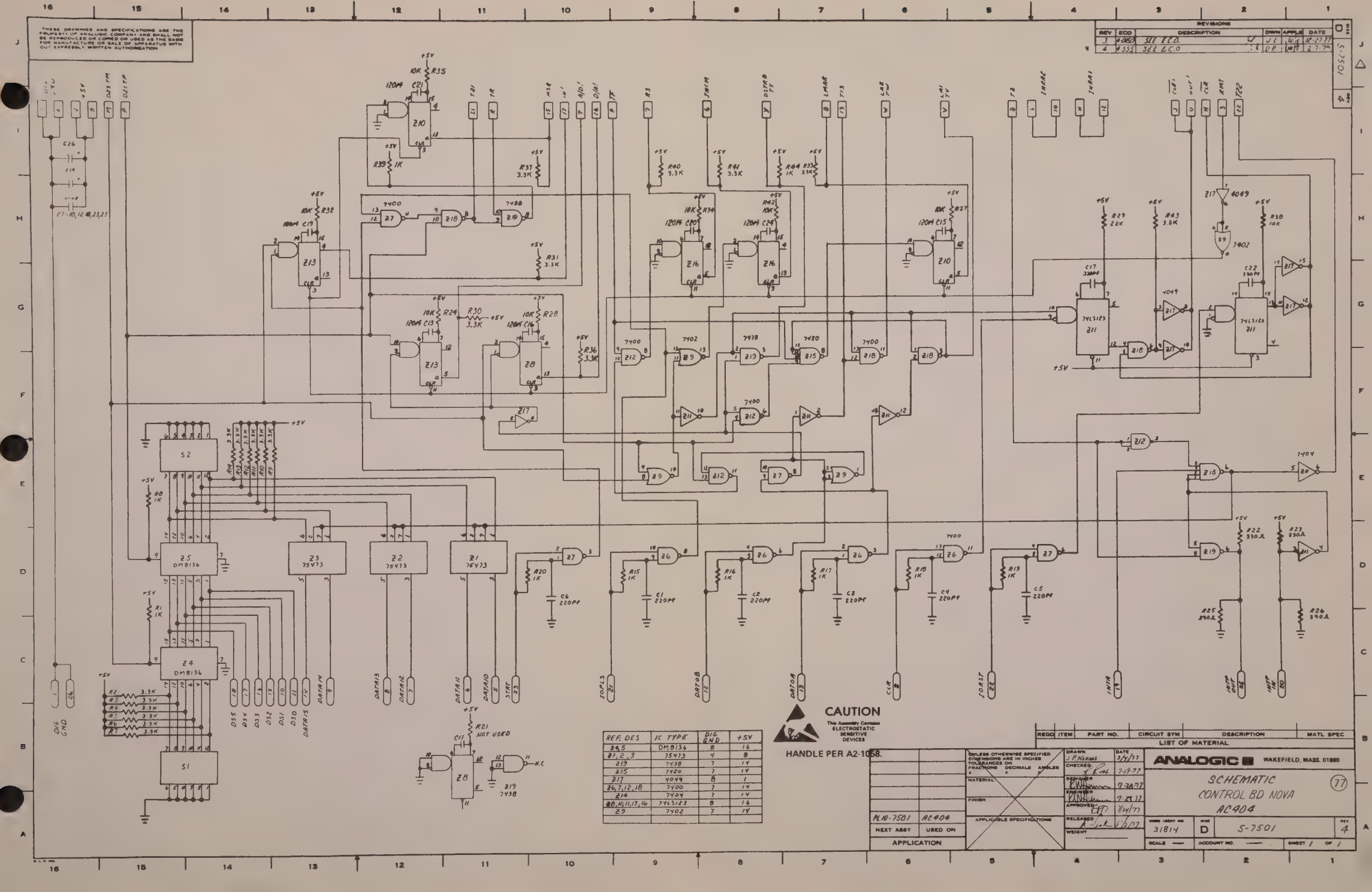


REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPL'D	DATE
4	4354	SEE ECO	RC	DP	11-30-77

NOTES:
1. FOR SCHEMATIC SEE D5-7500.
2. DOTS INDICATE PIN 1 OF I.C.'S.
3. ASSEMBLE IN ACCORDANCE WITH A2-1027.

COMPONENT SIDE

		"THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF ANALOGIC CO. AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION FROM ANALOGIC CO."	DRAWN J. FLANAGAN 2-25	ANALOGIC WAKEFIELD, MASS. 01880	
			CHECKED R. ROSS 2-25-77	ASSEMBLY DATA LATCH BOARD AC 403-XX	
			DESIGNER R. HAVENER 7-28-77		
			ENGINEER R. HAVENER 7-29-77		
P.C.B. 7500	AC 403-XX		APPROVED R.F.P. 7-29-77	CODE IDENT NO. 31814	SIZE D 7-7500 REV 4
NEXT ASSY	USED ON		RELEASED R. PEAKE 8-2-77	SCALE 4:1	ACCOUNT NO. SHEET 1 OF 1
APPLICATION			WEIGHT		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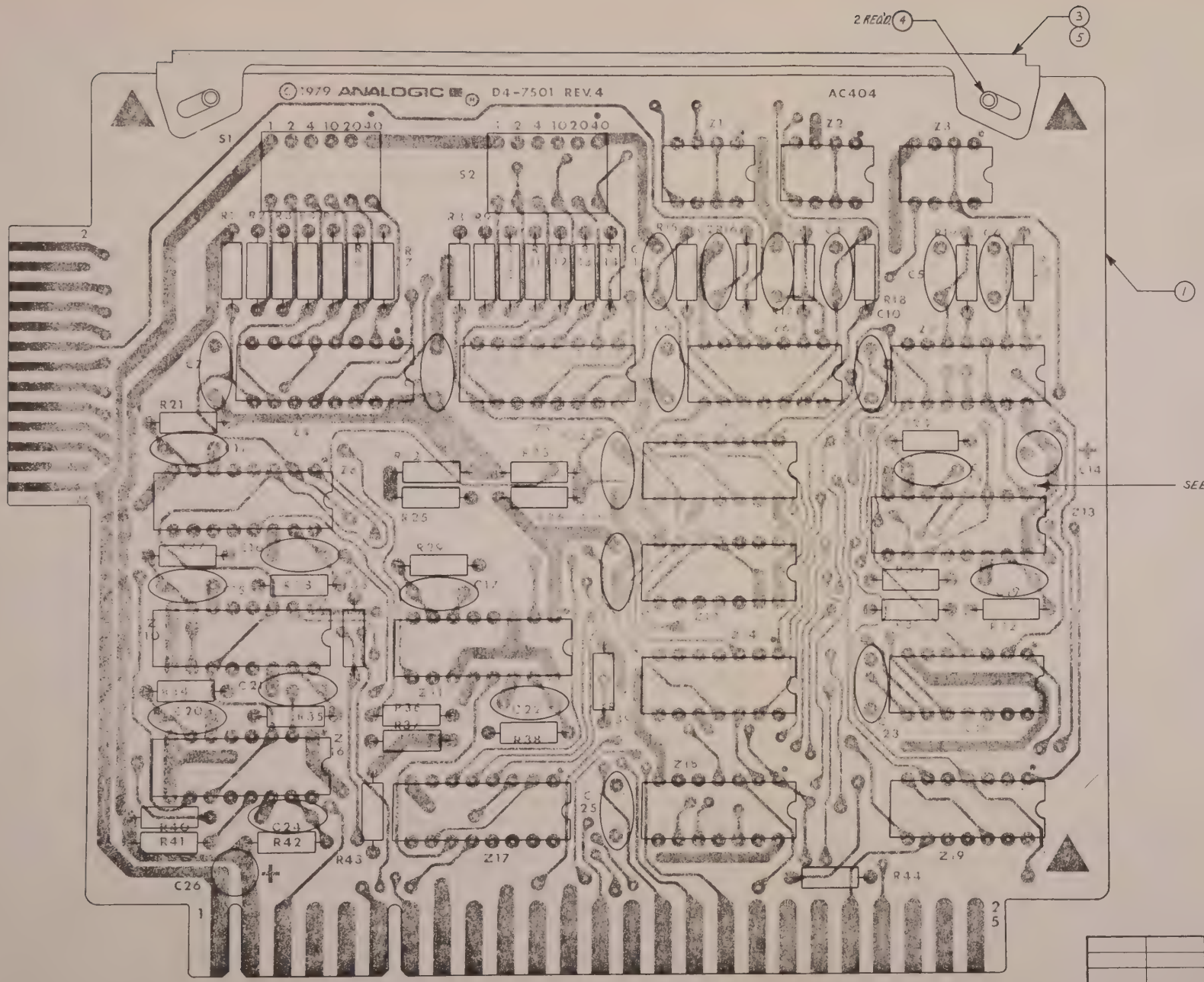
REVISIONS
REV ECO DESCRIPTION DWN APPR DATE
3 4083 SEE E.C.O. JJ WH 12-27-77
4 4355 SEE E.C.O. JJ DP WH 2-7-78
S-7501
CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
REF. DES | IC TYPE | DIG GND | +5V
Z4,5 | DM8136 | 8 | 16
Z1,2,3 | 75473 | 4 | 8
Z19 | 7438 | 7 | 14
Z15 | 7420 | 7 | 14
Z17 | 4049 | 8 | 1
Z6,7,12,18 | 7400 | 7 | 14
Z14 | 7404 | 7 | 14
Z9,10,11,13,16 | 74LS123 | 8 | 16
Z9 | 7402 | 7 | 14
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL
PLN-7501 AC404
NEXT ASSY USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN J.P.Kearns 3/14/77
CHECKED 7-19-77
DESIGNER 7-28-77
ENGINEER 7-28-77
APPROVED 7/14/77
RELEASED 8/2/77
WEIGHT
ANALOGIC WAKEFIELD, MASS. 01880
SCHEMATIC
CONTROL BD NOVA
AC404
(77)
DWG IDENT NO 31814
SIZE D
S-7501
REV 4
SCALE —
ACCOUNT NO. —
SHEET 1 OF 1



REVISIONS						
REV.	E.C.O.	DESCRIPTION	DWN	APP'D	DATE	
4	4-355	SEE E.C.O.	RP	D.P.	12-7-77	

D 7-7501 4

NOTES:
1. FOR SCHEMATIC SEE D5-7501.
2. DOTS INDICATE PIN 1 OF I.C.'S & SWITCHES.
3. ASSEMBLE PER A2-1027.

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

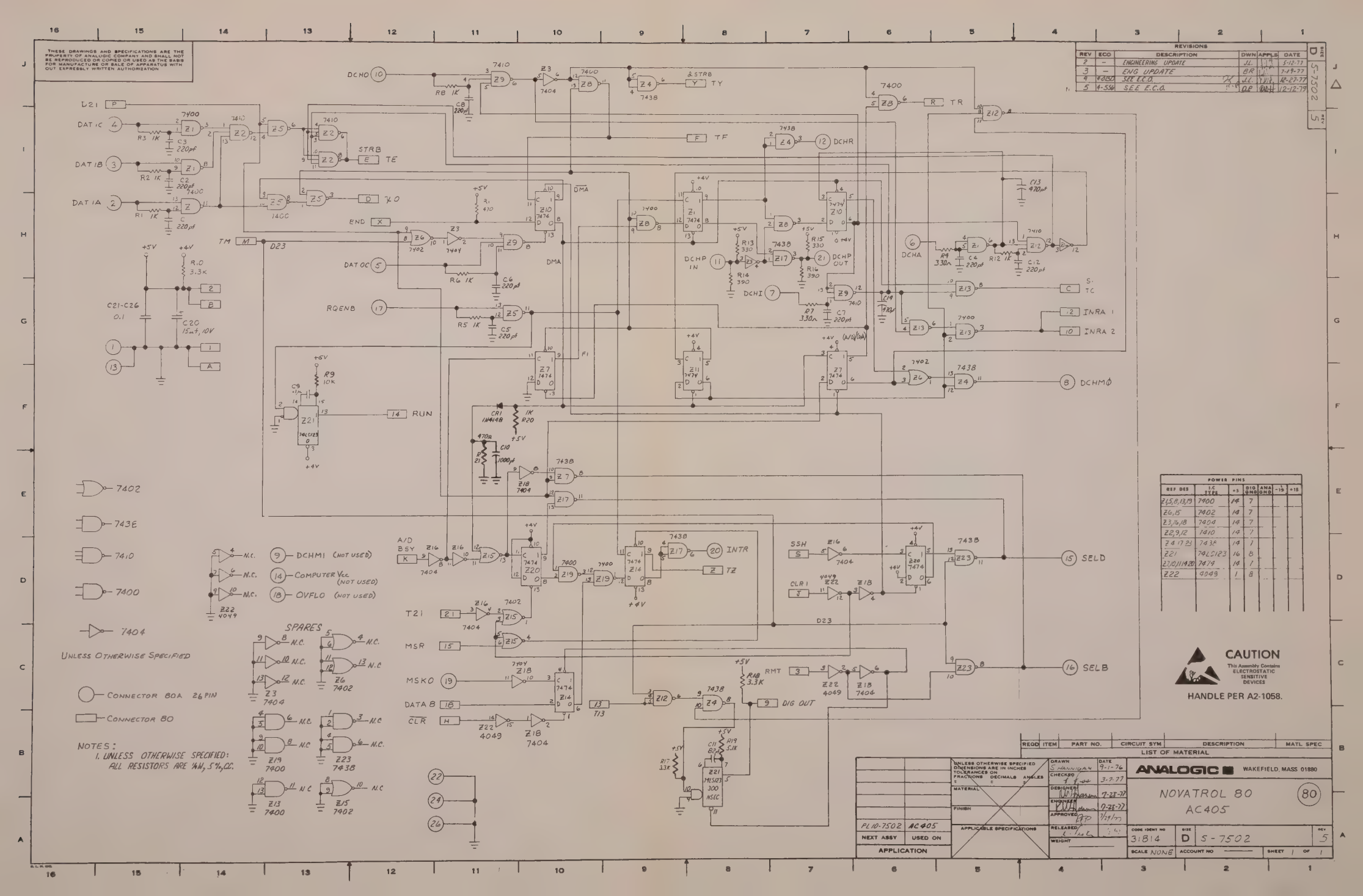
COMPONENT SIDE

		DRAWN	W. LASPINA	6-23-77
		CHECKED	R. ROSS	7-19-77
		DESIGNED	R. HAVENER	7-23-77
		ENGINEER	R. HAVENER	7-23-77
		APPROVED	R. POWELL	7-29-77
PL10-7501	AC404	RELEASED	R. PEAKE	8-2-77
NEXT ASSY	USED ON	WEIGHT		
APPLICATION				

ANALOGIC WAKEFIELD, MASS. 01880

ASSEMBLY
CONTROL BOARD NOVA (77)
AC 404

CODE IDENT NO	SIZE		REV
31814	D	7-7501	4
SCALE 4:1	ACCOUNT NO.		SHEET 2 OF 4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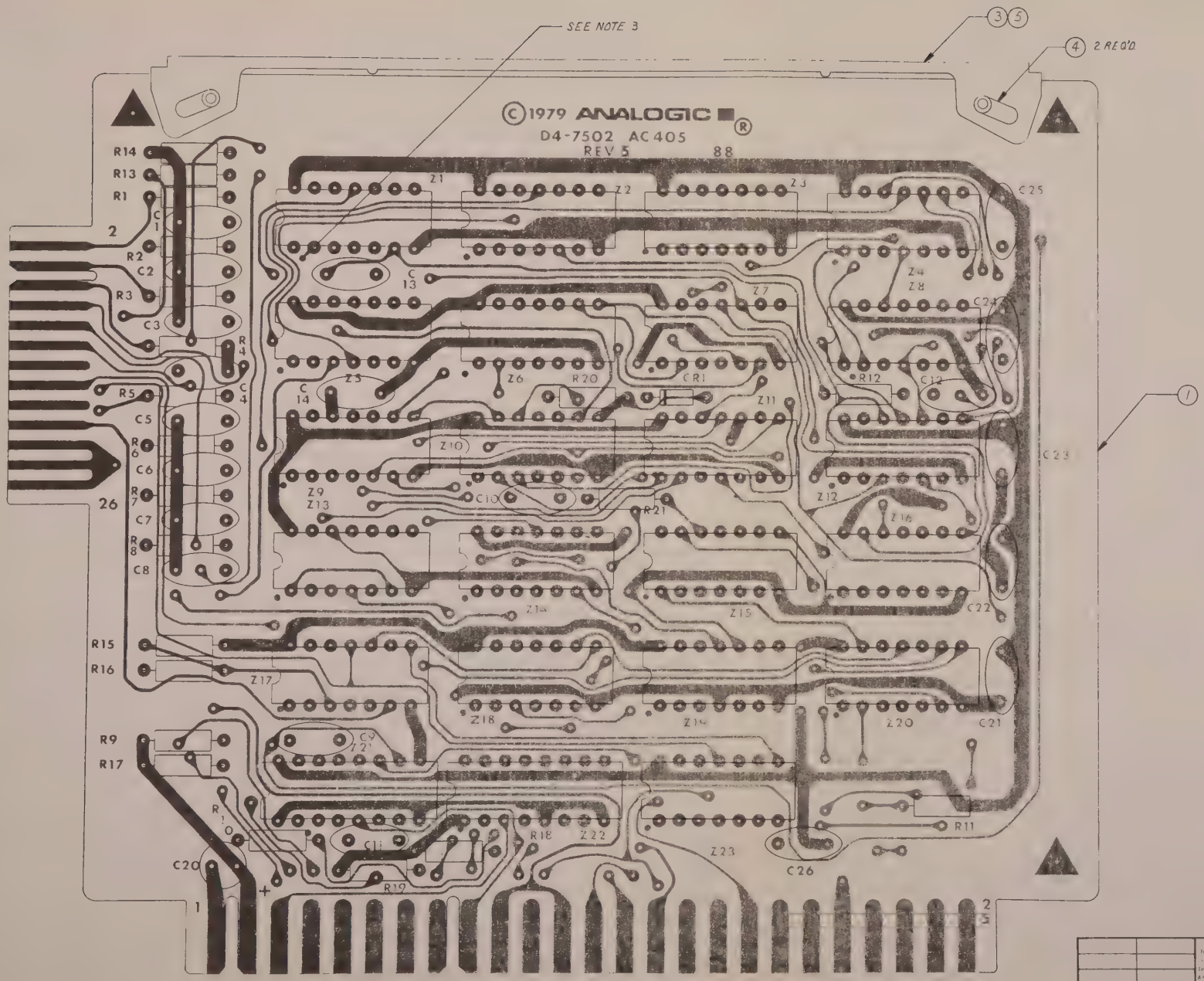
REVISIONS
REV ECO DESCRIPTION DWN APPD DATE
2 – ENGINEERING UPDATE JL 5-12-77
3 – ENG UPDATE BR 7-19-77
4 4010 SEE E.C.O. JL 12-27-77
5 14-556 SEE E.C.O. DP 12-12-79
D S-7502 5
DCH0 10
RB 1K
C8 220pf
7410
Z3
7400
Z8
Z4
7438
&STRB
Y TY
7400
Z8
R TR
F TF
7438
Z4
12 DCHR
DAT1C 4
DAT1B 3
DAT1A 2
R3 1K
C3 220pf
R2 1K
C2 220pf
R1 1K
C 220pf
7400
Z1
Z2
Z5
7410
Z3
Z2
STRB
E TE
Z5
1400
D YO
+5V
R1 430
DMA
Z10
7474
END X
TM M
D23
Z6
7402
Z3
7404
Z9
DAT0C 5
R6 1K
C6 220pf
RQENB 17
R5 1K
C5 220pf
Z5
F1
Z7
7474
+4V
R10 3.3K
C21-C26 0.1
C20 15uf, 10V
2 B
1 I
13 A
+5V
R9 10K
C9 47p
Z21
74LS123
14 RUN
CR1 IN4148
1K R20
470Ω
C10 1000pf
Z18 7404
7438
Z7
Z17
A/D BSY K
Z16
7404
Z15
7400
Z19
7400
Z19
7438
Z17
20 INTR
Z TZ
Z20
7474
T2i 2
7402
Z15
MSR 15
MSK0 19
DATA B 18
CLR H
7404
Z16
Z22
4049
Z18
7404
7400
Z18
Z14
7474
13 T13
7438
Z12
Z4
RMT 3
R18 3.3K
9 DIG OUT
Z22
4049
Z18
7404
+5V
R17 33K
C11 82
R19 5.1K
Z21
MIS123
300
NSIC
22
24
26
SSH S
Z16
7404
CLR1 J
4049
Z22
Z18
Z20
7476
7438
Z23
15 SELD
16 SELB
DCHA 6
R9 330Ω
C4 220pf
R12 1K
C12 220pf
7410
Z12
DCHP IN 11
DCHI 7
R13 330
R14 390
R15 330
R16 390
7438
Z17
DCHP OUT 21
R7 330Ω
C7 220pf
Z9
7410
C13 470pf
Z13
7400
C TC
12 INRA 1
10 INRA 2
7402
Z6
7438
Z4
8 DCHMØ
7402
7438
7400
7410
7404
7400
UNLESS OTHERWISE SPECIFIED
N.C.
9 DCHM1 (NOT USED)
14 COMPUTER Vcc (NOT USED)
18 OVFLO (NOT USED)
Z22 4049
SPARES
Z3 7404
Z6 7402
Z19 7400
Z23 7438
Z13 7400
Z15 7402
CONNECTOR 80A 26 PIN
CONNECTOR 80
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W, 5%, CC.
POWER PINS
REF DES IC TYPES +5 DIG GND ANA GND -15 +15
1,5,8,13,19 7400 14 7
6,15 7402 14 7
3,16,18 7404 14 7
2,9,12 7410 14 7
4 17 23 7438 14 1
21 74LS123 16 8
27,10,11,420 7474 14 1
22 4049 1 8
CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN S. MANIGAN 9-1-76
CHECKED 3-7-77
DESIGNER 7-25-77
ENGINEER 9-28-77
APPROVED 7/7/77
RELEASED
WEIGHT
PL10-7502 AC405
NEXT ASSY USED ON
APPLICATION
ANALOGIC WAKEFIELD, MASS 01880
NOVATROL 80 (80)
AC405
CODE IDENT NO 31814
SIZE D S-7502 REV 5
SCALE NONE ACCOUNT NO SHEET 1 OF 1



REVISIONS

	DESCRIPTION	DWN	APPD	DATE
5	4-556	SEE E.C.O.		

D 7-7502 5

NOTES:
1. FOR SCHEMATIC SEE D5-7502.
2. ASSEMBLE PER A2-1027.
3. DOTS INDICATE PIN 1 OF I.C.'S.

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

COMPONENT SIDE

DRAWN	J.FLANAGAN	3-4-77	ANALOGIC ■ WAKEFIELD, MASS. 01880	
CHECKED	K.ROSE	3-1-77	ASSEMBLY NOVATROL AC 405	80
DESIGNED	R.HAVENER	7-28-77		
ENGINEER	R.HAVENER	7-28-77		
APPROVED	R.POWELL	7-29-77		
RELEASED	R.PEANE	8-2-77		
WEIGHT				

PL10-7502 AC 405
NEXT ASSY | USED ON
APPLICATION

CODE IDENT NO	SIZE	DRAWING NO	REV
31814	D	7-7502	5
SCALE 4:1	ACCOUNT NO.	SHEET 1 OF 1	

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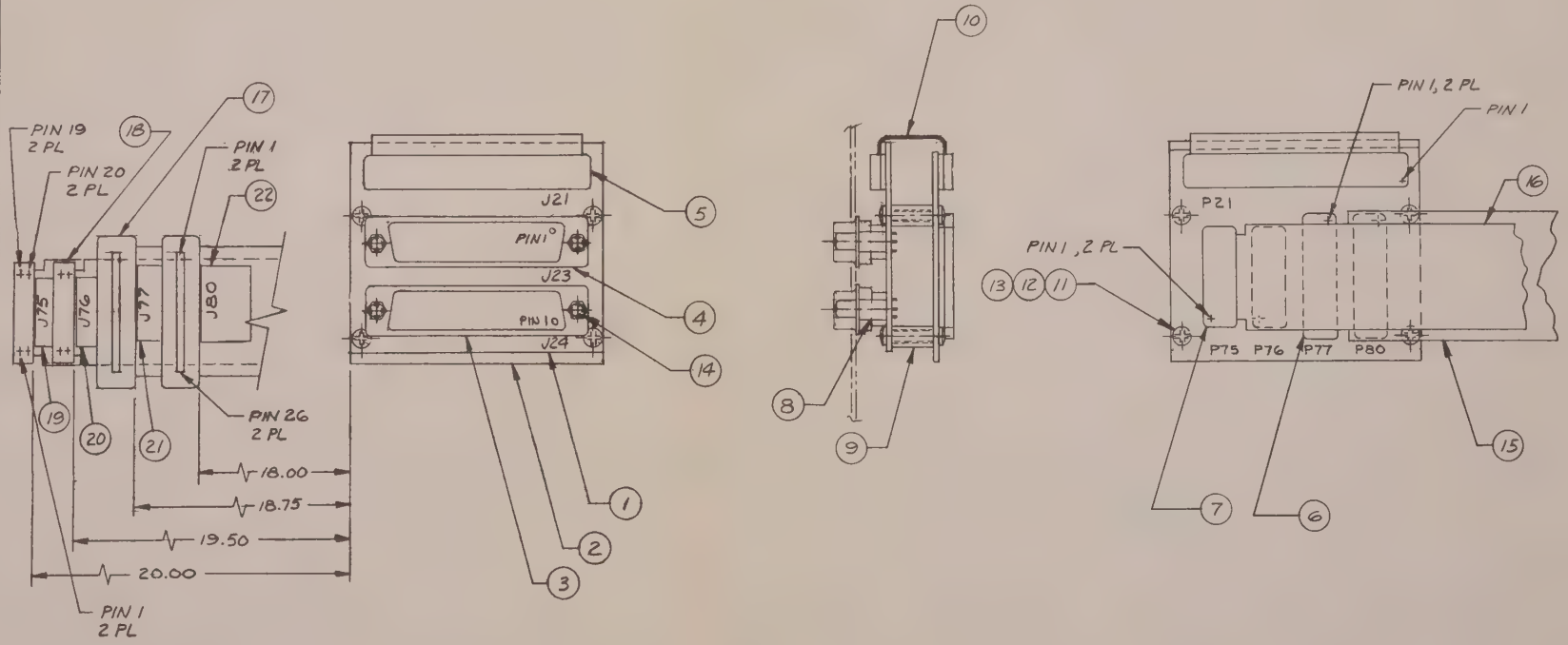
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1		ITEM 2 SHORTENED 3/4"	N.C.		7-15-77
2	4-580 4-581	SEE ECO.'S	RB		5/17/80

SIZE C | 7-2300 | REV 2



NOTES

1. SWAGE ITEM 8 TO ITEM 1 USING CAMBION TOOLS #435-6491-02 AND #435-6612-01 OR EQUIV

PL10-3700	AN5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± XX ± XXX ±
ANGLES

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

WEIGHT

		DATE
DRAWN	N. CARTER	6-3-77
CHECKED		15/6/77
ENGINEER		7-28-77
ENGINEERING MGR.		7-28-77
QUALITY CONTROL		7/29/77
PRODUCTION		8/1/77

ANALOGIC. WAKEFIELD, MASS. 01880

CONNECTOR ASSY-W2
(NOVA INTERFACE)

CODE IDENT NO	SIZE		REV
31814	C	7-2300	2
SCALE 1/1		SHEET 1 OF 1	

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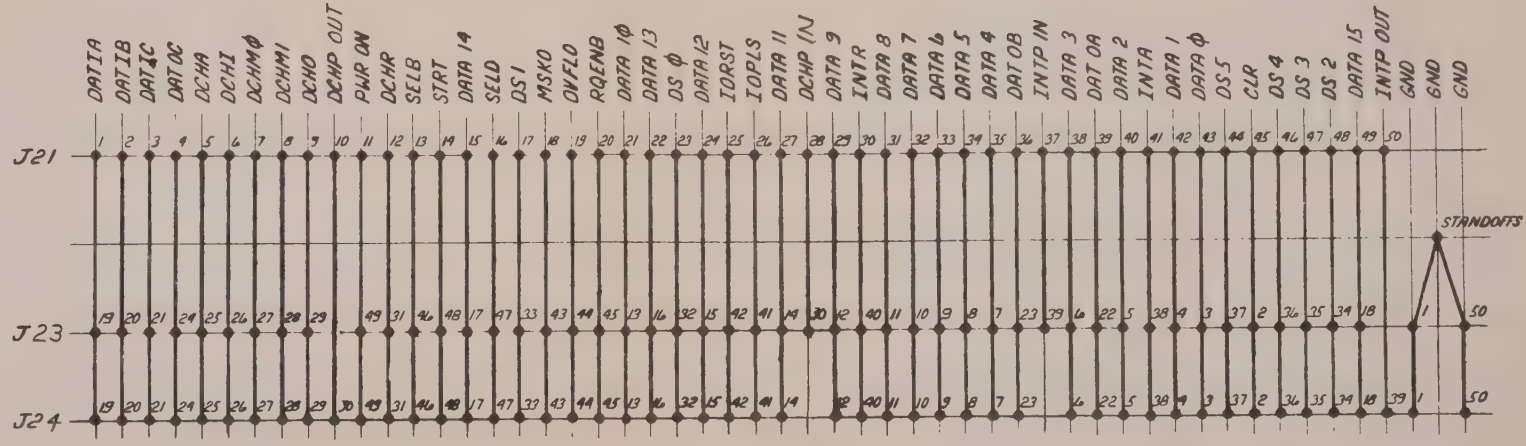
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APP'D	DATE
1	–	ENG. UPDATE			7/27/77
2	4-580	SEE ECO.			4/7/80

SIZE C | 5-8604 | REV 2



PL10-3700	AN5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .XX ± .01 .XXX ± .005 ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	J. LASPINA	6-21-77
CHECKED		7-27-77
ENGINEER		7-28-77
ENGINEERING MGR.		7-28-77
QUALITY CONTROL		7/29/77
PRODUCTION		8/5/77
WEIGHT		

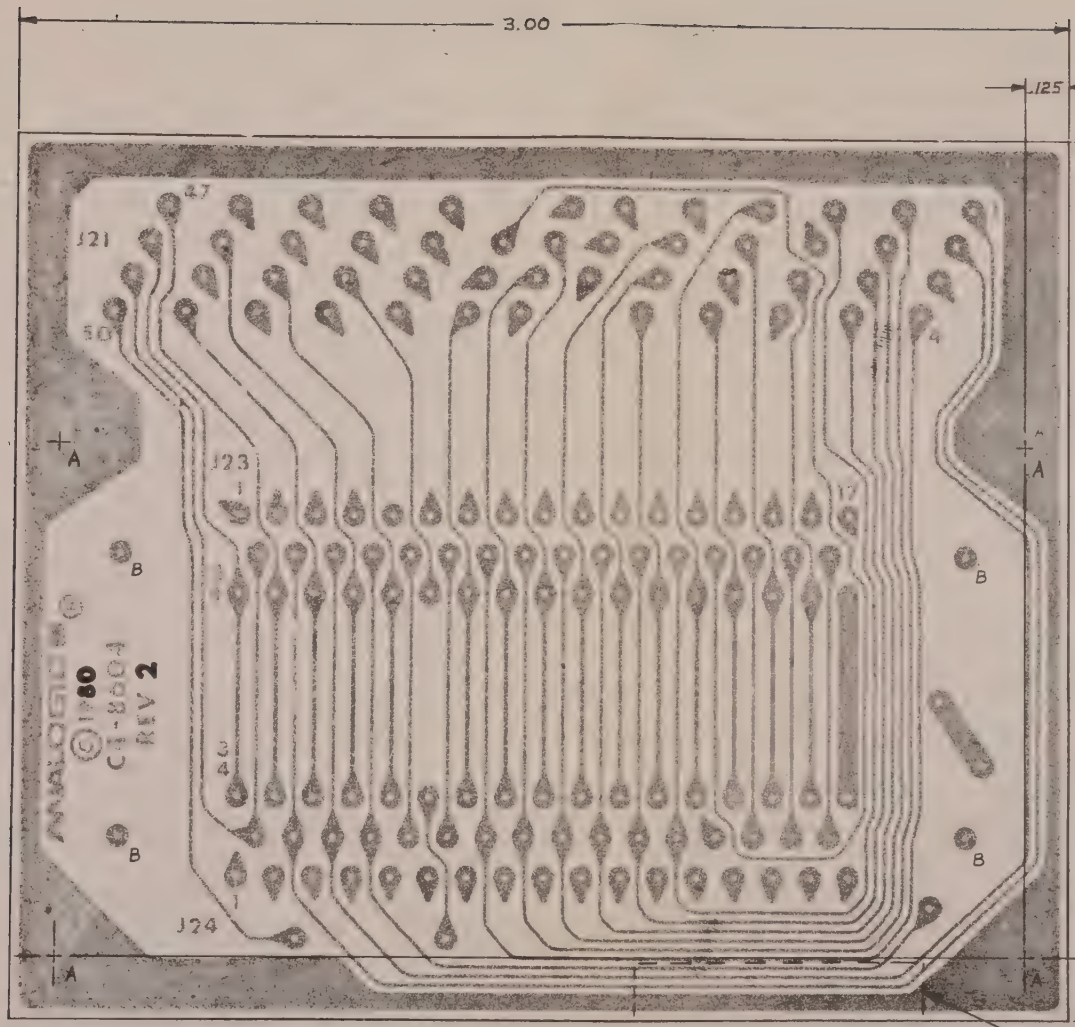
ANALOGIC WAKEFIELD, MASS. 01880

WIRING TABLE NOVATROL CABLE BOARD NO. 1

CODE IDENT NO	SIZE		REV
31814	C	5-8604	2
SCALE			SHEET 1 OF 1

REV	ECO	DESCRIPTION	DWN	APPD	DATE
1	-	ENG. UPDATE			7/27/77
2	4-580	SEE E.C.O.	R.K.	W.B.	9/29/80

4-8604 2



NOTES:(CONT.)

6. P.C. BOARD SHALL BE UL. APPROVED AND MARKED WITH UL. CODE IDENTIFICATION AND THE FLAMMABILITY RATING, EITHER UL-94V-0 OR UL-94V-02 (DEPENDING ON MATERIAL USED)

PUT UL. MARKING IN THIS AREA ONLY (WIRING SIDE) SEE NOTE 6

NOTES:

1. MATERIAL: GLASS EPOXY (~~FR4~~) DOUBLE SIDED 2 OZ. COPPER, GREEN, .062 THICK.
2. SOLDER TIN PLATE (60/40) WITH THICKNESS OF .0005 TO .0010.
3. UNLESS OTHERWISE SPECIFIED ALL HOLES ARE PLATED THRU.

UNMARKED HOLES	.039-.045 DIA. AFTER PLATING	
A HOLES	.130 DIA. AFTER PLATING	4 REQ'D.
B HOLES	.187 +.000 -.003 DIA. DO NOT PLATE CSK 120° TO .200 DIA.	4 REQ'D.

4. FABRICATE PER A2-1040.
5. FOR ASSEMBLY SEE C7-2300.

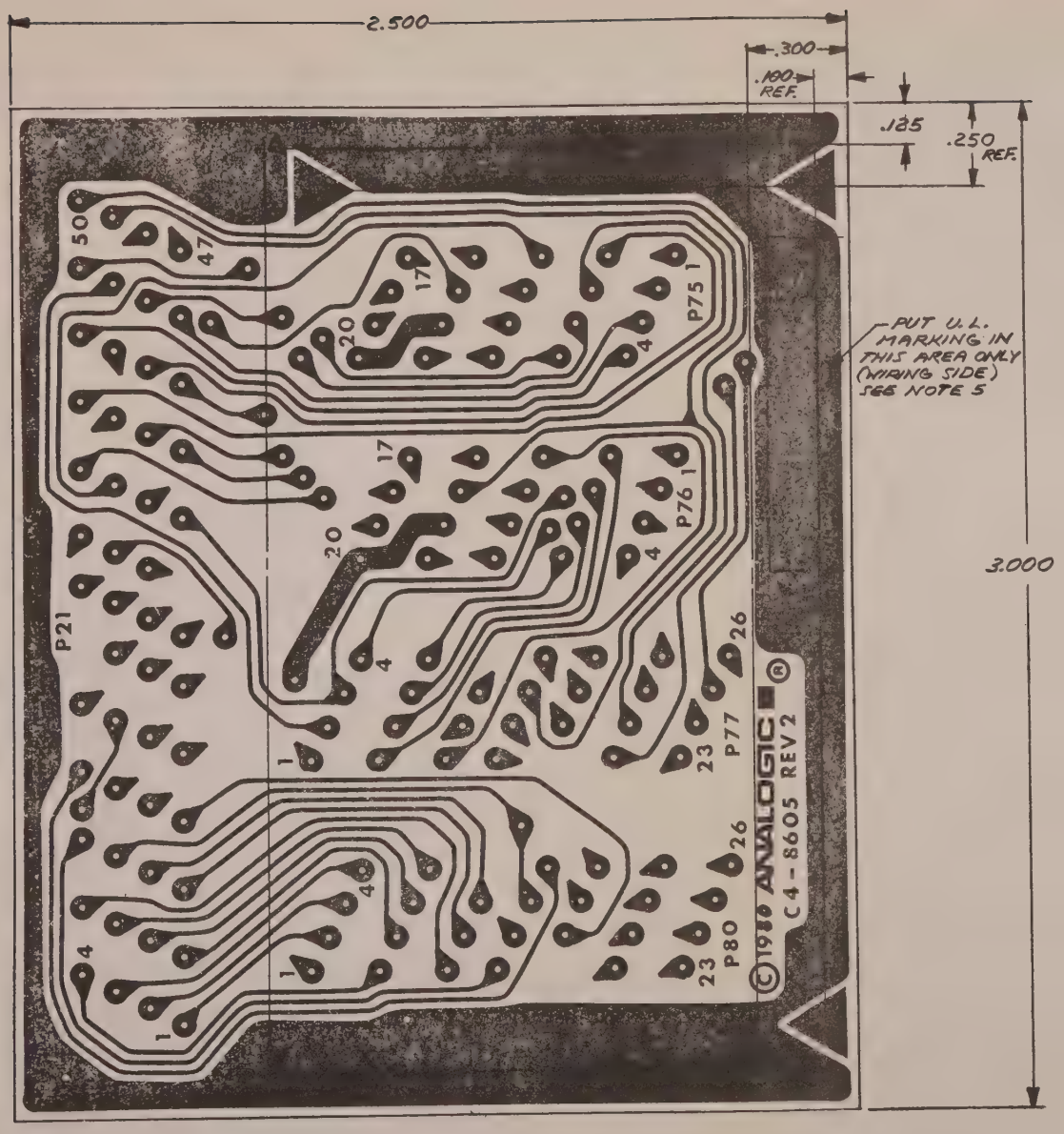
WIRING SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±			"THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF ANALOGIC CO. AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION FROM ANALOGIC CO."	DRAWN J.S. ROGERS	DATE 7/27/77
MATERIAL SEE NOTE 1				CHECKED	7-27-77
FINISH SEE NOTE 2				DESIGNER	7-27-77
				ENGINEER	7-27-77
				APPROVED	7/29/77
APPLICABLE SPECIFICATIONS A2-1040	PL10-3700	AN5400		RELEASED	8/2/77
	NEXT ASSY	USED ON		WEIGHT	
	APPLICATION				

ANALOGIC WAKEFIELD, MASS. 01880

DRILLING
NOVATROL
CABLE BOARD NO. 1

CODE IDENT NO	SIZE		REV
31814	C	4-8604	2
SCALE 4/1	ACCOUNT NO.	SHEET 1 OF 4	



REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPLD	DATE	
2	4-581	SEE E.C.O.	RP	WR	WR	4/24/80

SIZE 4-8605 REV 2

NOTES:

1. MATERIAL: GLASS EPOXY (FR4) DOUBLE SIDED, 2 OZ. COPPER, GREEN, .062 THK.
2. SOLDER TIN PLATE (60/40) WITH THICKNESS OF .0005 TO .0010
3. FABRICATE PER A2-1040
4. FOR ASSEMBLY SEE C7-2300
5. P.C. BOARD SHALL BE UL. APPROVED AND MARKED WITH U.L. CODE IDENTIFICATION AND THE FLAMMIBILITY RATING, EITHER UL-94V-01 OR UL-94V-02 (DEPENDING ON MATERIAL USED.)
6. HOLE LEGEND:

LTR	SIZE		QTY
*	.039-.045 DIA.	AFTER PLATING	A/R
A	.130 DIA.	" "	4
B	.125 +.003 -.000	NON PLATED	3

WIRING SIDE

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			CHECKED R ROSS	7/27/77	DRILLING NOVATROL CABLE BOARD NO.2
			DESIGNER RWH	7/28/77	
			ENGINEER RWH	7/28/77	
			APPROVED REP	7/29/77	
PL10-3700	AN5400		RELEASED R. FRAKE	8/2/77	CODE IDENT NO. 31814 | SIZE C | 4-8605 | REV 2
NEXT ASSY	USED ON		WEIGHT TOL. .XX - .01 .XXX - .005		SCALE 4/1 | ACCOUNT NO. | SHEET 1 OF 4
APPLICATION					

DEC LSI-11* INTERFACE FOR AN5400

GENERAL

The LSI-11* Interface is an extremely powerful, compact unit allowing the full capability of the AN5400 Data Acquisition System to be efficiently utilized. With this Interface, the Data Acquisition System becomes an integral part of the computer hardware.

Very high speed DMA transfers can be used to read A/D channels, load digital output channels, or interrogate digital input channels. DMA operation with A/D channels is particularly fast because 2-cycle DMA bursts are made during the A/D conversion, thus avoiding unnecessary waiting time between conversions.

Full program control augments the DMA capability and allows three types of data transfers (A/D, digital out, or digital in) to be made through a single register, based on the mode of operation set up in the control register. Special commands allow operation of simultaneous sample and hold amplifiers in the AN5400.

A vector interrupt is used to signal the following:

- The end of a DMA operation.
- Completion of an A/D conversion.
- Reception of an external sample and hold command.
- The detection of an error.

A second vector interrupt indicates the reception of an interrupt request from the user cards in the AN5400 systems.

A special register in the LSI-11 peripheral address space allows direct access to the thumbwheel switches on the AN5400 front panel.

Finally, the Interface uniquely provides for 128 master registers. These registers are locations in the peripheral address space which directly control digital input or output cards installed in the AN5400 chassis. These Read/Write registers allow implementation of memory reference instructions on the individual cards installed in the AN5400 system. This technique allows such instructions as CLR, INC, DEC*, TST, CMP, etc., to operate directly on relay cards, D/A converters, digital output cards and others.

MECHANICAL

The Interface consists of one quad-size DEC board which plugs directly into the LSI-11 bus and connects to the Zero-Level interface in the AN5400 chassis through a 12-foot cable.

POWER

Power for the Interface is +5 volts ±5% at 2.5 amps., supplied by the LSI-11 system. A power-off condition of the AN5400 does not affect the LSI-11 bus operation.

ENVIRONMENTAL

- Operating ambient: 0° to 50°C.
- Storage ambient: −20° to +85°C.
- Non-condensing humidity: 90%.

OPERATING MODES

The Interface is designed to control A/D conversions, digital inputs, and digital outputs through six operating modes, defined by the Mode bits in the Control and Status Register (CSR). Three of the modes allow programmed I/O operation while the other three modes allow DMA operation. Communication with the AN5400 is accomplished through the Transaction Register, hereafter referred to as TRR. In programmed I/O operation, addresses or data are loaded into TRR and data is read from TRR. During DMA operation, TRR is automatically loaded from a table in memory and the resulting data is read from TRR into memory. The addresses associated with all of the modes may be random in nature.

PROGRAMMED I/O — MODE Ø — A/D INPUTS

- Set Mode bits to ØØØ in CSR.
- Write gain and address into TRR for desired channel.
- READY will go low in CSR until the conversion is complete. When the conversion is finished, READY will go high and the Interface will generate an interrupt.
- When the READY bit goes high, the resulting A/D data may be read from TRR.
- The process may be continued by returning to the second step above.

PROGRAMMED I/O — MODE 2 — DIGITAL OUT

- Set Mode bits in CSR to Ø1Ø.
- Write address of desired digital output card into TRR.
- Write data to be transmitted to previously addressed card into TRR.
- The process may be continued by returning to the second step above.

NOTE: To avoid a possible lack of synchronization between the two Write steps, a bit in the CSR called PART 2 will go high after the address is sent to TRR and will return low after the data is sent to TRR. Thus, a high state for PART 2 indicates that the next Write to TRR will be interpreted as data and not as an address. Performing any transaction other than digital out, while PART 2 is high, will give ambiguous results.

PROGRAMMED I/O — MODE 3 — DIGITAL IN

- Set Mode bits in CSR to Ø11.
- Write address of desired digital input card into TRR.
- Read data being transmitted by previously addressed card from TRR.
- The process may be continued by returning to the second step above.

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DMA – MODE 4 – A/D INPUTS

- Load DMAR1 with the starting location of the gain and address table in memory.
- Load DMAR2 with the starting location of the A/D data buffer.
- Set the Mode bits in CSR to 100.
- Set the GO bit high in the CSR.
- The READY bit in the CSR will go low until the DMA transfers are complete. The DMA transfers will stop when a –1 is read from the gain and address table, or if an error is detected, or if the GO bit is cleared.
- When the DMA transfers are complete, the GO bit will be reset and the READY bit will be set. At this time, an interrupt will be generated by the Interface.
- The process may be restarted by returning to the first step above.

DMA – MODE 6 – DIGITAL OUTPUT

- Load DMAR1 with the starting memory location of the address table.
- Load DMAR2 with the starting memory location of the digital data table.
- Set the mode bits in the CSR to 110.
- Set the GO bit high in the CSR.
- Same as third-last item under Mode 4.
- Same as second-last item under Mode 4.
- Same as last item under Mode 4.

DMA – MODE 7 – DIGITAL INPUT

- Load DMAR1 with the starting memory address of the address table.
- Load DMAR2 with the starting memory location of the digital input buffer.
- Set the mode bits in the CSR to 111.
- Set the GO bit high in the CSR.
- Same as third-last item under Mode 4.
- Same as second-last item under Mode 4.
- Same as last item under Mode 4.

FRONT PANEL REGISTER

A specific peripheral address is assigned as a Read Only Register for the thumbwheel switches on the AN5400 front panel.

MASTER REGISTERS (MR)

128 specific memory locations are reserved in the LSI-11 peripheral address space to directly control up to 128 channels of 16-bit digital registers located in the AN5400 system. These registers correspond to card addresses in the AN5400 system, and their presence, absence and characteristics are determined solely by the types of user cards installed. Based on these cards, the registers may appear to be read only, write only, read/write, or missing. From a hardware standpoint, all registers will reply to data in or data out cycles, but reading or writing to missing cards will be meaningless.

A typical system example will illustrate the usefulness of the MR's. Assume a standard AN5400 system which contains a standard D/A patch plug i.e., D/4. The MR addresses, associated with the card slots, would be as shown in Table1. All MR addresses must be added to the switch-selected base address chosen for the Interface.

Table 1
Master Register Addresses (Example)

	SLOT J1	SLOT J2	SLOT J3	ETC.
MASTER REGISTER ADDRESS	0 2 4 6	10 12 14 16	20 22 24 26	

Now assume the slots contain the following cards:

J1 = AC1562 (4-channel D/A converter)
J2 = AC1530 (2-channel D/A converter with readback)
J3 = DC6000 (2-channel digital input)

Thus, the MR addresses and characteristics for this system are as listed in Table 2.

Table 2
Master Register Address Characteristics (Example)

MASTER REGISTER ADDRESS (ADD TO BASE ADDRESS)	CHARACTERISTICS
0	Channel 0, AC1562, Write only
2	Channel 1, AC1562, Write only
4	Channel 2, AC1562, Write only
6	Channel 3, AC1562, Write only
10	Channel 0, AC1530, Read/Write
12	Missing
14	Channel 1, AC1530, Read/Write
16	Missing
20	Channel 0, DC6000, Read only
22	Missing
24	Channel 1, DC6000, Read only
26	Missing
30	} Determined by cards
.	
.	
.	
376	

In this example, MR 10 and 14 are the most flexible since read/modify/write LSI-11 instructions can be directly applied to them. Thus, commands like COM, INC, DEC, NEG, ASR, ASL, ROR, ADD and SUB may be directly applied to either channel of the AC1530 card.

BASE ADDRESS

The base address of the AN5400 Interface is switch-selectable to any one of the 16 locations shown in Table 3. The unit is shipped with address 164000.

Table 3
Interface Base Addresses

SWITCHES				
A12	A11	A10	A9	BASE ADDRESS
1	1	1	1	177000
1	1	1	0	176000
1	1	0	1	175000
1	1	0	0	174000
1	0	1	1	173000
1	0	1	0	172000
1	0	0	1	171000
1	0	0	0	170000
0	1	1	1	167000
0	1	1	0	166000
0	1	0	1	165000
0	1	0	0	164000
0	0	1	1	163000
0	0	1	0	162000
0	0	0	1	161000
0	0	0	0	160000

NOTE: S1 on P.C. Board = Address switch. "ON" = 1 in address table. The switch nearest the card handles controls A12; the next one down controls A11, etc.

INTERFACE REGISTER

All of the Interface registers are 16-bit word registers; they will not properly respond to byte commands that load or swap 8-bit bytes. A list of all Interface registers and their characteristics is given in Tables 4 and 5.

Table 4
Interface Registers

NAME	ABBR.	READ/WRITE	ADD. REL. TO BASE
MASTER REGISTERS	MR	R/W	000-376
CONTROL & STATUS	CSR	R/W	400
DIRECT MEMORY ACCESS 1	DMAR1	R/W	402
DIRECT MEMORY ACCESS 2	DMAR2	R/W	404
SPARE	SPARE	.....	406
TRANSACTION	TRR	R/W	410
FRONT PANEL	FPR	R	412

Table 6
Transfer Characteristics Established by Bits 1, 2 & 3

MODE	BIT 3	BIT 2	BIT 1	TYPE
7	1	1	1	DIG IN (DMA)
6	1	1	Ø	DIG OUT (DMA)
5	1	Ø	1	NOT USED
4	1	Ø	Ø	A/D (DMA)
3	Ø	1	1	DIG IN (PI/O)
2	Ø	1	Ø	DIG OUT (PI/O)
1	Ø	Ø	1	NOT USED
Ø	Ø	Ø	0	A/D (PI/O)

CONTROL & STATUS REGISTER

GO (BIT Ø)

The GO bit is used to start and stop DMA action. The type of transfers to be made when the GO bit is high depend upon the mode established by the Mode bits. Writing a one to the GO bit is the only way that DMA transfers can be initiated. Any of the following conditions will reset the GO bit and stop DMA transfers:

a. Writing a zero to the GO bit.
b. Selection of Modes Ø, 1, 2 or 3.
c. AN5400 in local control.
d. Imminent loss of DC power (BPOK NEGATION).
e. Bus initialization (BINIT).
f. Detection of an error (CSR BIT 15).
g. Detection of the normal DMA stop code (a–1 in address table).

The GO bit may be set at the same time that a DMA mode is established, without causing a reset of the GO bit by the action of "b" listed above.

MODE BITS (BITS 1, 2 AND 3)

These three bits establish the types of transfers to take place as listed in Table 6.

Modes 1 and 5 are illegal modes which will cause indeterminate results if used. Modes Ø, 2 and 3 control the type of programmed I/O transfers made through the Transaction Register. Modes 4, 6 and 7 control the type of DMA transfers to be started when the GO bit is set.

PART 2 (BIT 4)

Part 2 is a bit that may be used in conjunction with Mode 2 to maintain synchronization among successive write commands to the Transaction Register. When this bit is high, the next word sent to TRR will be interpreted as data and not as an address.

54 ENB. (BIT 5)

This bit controls the ability of the AN5400 user cards to cause an interrupt. It is set by writing a one to bit 5. It is reset by writing a zero to bit 5 or by bus initialization (BINIT).

INTERRUPT ENABLE (BIT 6)

This bit controls the ability of the Interface to cause an interrupt. It is set by writing a one to bit 6. It is reset by writing a zero to bit 6 or by bus initialization (BINIT).

Table 5
Control & Status Register Characteristics

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	PI/O ERR	DMA ERR	LOCK	RMT	SSH	CLR	CLR1	READY	INT ENB.	54 ENB.	PART 2	MODE 2	MODE 1	MODE Ø	G 0
R	R	R	R/W	R	R	W	W	R	R/W	R/W	R	R/W	R/W	R/W	R/W

NOTES: R = Read only W = Write only R/W = Read/Write

READY (BIT 7)

The READY bit indicates the ability of the Interface to accept a new command. It is high unless:

- The GO bit is set.
- An A/D conversion is taking place.
- The SSH bit is high.

CLR 1 (BIT 8)

CLR 1 is a WRITE ONLY bit which performs a limited clearing function in the Interface and in the AN5400 system. It is particularly useful for getting out of hangup states caused by detected errors or external synchronization signals. In the Interface, CLR 1 resets any detected errors (Bits 13, 14 and 15 of CSR). In the AN5400 system, CLR 1 resets SSH and reset BSY. This bit will always be read as a zero.

CLR (BIT 9)

CLR is a WRITE ONLY bit that causes a general clearing function to occur in the AN5400 as follows:

- Selects A/D address decoding.
- Selects "OUT" mode for digital bus.
- Resets range register.
- Resets address register.
- Goes to all user cards.

The CLR bit is always read as a zero.

SSH (BIT 10)

This bit is used in conjunction with simultaneous sample and hold operations when an external signal gates the "HOLD" function. It is high only when the following two conditions exist:

- An "External Hold" command has been sent to the AN5400 system.
- An external signal is pulling down on pin 5 of J28 at the rear of the AN5400 system, preventing the completion of the "Hold" command.

The SSH bit will go low when the signal on J28 goes high, thus indicating the completion of the "Hold" command. This bit is normally used when simultaneous sample and holds are being synchronized to external real-time events.

RMT (BIT 11)

The REMOTE bit is a reflection of the RMT light on the AN5400 front panel and is high when the system is in remote (computer) control and low when it is in local (front panel) control. Any commands sent to the AN5400, while it is in local control, will have no effect.

LOCK (BIT 12)

The LOCK bit can be used to prevent placing the AN5400 into local control. If this bit is set while the AN5400 is in remote control, the system cannot be put into local control, thus rendering all front panel pushbuttons inoperative. If the bit is set while the AN5400 is in local control, it will have no effect.

DMA ERR (BIT 13)

This bit is set if either DMAR1 or DMAR2 attempts to access a non-existent memory location. If during a DMA operation BRPLY is not received from memory within 12 μsec., the DMA ERR bit will be set.

PI/O ERR (BIT 14)

The Programmed I/O Error bit is set if an attempt is made to access the front panel register, the Transaction Register, or any Master Register during a DMA operation. The CSR, DMAR1, and DMAR2 registers may be read during DMA operations, but writing to them will usually cause indeterminate results.

ERR (BIT 15)

This bit is set if either bit 13 or bit 14 is set. Errors may be cleared only by issuing a CLR 1.

DMAR1

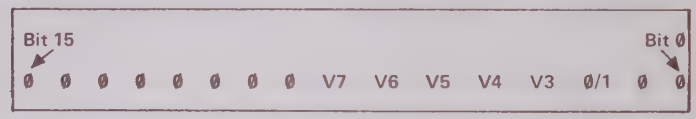
Direct Memory Address Register 1 is used as a pointer to the address table during DMA operation. Since it points at consecutive 16-bit words, it is a 15-bit Read/Write register. Bit zero is always read as a zero.

DMAR2

Direct Memory Address Register 2 is used as a pointer to the Data buffer, in Modes 4 and 7, and as a pointer to a data table in Mode 6. DMAR2 is also a 15-bit Read/Write Register, where bit zero is always read as a zero.

INTERRUPTS

Two interrupt vectors are used by the Interface to signal completion of a task, arrival of an external hold signal, detection of an error, or a AN5400 user card request. The vectors are switch selectable over the range 000 to 370 in steps of 10, as illustrated:



Switch S2 controls the vector address. "ON" = 1 in the vector. The switch nearest the card handles controls V7, the next one down V6, etc. The card is shipped with vectors 270/274 selected.

If the INTERRUPT ENABLE bit in the CSR is set, an interrupt will occur (normally at 270) if any of the following four occurrences take place:

- Completion of an A/D conversion during P I/O operation.
- Completion of a DMA cycle. (Fall of GO bit).
- Reception of an external sample and hold signal. (Fall of BSSH)
- Detection of an error. (Rise of ERR).

The second item above will cause an interrupt if the GO bit is reset for any of the reasons stated in the GO (BIT 0) Section. Interrupts, caused by the detection of an error, must be reset by issuing a CLR 1 through the CSR.

If the 54 ENB bit in the CSR is set, an interrupt will occur (normally at 274) if a AN5400 user card requests service. At this point, the user's routine would normally do a digital input from address 4000 to read the vector from the AN5400 user card.

REFERENCES

- AN5400 System Manual (A2-4113).
- Zero Level Interface Spec. (A2-4106).
- DEC Microcomputer Handbook.
- Interface Schematic (D5-8612, Figs. 1a and 1b).
- Interface Assembly (D7-8612, Fig. 2).

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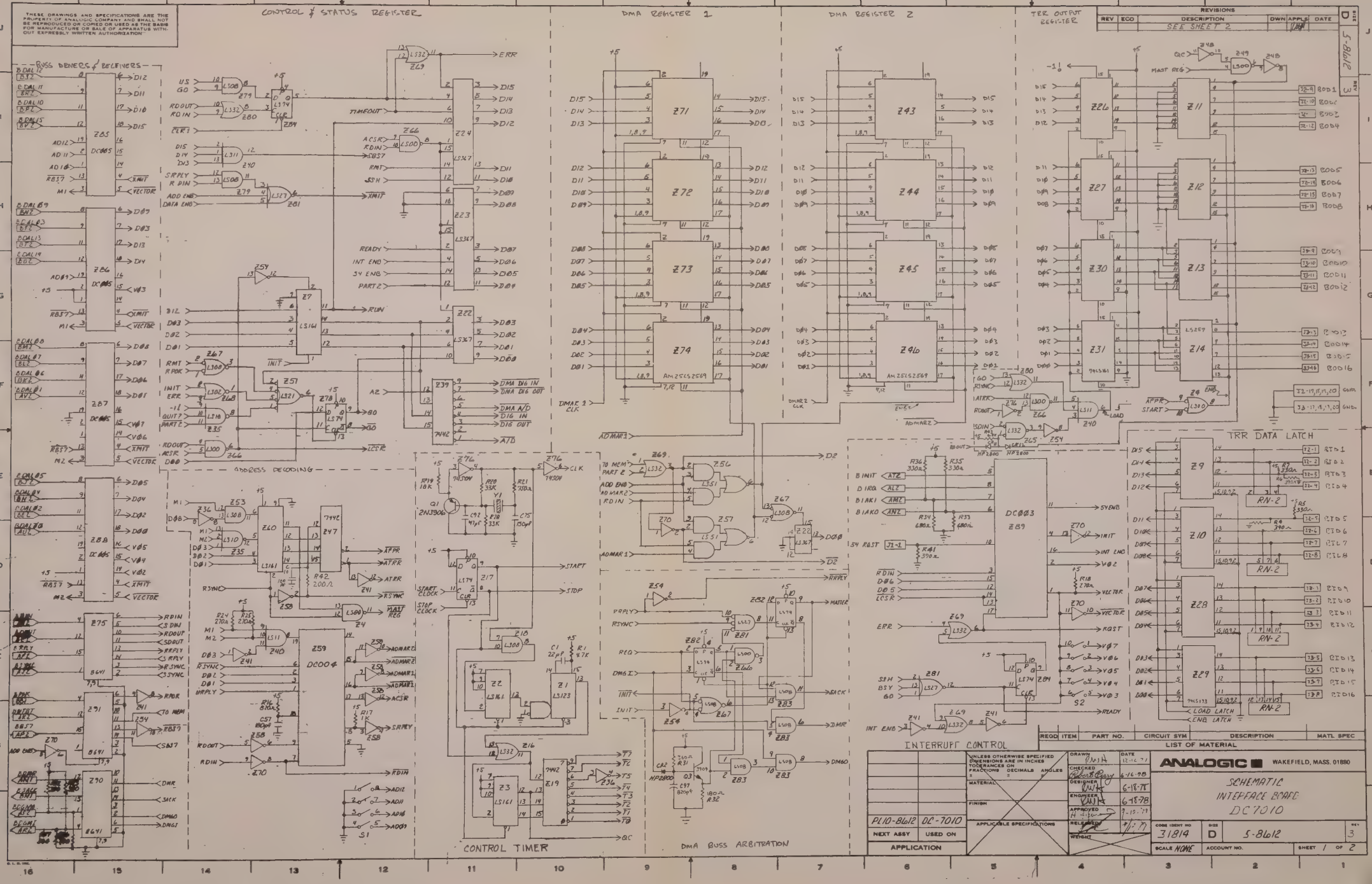
CONTROL & STATUS REGISTER
DMA REGISTER 1
DMA REGISTER 2
TRR OUTPUT REGISTER
TRR DATA LATCH
BUSS DRIVERS & RECEIVERS
ADDRESS DECODING
CONTROL TIMER
DMA BUSS ARBITRATION
INTERRUPT CONTROL
LIST OF MATERIAL
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REVISIONS
REV ECO DESCRIPTION DWN APPD DATE
SEE SHEET 2
ANALOGIC WAKEFIELD, MASS. 01880
SCHEMATIC
INTERFACE BOARD
DC7010
31814
D
5-8612
3
SCALE NONE
SHEET 1 OF 2
PL10-8612 DC-7010
NEXT ASSY USED ON
APPLICATION
DRAWN 12-16-77
CHECKED 6-16-78
DESIGNER 6-18-78
ENGINEER 6-18-78
APPROVED 7-10-79
RELEASED 7/1/79
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
2	4918	SEE E.C.O.	KH	DP	10-11-78
3	4-508	NO CHANGE UPDATED REV	KH	BR	4-5-79

D SIZE 5-8612 REV 3

POWER PINS

REF DES.	I.C. TYPE	+5	DIG. RTN.
Z43,44,45,46,71,72,73,74	AM25LS2569	20	10
Z4,43,66	74LS00	14	7
Z39,61,68	74LS02	14	7
Z8,36,41,46,56,68,70	74LS04	14	7
Z76	74S04	14	7
Z16,30,53,67,79,83	74LS08	14	7
Z35	74LS10	14	7
Z40	74LS11	14	7
Z51	74LS21	14	7
Z33, 81	74L27	14	7
Z16, 62, 69, 80	74LS32	14	7
Z6, 20	7433	14	7
Z5	7438	14	7
Z19 29, 47	7442	16	8
Z57, 58, 59	74LS51	14	7
Z17, 38, 52, 62, 63, 64, 77, 78, 82, 84	74S74	14	7
Z1, 21, 32	74LS123	16	8
Z2, 3, 22, 27, 30, 31, 60	74LS161	16	8
Z9, 10, 28, 29	74LS173	16	8
Z11, 12, 13, 14	74LS257	16	8
Z22, 23, 24	74LS367	16	8
Z75, 76, 91	B641	16	8
Z89	DC003	18	9
Z59	DC004	20	10
Z85, 86, 87, 88	DC005	20	10
RN1, 2		16	8

ALSO SAME FOR C AND D CONNECTORS

DMA GRANT

INT GRANT

DMA CONTROL

J4

J1

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

P10-8612	DC-7010		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±

MATERIAL

FINISH

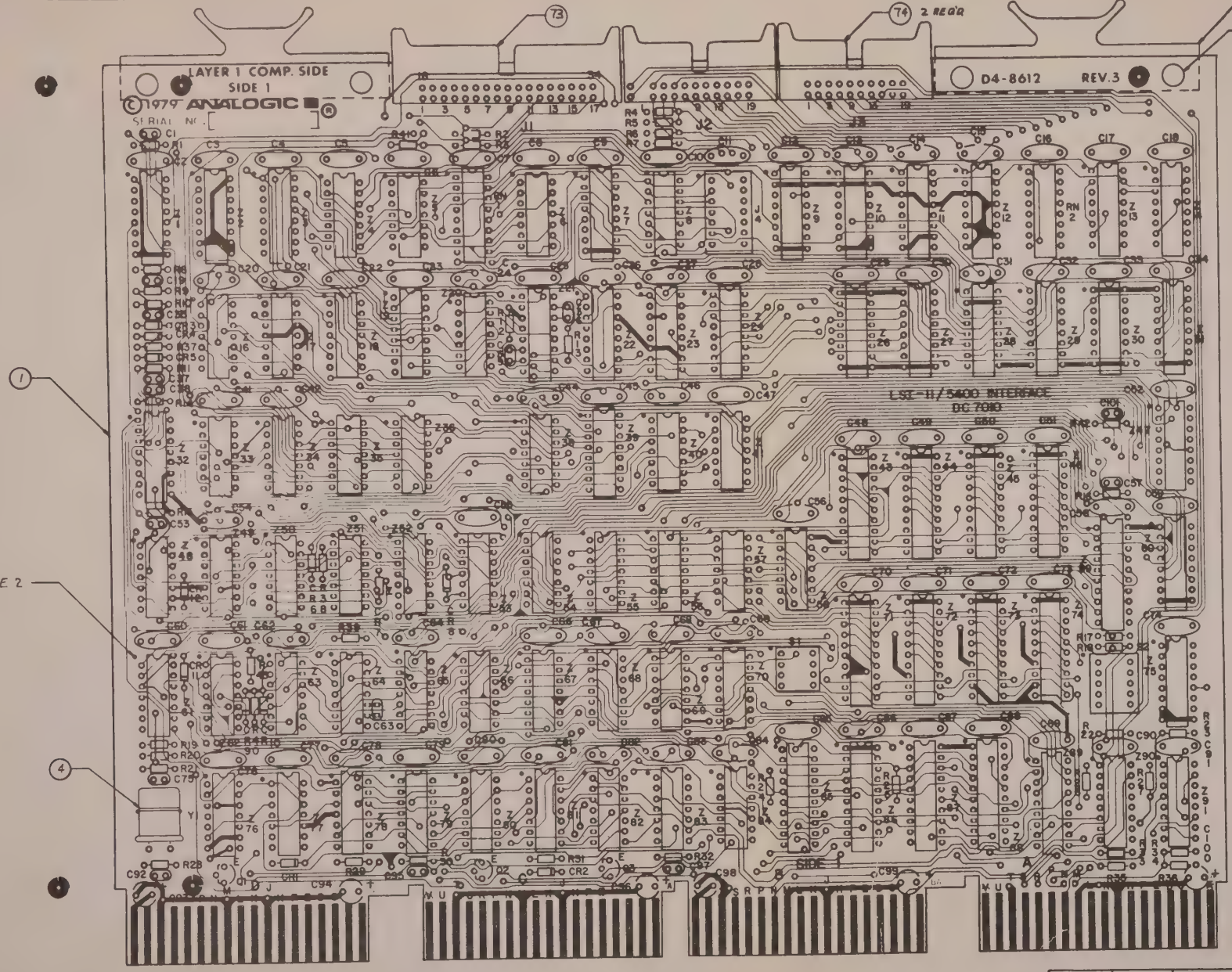
APPLICABLE SPECIFICATIONS

DRAWN	KWH	12-12-77
CHECKED		4-6-78
DESIGNER	KWH	6-15-78
ENGINEER	KWH	6-16-78
APPROVED		7-16-78
RELEASED		9/12/78
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC
INTERFACE BOARD
DC 7010

CODE IDENT NO	SIZE		REV
31814	D	5-8612	3
SCALE NONE	ACCOUNT NO		SHEET 2 OF 2



COMPONENT SIDE

REVISIONS				
REV	ECO	DESCRIPTION	DWN	APPD	DATE
2	1140	SEE ECO.	[illegible]	[illegible]	5-7-79
3	1340	UPDATED REVISION	[illegible]	[illegible]	7-6-79

D T-8612 3

NOTES:
1. FOR SCHEMATIC SEE D5-8612.
2. DOT INDICATES PIN 1 OF I.C.S, RESISTOR NETWORKS AND SWITCHES.
3. ASSEMBLE PER A2-1027.
4. MAXIMUM COMPONENT HEIGHT= .375" ABOVE BOARD SURFACE.

PL10-8612	DC 7010
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS ANGLES
X ± .10 ± XXX ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
A2-1027

		DATE
DRAWN	T. Low	6-7-78
CHECKED	Richard Berry	6-16-78
ENGINEER	[illegible]	6-19-78
ENGINEERING MGR	[illegible]	6-19-78
QUALITY CONTROL	[illegible]	9-10-79
PROJECT ENGINEER	[illegible]	9/10/79
WEIGHT		

ANALOGIC, WAKEFIELD, MASS 01880

ASSEMBLY INTERFACE BOARD DC 7010

CODE IDENT NO	SIZE	DWG NO	REV
31814	D	T-8612	3

SCALE 2:1 SHEET 1 OF 1

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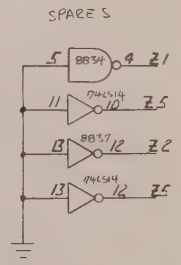
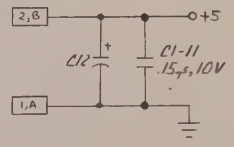
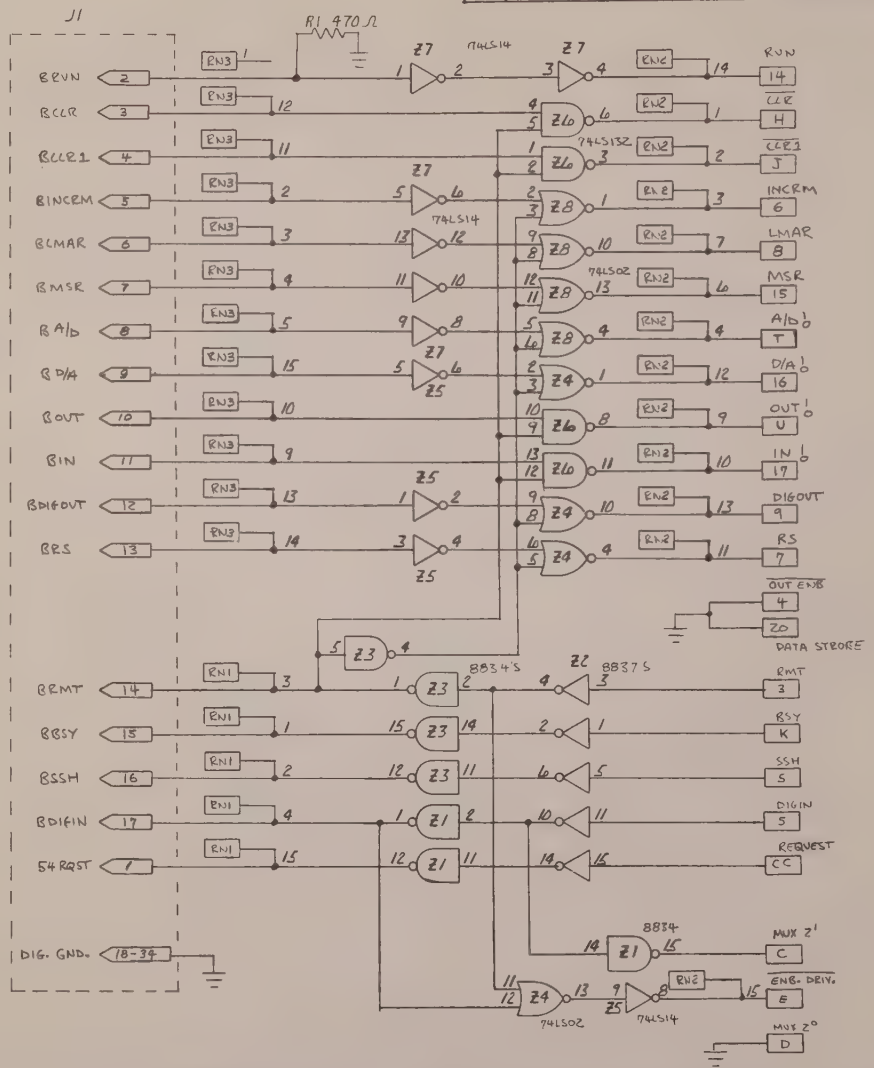
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1	4 424	SEE E.C.O	L.I	L	4 9 79
2	4-564	SEE E.C.O.	D.P	L.M.	1-24-80

SIZE C | 5-8639 | REV 2

POWER & GROUND PINS FOR I.C.'S	GND PINS	+5 PINS
74LS132	7	14
74LS02	7	14
74LS14	7	14
8834	7,8,9	16
8837	7,8,9	16
RN 1,2,3	8	16







		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX ± .XXX ± ANGLES ±	DRAWN [illegible]	DATE 6-5-78	ANALOGIC, WAKEFIELD, MASS. 01880
		MATERIAL	CHECKED [illegible]	6-19-78	SCHEMATIC ZERO LEVEL INTERRUPT INTERFACE CARD AC463
		FINISH	ENGINEER [illegible]	6-19-78	
			ENGINEERING MGR. [illegible]	6-19-78	
PL10-8639	AC463	APPLICABLE SPECIFICATIONS	QUALITY CONTROL [illegible]	9-18-79	
NEXT ASSY	USED ON		PRODUCTION [illegible]	9/19/79	CODE IDENT NO 31814 | SIZE C | 5-8639 | REV 2
APPLICATION			WEIGHT		SCALE NONE | SHEET 1 OF 1

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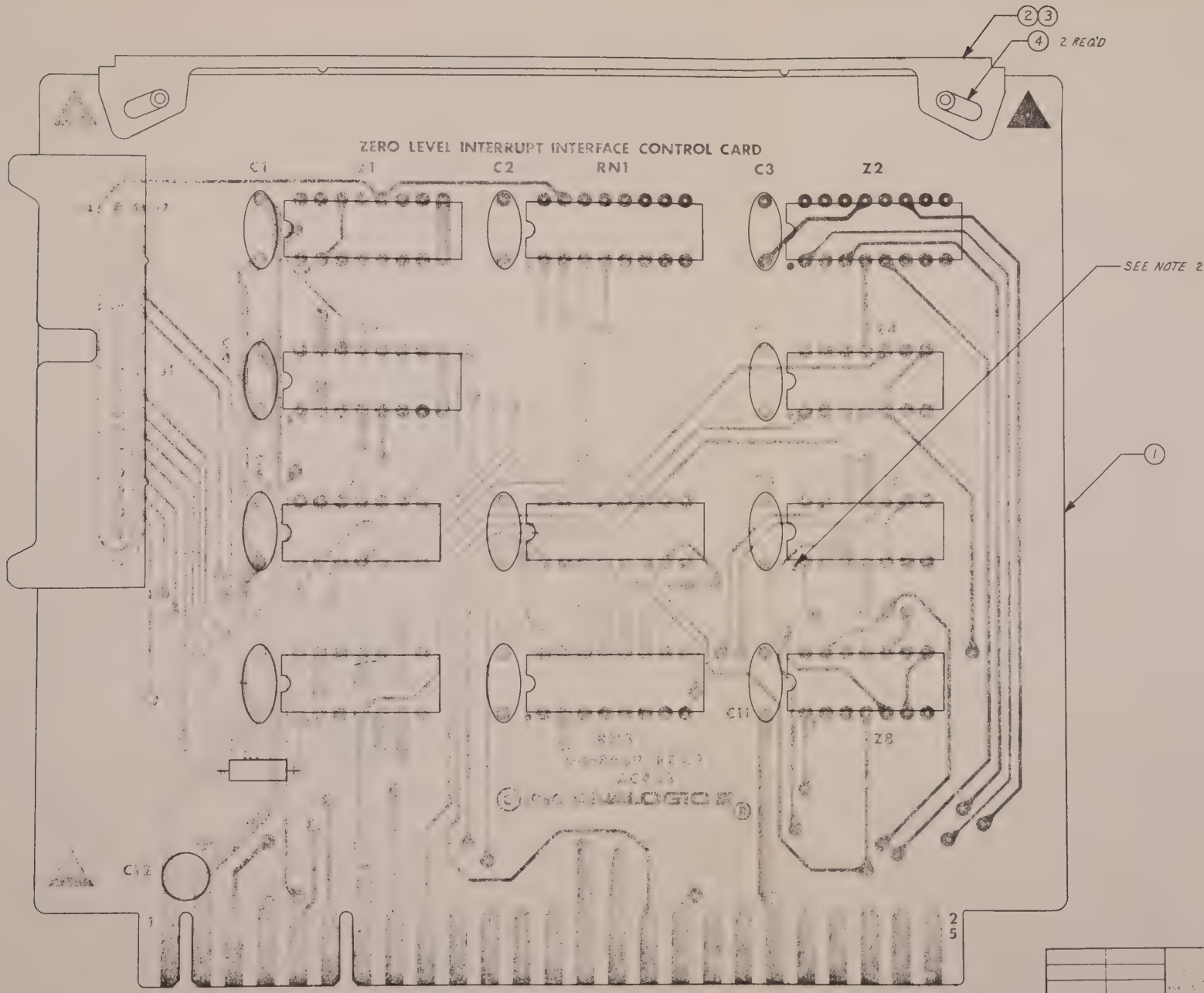
REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPLS	DATE	
2	4-569	SEE ECO.	R.S	DP	CM	1-26-80

D 7-8639 2



NOTES:
1. FOR SCHEMATIC SEE C5-8639.
2. DOT INDICATES PIN 1 OF I.C.'S & R.N.'S.
3. ASSEMBLE PER A2-1027.

COMPONENT SIDE

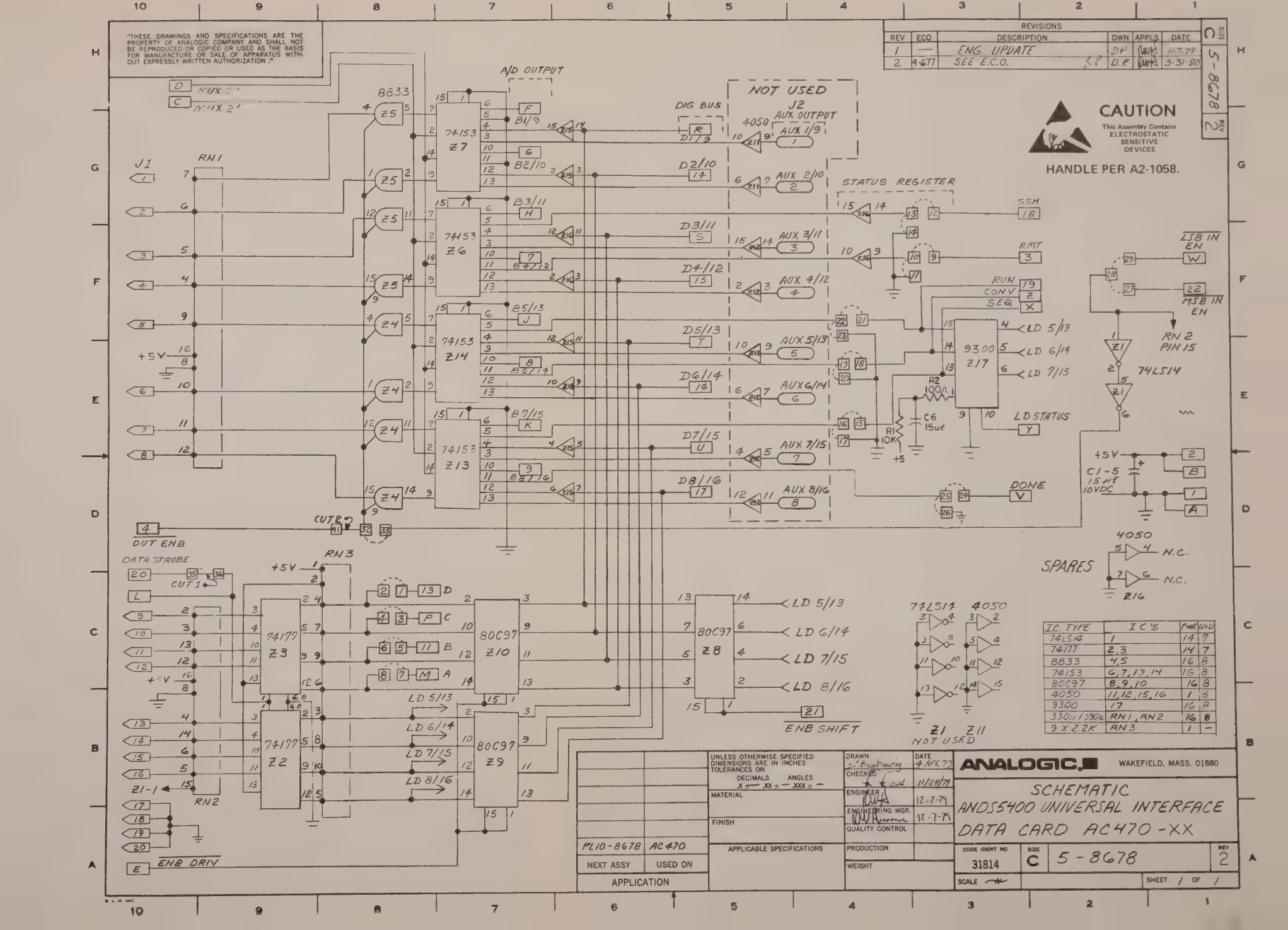
	DRAWN	J. LASPINA	6-19-78
		R. PERRY	6-19-78
		R.W. HAVENER	6-19-78
	APPROVED	R.K. HAVENER	6-19-78
		H. GARAVANIAN	9-18-79
	RELEASED	R. KINSALL	9-19-79

PL10-8639 AC 463
NEXT ASSY | OPTION
APPLICATION

ANALOGIC WAKEFIELD, MASS. 01880

ASSEMBLY
ZERO LEVEL INTERRUPT INTERFACE CARD
AC 463

DO NOT SCALE	SIZE		REV
31814	D	7-8639	2
SCALE 4:1	AT COUNT NO	SHEET 1 OF 1	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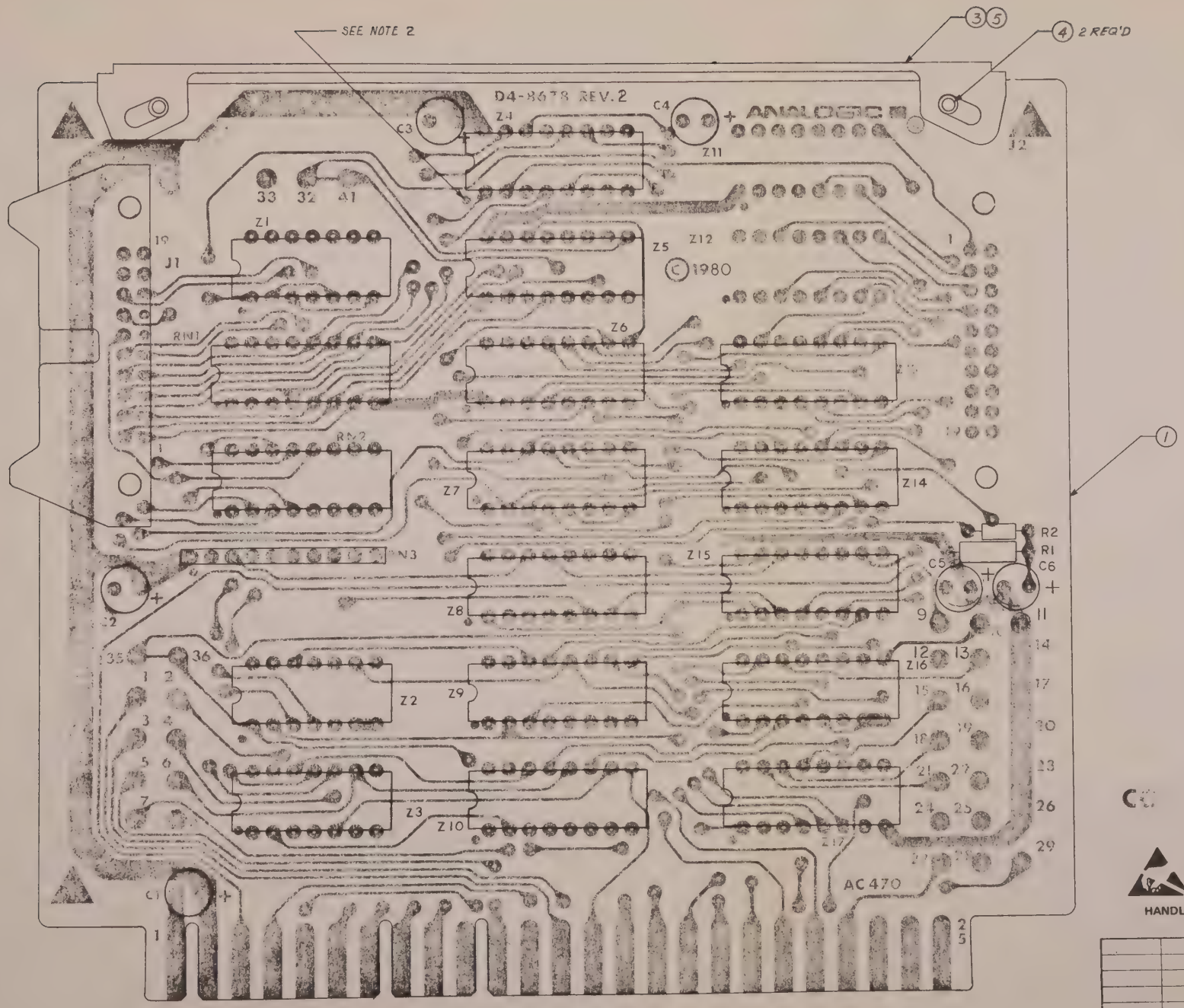
REVISIONS
REV | ECO | DESCRIPTION | DWN | APPLS | DATE
1 | — | ENG. UPDATE | D.P. | | 11-7-79
2 | A-677 | SEE E.C.O. | D.P. | | 3-31-80
SIZE C 5-8678 REV 2
CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
A/D OUTPUT
NOT USED
J2
4050
AUX OUTPUT
DIG BUS
STATUS REGISTER
J1
RN1
8833
74153 Z7
74153 Z6
74153 Z14
74153 Z13
AUX 1/9
AUX 2/10
AUX 3/11
AUX 4/12
AUX 5/13
AUX 6/14
AUX 7/15
AUX 8/16
D1/9
D2/10
D3/11
D4/12
D5/13
D6/14
D7/15
D8/16
B1/9
B2/10
B3/11
B4/12
B5/13
B6/14
B7/15
B8/16
SSH
RMT
RUN CONV SEQ
LD STATUS
DONE
LD 5/13
LD 6/14
LD 7/15
9300 Z17
R1 10K
R2 100Ω
C6 15μF
+5V
LSB IN EN
MSB IN EN
RN2 PIN 15
74LS14
C1-5 15 μF 10VDC
SPARES
N.C.
Z16
CUT 2
OUT ENB
DATA STROBE
CUT 1
RN3
74177 Z3
74177 Z2
80C97 Z10
80C97 Z9
80C97 Z8
LD 5/13
LD 6/14
LD 7/15
LD 8/16
ENB SHIFT
Z1-1
RN2
ENB DRIV
Z1 Z11 NOT USED
IC. TYPE | IC'S | PWR | GND
74LS14 | 1 | 14 | 7
74177 | 2,3 | 14 | 7
8833 | 4,5 | 16 | 8
74153 | 6,7,13,14 | 16 | 8
80C97 | 8,9,10 | 16 | 8
4050 | 11,12,15,16 | 1 | 8
9300 | 17 | 16 | A
330Ω/390Ω | RN1, RN2 | 16 | B
9 X 2.2K | RN3 | 1 | —
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS ANGLES .X ± .XX ± .XXX ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN D. Brightwing 4 APR 79
CHECKED 11/28/79
ENGINEER 12-7-79
ENGINEERING MGR. 12-7-79
QUALITY CONTROL
PRODUCTION
WEIGHT
PL10-8678 AC470
NEXT ASSY USED ON
APPLICATION
ANALOGIC WAKEFIELD, MASS. 01880
SCHEMATIC
AND5400 UNIVERSAL INTERFACE
DATA CARD AC470-XX
CODE IDENT NO 31814
SIZE C 5-8678 REV 2
SCALE
SHEET 1 OF 1



NOTES:
1. FOR SCHEMATIC SEE C5-8678.
2. DOTS INDICATE PIN 1 OF I.C.'S AND R.N.'S.
3. ASSEMBLE PER A2-1027.
4. MAXIMUM COMPONENT HEIGHT TO BE .500".

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
1	—	ENG UPDATE	DP		11-7-79
2	1-677	SEE E.C.O.	RP	DP	4-2-80

D 7-8678 2

		D. PONJU	11-7-79
		R. Rose	11/20/79
			12-7-79
			12-7-79

APPROVED

PL10-8678	AC-470
N. HT ASSY	USED ON
APPLICATION	

ANALOGIC NEWBURYPORT, MASS. 01-80

ASSEMBLY
ANDS 5400 UNIVERSAL
INTERFACE DATA CARD AC470

31814	D 7-8678	2
SCALE 4:1		SHEET 1 OF 1

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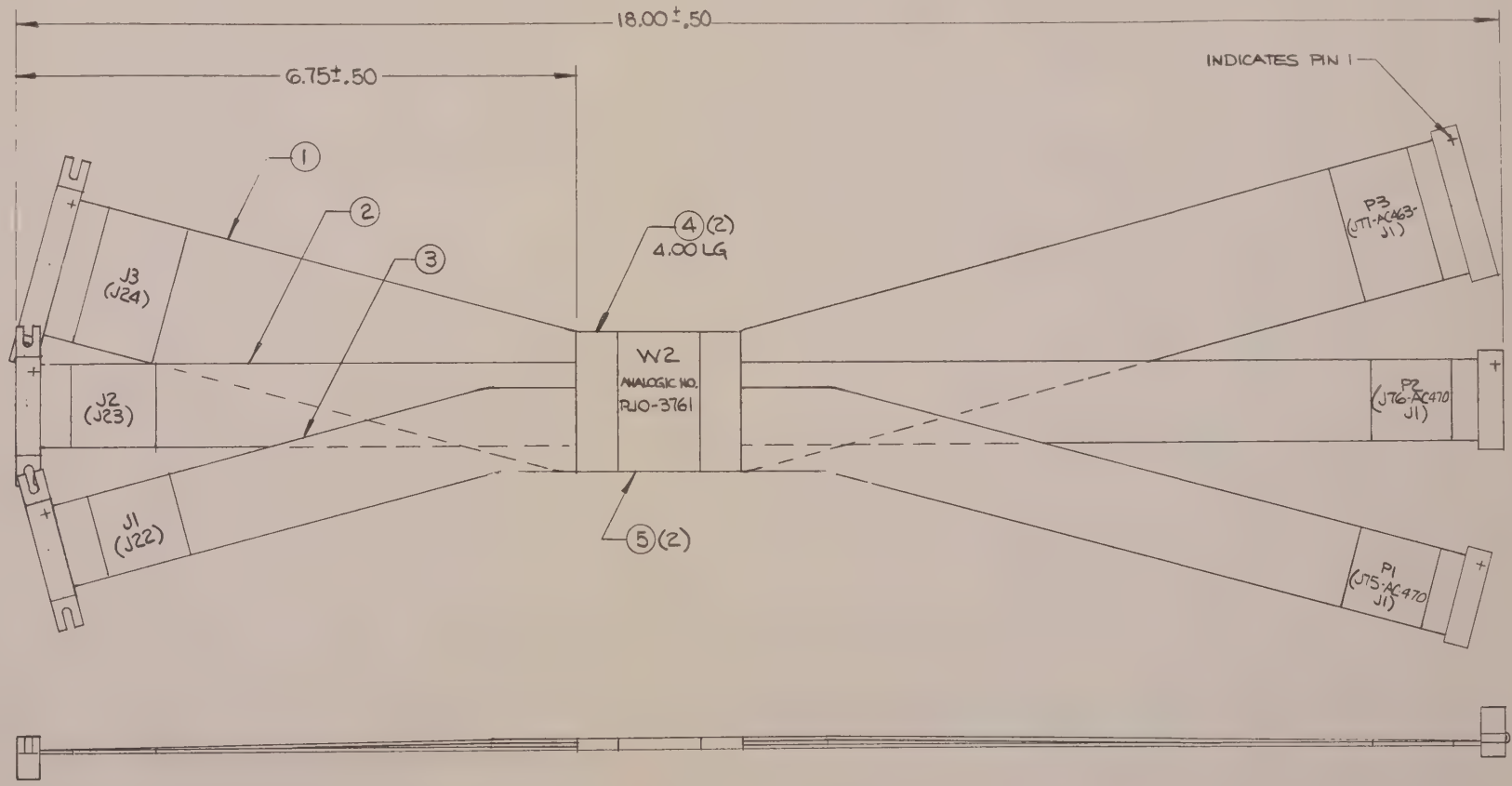
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1	4-742	SEE E.C.O	D.P	WH	7-17-80

SIZE C 7-2352 REV 1



PJO-3761	AND57000
PJO-3761	AN5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± 1.00 XXX ±
ANGLES ±
MATERIAL —
FINISH —
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	Ruby Curtis	6/22/78
CHECKED	K. E. Lunay	6/22/78
ENGINEER	DWH	6-22-78
ENGINEERING MGR.	WA	6-22-78
QUALITY CONTROL		9-18-79
PRODUCTION		9/21/79
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY, INT. (W2)

CODE IDENT NO	SIZE		REV
31814	C	7-2352	1
SCALE 1/1		SHEET 1 OF 1	

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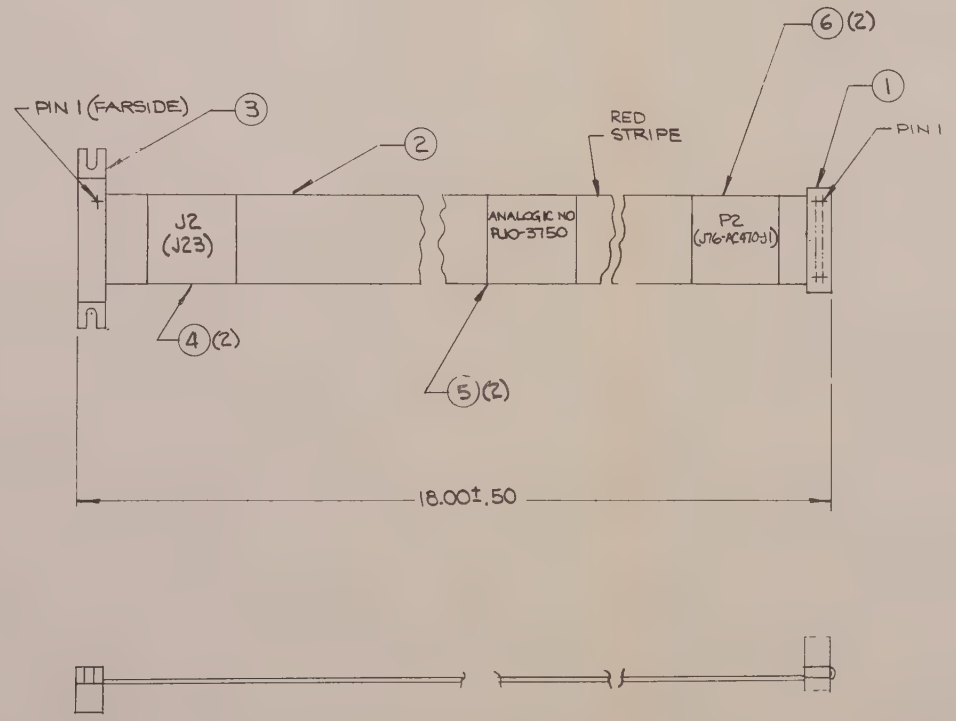
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1	4-742	SEE E.C.O.	D.P.		7-17-80

SIZE C | 7-2342 | REV 1

ITEM NO.	WIRE NO.	FROM	TO	SIGNAL
2	1	J2-1	P2-1	
1	2	-2	-2	
	3	-3	-3	
	4	-4	-4	
	5	-5	-5	
	6	-6	-6	
	7	-7	-7	
	8	-8	-8	
	9	-9	-9	
	10	-10	-10	
	11	-11	-11	
	12	-12	-12	
	13	-13	-13	
	14	-14	-14	
	15	-15	-15	
	16	-16	-16	
	17	-17	-17	
	18	-18	-18	
1	19	-19	-19	
2	20	J2-20	P2-20	



PL10-3750	AND57000
PL10-3750	AN 5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± .XXX ±
ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	Kathy Curtin	15JUN78
CHECKED	K. Z. Swain	22JUN78
ENGINEER	[illegible]	6-22-78
ENGINEERING MGR.	[illegible]	6-22-78
QUALITY CONTROL	[illegible]	7-17-80
PRODUCTION	[illegible]	8/21/79
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSY (BASIC BUFFERED, INTERNAL 20 COND.)

CODE IDENT NO	SIZE		REV
31814	C	7-2342	1

SCALE 1/1 SHEET 1 OF 1

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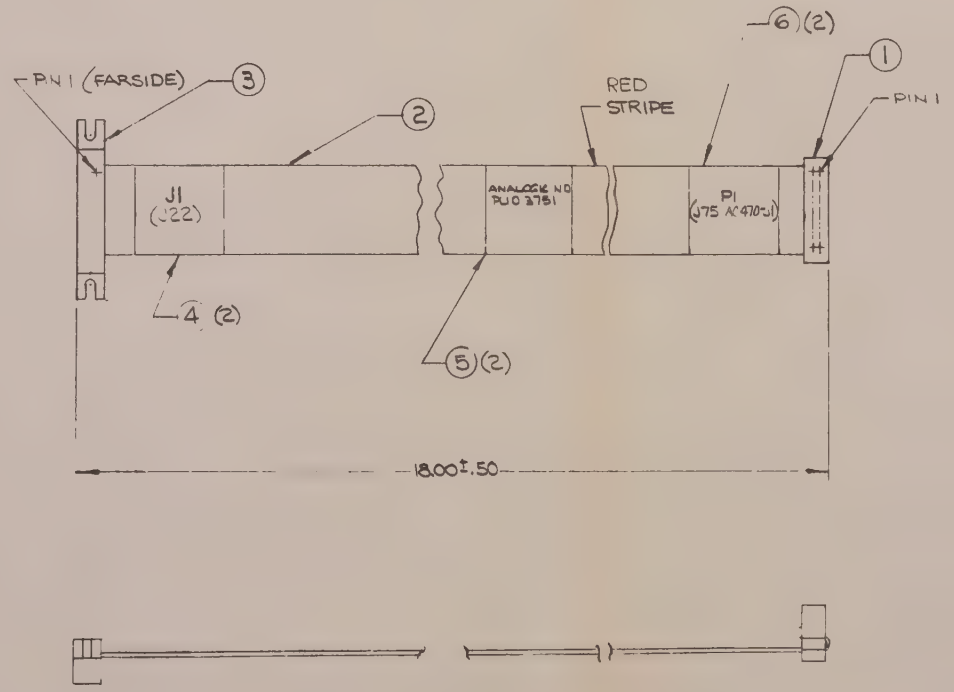
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLD	DATE
.	A-742	SEE ECO	K.T.	D.P.	7-17-80

C 7-2343 REV 1

ITEM NO.	WIRE NO.	FROM	TO	SIGNAL
2	1	J1-1	P1-1	
	2	-2	-2	
	3	-3	-3	
	4	-4	-4	
	5	-5	-5	
	6	-6	-6	
	7	-7	-7	
	8	-8	-8	
	9	-9	-9	
	10	-10	-10	
	11	-11	-11	
	12	-12	-12	
	13	-13	-13	
	14	-14	-14	
	15	-15	-15	
	16	-16	-16	
	17	-17	-17	
	18	-18	-18	
	19	-19	-19	
2	20	J1-20	P1-20	



PLIO-3751	AND57000
PLIO-3751	AN5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± .XX ± ANGLES .XXX ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	K. Curtin	15JUN78
CHECKED	R.E. Swain	22JUN78
ENGINEER	RW	6-22-78
ENGINEERING MGR	WJF	6-22-78
QUALITY CONTROL	[illegible]	9-18-79
PRODUCTION	[illegible]	9/21/79
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSY
(BASIC BUFFERED, INTERNAL 20 COND)

CODE IDENT NO	SIZE		REV
31814	C	7-2343	1
SCALE 1/1		SHEET 1 OF 1	

GENERAL PURPOSE INTERFACE for the ANDS5400

INTERFACE DESCRIPTION

The General Purpose Interface (GPI) configures the ANDS5400 Data Acquisition System to operate with a wide variety of computers. It provides 16-bit parallel transfers for instructions, status, and data. It also interprets a 4-bit operation code (OP Code), initiates the requested operations under computer control, and provides easy-to-use handshaking. The OP Codes have been assigned both to simplify software development and to maximize throughput rates when used with most computers. Some of the more common computers accomodated by the GPI are listed in the ordering guide. Figure 1 shows a typical system using the GPI.

This interface consists of three printed circuit boards that plug into slots 75, 76 and 77 of the ANDS5400 Master Chassis. Internal cabling connects these boards to three connectors mounted on the rear of the Master Chassis.

The 32 data lines, 1 control line, and 2 status lines are available in either terminated or unterminated form, as shown in Figures 2 and 3, respectively. The unterminated form can drive, and can be driven by, standard TTL/DTL, and is recommended for cabling distances of 7 feet or less. The terminated form can be used for distances of up to 60 feet when mated with similar terminations on the user interface, as shown in Figure 3.

NOTE

Nomenclature Convention: When applied to external communication, *out* refers to a flow from the user's computer to the ANDS4500; *in* refers to flow from the ANDS5400 to the user's computer.

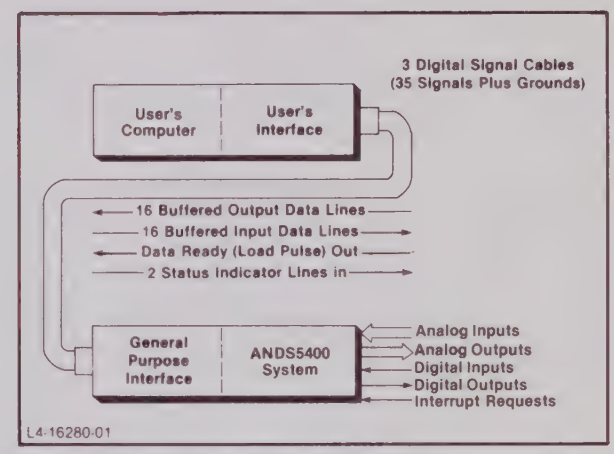


Figure 1. Typical System Block Diagram

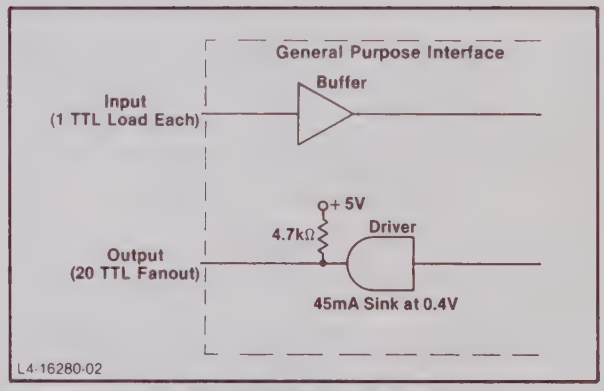


Figure 2. Unterminated Input Configuration

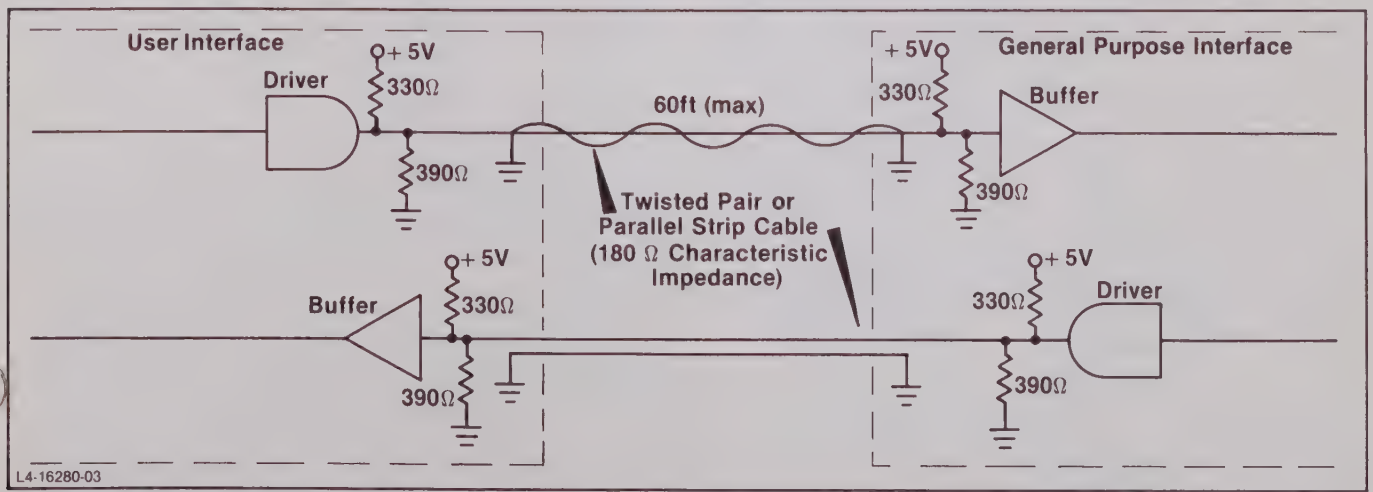


Figure 3. Optional Terminated Configuration for Interface Connections up to 60 feet Apart

ANALOGIC®

Solutions...not Slogans

OPERATION and TIMING

Data communication is via the 16 parallel buffered output data lines (BOD 1, the MSB, through BOD 16, the LSB), and via the 16 parallel buffered input data lines (BID 1, the MSB, through BID 16, the LSB). Data is true when high.

The 16-bit input word to the GPI is interpreted as a 4-bit operational code (MSB's) followed by a 12-bit data field. Table 1 identifies the functions of the eleven OP Codes that are assigned, identified octally for convenience. Table 2 identifies the control and status signals.

Timing Transmission of a command is completed by applying it to the BOD lines and then strobing the DATA READY line. The ANDS5400 accepts the command after the rising edge* of DATA READY. The minimum allowable width of this pulse is 100ns, with no maximum pulse width specification. Data must be held constant on the BOD lines for at least 500ns after the rising edge of DATA READY.

The DONE line from the GPI (and the DONE bit in the Status Register) will go low immediately after the rising edge of DATA READY and will go high when the current command is completed. The next command may be applied any time after the DONE line has risen. The elapsed time before the DONE line rises depends on the type of command given. Commands that do not initiate an A/D conversion will be done in $\approx 3\mu s$. Commands that directly initiate a conversion will be done after the conversion is complete. This time will depend on the Signal Processor and A/D converter options installed into the system, and will be from 10 to $100\mu s$.

NOTE: If a command to initiate a conversion is transmitted while the EXTERNAL TRIGGER line (A/D control) of the ANDS5400 is held low, then the DONE line will go low immediately, but the start of the conversion will be delayed until the EXTERNAL TRIGGER line rises. The DONE line will then rise after the conversion is complete. (The EXTERNAL TRIGGER input is via pin 4 of J-28). For timing with externally controlled simultaneous sample and holds, consult the ANDS5400 Manual.

The information on the BID lines supplied to the user will depend on the previous commands, and may be read any time DONE is high.

If possible, data on the BOD lines should be held static during the A/D conversion process to prevent digital noise from disturbing the analog measurement.

Bus Control OP Codes 0, 1, 2, and 3 control the internal ANDS5400 bus configuration. This operation is similar to that of a four position switch, as shown in Fig. 4. The "switch" will remain in the last position selected until an OP Code which changes the bus connection is received.

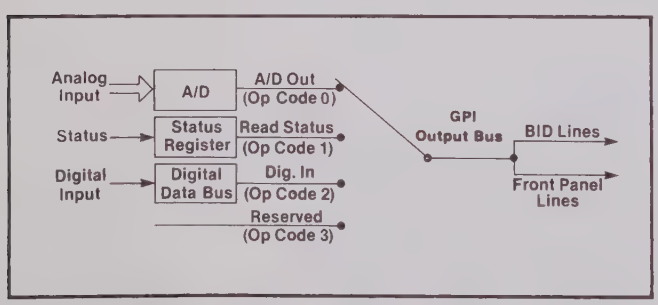


Figure 4. Bus Control OP Codes, internal ANDS5400 operation

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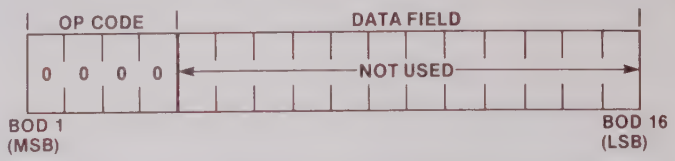
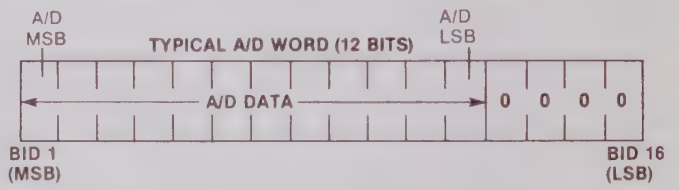
* To invert the sense of this line, simply install a jumper per the ANDS5400 Manual (AC471 schematic).

OP Code 0_8 — Read A/D Data

The format of OP Code 0 is as follows.



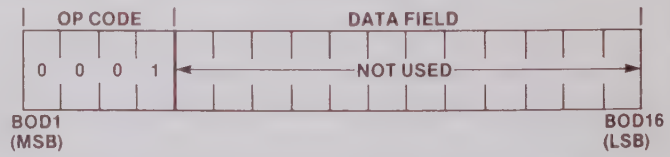
In response to receiving this OP Code and a DATA READY strobe, the GPI connects parallel A/D data (from the last analog channel selected via any of OP Codes 4, 5, 7, or 10) to the 16 BID lines. This data is left-hand justified and would appear, for a 12-bit converter, as shown.



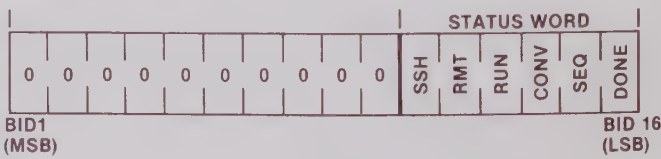
The A/D data will remain connected to the BID lines, communicating data from subsequent conversions until either OP Code 1, 2, or 3 has been received by the ANDS5400.

OP Code 1_8 — Read Status

The format of OP Code 1 is as follows.



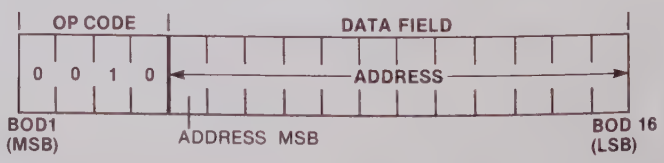
Transmitting OP Code 1 connects the ANDS5400's status register to the BID lines, in the format shown below. (The five standard and one system-optional status bits are defined on page 4.)



This data can be read by the user at any time until either OP Code 0, 2, or 3 has been received by the ANDS5400.

OP Code 2_8 — Read Digital Data

OP Code 2 should be accompanied by the address of the digital input device to be polled. Typically the address would refer either to the front panel digi-switches or to a user digital input module. This OP Code and its corresponding data word have the formats shown below.



OPERATION and TIMING

Data communication is via the 16 parallel buffered output data lines (BOD 1, the MSB, through BOD 16, the LSB), and via the 16 parallel buffered input data lines (BID 1, the MSB, through BID 16, the LSB). Data is true when high.

The 16-bit input word to the GPI is interpreted as a 4-bit operational code (MSB's) followed by a 12-bit data field. Table 1 identifies the functions of the eleven OP Codes that are assigned, identified octally for convenience. Table 2 identifies the control and status signals.

Timing Transmission of a command is completed by applying it to the BOD lines and then strobing the DATA READY line. The ANDS5400 accepts the command after the rising edge* of DATA READY. The minimum allowable width of this pulse is 100ns, with no maximum pulse width specification. Data must be held constant on the BOD lines for at least 500ns after the rising edge of DATA READY.

The DONE line from the GPI (and the DONE bit in the Status Register) will go low immediately after the rising edge of DATA READY and will go high when the current command is completed. The next command may be applied any time after the DONE line has risen. The elapsed time before the DONE line rises depends on the type of command given. Commands that do not initiate an A/D conversion will be done in ≈ 3μs. Commands that directly initiate a conversion will be done after the conversion is complete. This time will depend on the Signal Processor and A/D converter options installed into the system, and will be from 10 to 100μs.

NOTE: If a command to initiate a conversion is transmitted while the EXTERNAL TRIGGER line (A/D control) of the ANDS5400 is held low, then the DONE line will go low immediately, but the start of the conversion will be delayed until the EXTERNAL TRIGGER line rises. The DONE line will then rise after the conversion is complete. (The EXTERNAL TRIGGER input is via pin 4 of J-28). For timing with externally controlled simultaneous sample and holds, consult the ANDS5400 Manual.

The information on the BID lines supplied to the user will depend on the previous commands, and may be read any time DONE is high.

If possible, data on the BOD lines should be held static during the A/D conversion process to prevent digital noise from disturbing the analog measurement.

Bus Control OP Codes 0, 1, 2, and 3 control the internal ANDS5400 bus configuration. This operation is similar to that of a four position switch, as shown in Fig. 4. The "switch" will remain in the last position selected until an OP Code which changes the bus connection is received.

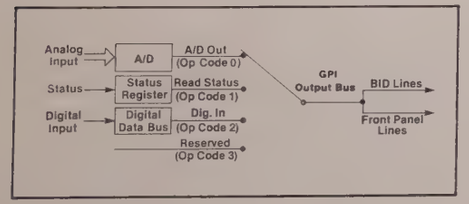


Figure 4. Bus Control OP Codes, internal ANDS5400 operation

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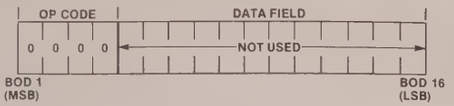
* To invert the sense of this line, simply install a jumper per the ANDS5400 Manual (AC471 schematic).

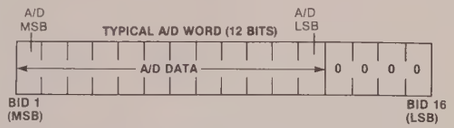
OP CODES

OP Code 0_8 — Read A/D Data

The format of OP Code 0 is as follows.



In response to receiving this OP Code and a DATA READY strobe, the GPI connects parallel A/D data (from the last analog channel selected via any of OP Codes 4, 5, 7, or 10) to the 16 BID lines. This data is left-hand justified and would appear, for a 12-bit converter, as shown.



The A/D data will remain connected to the BID lines, communicating data from subsequent conversions until either OP Code 1, 2, or 3 has been received by the ANDS5400.

OP Code 1_8 — Read Status

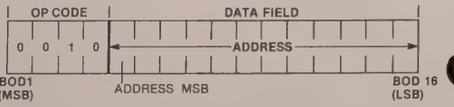
The format of OP Code 1 is as follows.

Transmitting OP Code 1 connects the ANDS5400's status register to the BID lines, in the format shown below. (The five standard and one system-optional status bits are defined on page 4.)

This data can be read by the user at any time until either OP Code 0, 2, or 3 has been received by the ANDS5400.

OP Code 2_8 — Read Digital Data

OP Code 2 should be accompanied by the address of the digital input device to be polled. Typically the address would refer either to the front panel digi-switches or to a user digital input module. This OP Code and its corresponding data word have the formats shown below.



After OP Code 2 has been received, the internal digital data bus will contain data from the addressed input source and will be connected to the BID lines (through the GPI). It will remain connected until either OP Code 0, 1, or 3 is received. However, because the internal digital data bus has multiple uses within the ANDS5400, the source of data on it will change when any other OP Code is received. Thus, after applying OP Code 2, the user should read the addressed data before applying another OP Code.

OP CODE 3_8 — Reserved

OP Code 3 can be used to connect a fourth source of digital data to the BID Lines. It is reserved for future use.

NOTE: All subsequent format diagrams in this data sheet refer to the BOD lines.

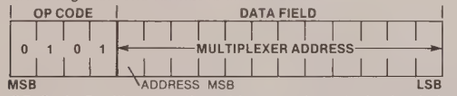
OP CODE 4_8 — Load Range *(with convert and sequence options)*

OP Code 4 should be accompanied by the range information to be loaded into the ANDS5400 range register. The format is shown below.

OP Code 4 will cause the range register to be loaded with the new range information and, based on the control bits of the status register, may also cause a conversion to begin and may cause the multiplexer address to be incremented after the conversion is completed. Once loaded, the range register will retain the information until modified by the user.

OP CODE 5_8 — Load Address *(with convert and sequence options)*

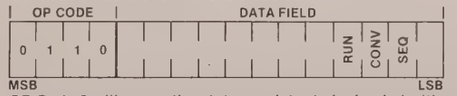
OP Code 5 should be accompanied by the address information to be loaded into the ANDS5400 multiplexer address register. The format is shown below.



OP Code 5 will cause the address register to be loaded with the new address information and, based on the control bits of the status register, may cause a conversion to begin and may cause the multiplexer address to be incremented after the conversion is completed.

OP CODE 6_8 Load Status

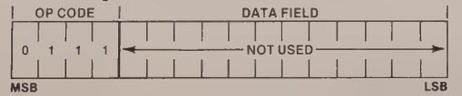
OP Code 6 has the format shown below.



OP Code 6 will cause the status register to be loaded with new information for the Run, Convert, and Sequence Bits. These bits are defined on page 4.

OP CODE 7_8 — Convert *(with sequence option)*

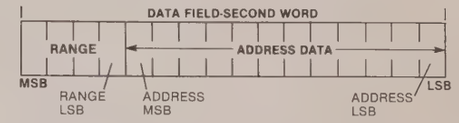
OP Code 7 will cause a conversion cycle to begin on a previously addressed channel and may, based on a control bit in the status register, cause the multiplexer address to be incremented after the conversion is completed. It has the following format.



OP CODE 10_8 — Load Range & Address *(with convert and sequence options)*

OP Code 10 is a two-stage command. The first word will contain OP Code 10 and an unused data field as shown below.

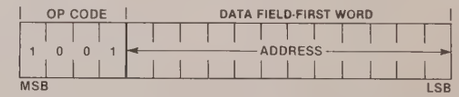
Reception of OP Code 10 will cause the interface to interpret the next word received as combined range **and** address information, formatted as shown below.



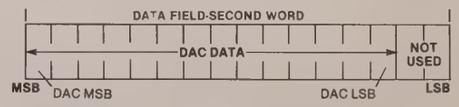
The information in the second word will be loaded into the range and address registers and, depending on the control bits of the status register, may cause a conversion to begin and may cause the address register to be incremented after the conversion is completed. **It is important to note that OP Code 10 is a two-stage command. After an "OP code 10 word" is recieved, the next word is always interpreted as a "range and address data word".** If, inadvertantly, the next word received were a new OP code command, the new OP code would not be executed, but rather the range and address registers would be loaded with spurious information. (See also the recommended procedure for initialization).

OP CODE 11_8 — Load DAC or Load Digital Data

OP Code 11 is also a two-stage command. The first word will contain OP Code 11 and the address of the DAC or digital output module to be loaded, as shown below.



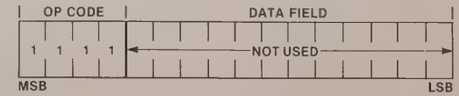
The next word received will be interpreted as digital data to be loaded into the previously addressed DAC or digital output module. For DAC's, the data is left-hand justified, appearing as shown below for a 14-bit DAC. **The cautions regarding the two-stage nature of OP Code 10 also apply to OP Code 11.**



OP CODES 12_8 thru 16_8 —*Not Used*

OP CODE 17_8 — Clear

OP Code 17 does not require a data field, as shown below. It performs a general clearing and resetting function throughout the ANDS5400.



CONTROL and STATUS SIGNALS

When equipped with a GPI, the ANDS5400 provides a read/write status register plus two status lines and one control line. The functions of each are summarized below.

STATUS REGISTER BITS

The status register provides control over three functions of the ANDS5400 and indicates the status of three others. Its format was shown earlier. It may be read by using OP Code 1, and may be loaded by using OP Code 6, both also described earlier. Only the RUN, CONV, and SEQ bits can be loaded. The SSH, RMT, and DONE bits are 'Read Only' system indicators. The interpretation of the bits in the status register is as follows:

SSH (Simultaneous Sample and Hold)—*system option.* This bit is used to indicate the status of the Simultaneous Sample and Hold Amplifiers' control logic. It is set high when the amplifiers are "Ready to Hold", awaiting an EXTERNAL HOLD. It goes low to indicate that the SSH Amplifiers are in 'Hold' and action is required by the host computer to scan the affected channels. See the ANDS5400 Manual.

RMT (Remote) This bit is a reflection of the ANDS5400 front panel indicator light and is high when the system is in remote (computer) control.

RUN This is a read/write control bit and can be used to prevent the system from being put into local control. If the system is in remote control, and if the RUN bit is set high, then the system cannot be placed into local control, and the front panel controls are effectively locked out.

CONV (Convert) This is a read/write control bit which, if set high, will cause an A/D conversion to take place when OP Codes 4, 5, and 10 are received.

SEQ (Sequence) This is a read/write control bit which, if set high, will cause the multiplexer address to be incremented at the end of a conversion cycle. This bit may be used alone (OP Code 7) or in conjunction with the convert bit (OP Codes 4, 5, and 10).

DONE This bit is a reflection of the DONE line from the GPI and will go high after each command to the interface is complete.

DATA READY LINE — See Operation and Timing

DONE LINE — See Operation and Timing

54RQST LINE

This line goes high within 5μs after a user card generates an interrupt request, remaining high until the user services the request. Refer to the ANDS5400 software documentation for reading the interrupt vectors.

If multiple requests are pending, *i.e.,* other cards interrupt before the line goes low or more than one card interrupts simultaneously, the line will go low for a minimum of 1μs as each request is serviced. The rising edge of the request line is used to initiate each new interrupt.

To determine if there are other interrupts pending, the user must either issue an OP Code 2 to a new address, or issue an OP Code 11. It is recommended that the data from the interrupting card always be read immediately (OP Code 2). This act of servicing the interrupt automatically re-enables the ability to read other interrupts that may be pending.

QUICK REFERENCE GUIDE

This page summarizes in convenient format key user information, including OP Codes, Control & Status Signals and recommended procedures.

Table 1.
General Purpose Interface
OPERATION CODES

OP Code (Octal)	Function	Data Field	Options*
0	Read A/D Data		
1	Read Status		
2	Read Digital Data	Address	
3	Reserved		
4	Load Range	Range	Convert and/or Sequence
5	Load Address	Address	Convert and/or Sequence
6	Load Status	Status	
7	Convert		Sequence
10	Load Range & Address	Range and Address (total of two words)	Convert and/or Sequence
11	Load DAC Data & Address (or Load Digital Data)	Address and Data (total of two words)	
12 to 16 inclusive	Not Used		
17	Clear		

*These optional functions will be executed by the OP Code if the corresponding control bits in the STATUS REGISTER are set

Table 2.
General Purpose Interface
CONTROL and STATUS SIGNALS

Signal	Function	Direction
DATA READY	Strobes data on BOD lines into the General Purpose Interface	Out
DONE	Indicates last command has been completed and the ANDS5400 is ready to accept the next command	In
54RQST	Interrupt request — indicates that a user module has requested service from the user's computer	In

RECOMMENDED PROCEDURES

Initialization. During power turn-on of the ANDS5400 and the user's interface, it is possible that the GPI may initialize in a state in which it anticipates receiving the second half of a two-stage OP Code. Thus, it is advisable to begin any program with two OP Code 17 (CLEAR) commands. The first CLEAR will act as the second half of the 2-stage instruction, and the next CLEAR will perform the resetting function.

Bus Control. In most cases the system will be used for predominately A/D input, therefore it is recommended that the user adopt the following procedure: after completion of an OP Code 1 or 2 function, transmit OP Code 0 to reconnect the A/D data to the BID lines.

Two stage commands. When using OP codes 10 and 11, it is recommended that the DONE signal be tested for completion separately after each 16 bit transmission.

Table 3.
General Purpose Interface
REAR PANEL CONNECTIONS

J22				J23				J24			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	BID 1 (BID MSB)	2	BID 2	1	BID 9	2	BID 10	1	Digital Ground	2	Digital Ground
3	BID 3	4	BID 4	3	BID 11	4	BID 12	3	Not Used	4	Digital Ground
5	BID 5	6	BID 6	5	BID 13	6	BID 14	5	DONE	6	Digital Ground
7	BID 7	8	BID 8	7	BID 15	8	BID 16 (LSB)	7	Not Used	8	Digital Ground
9	BOD 1 (BOD MSB)	10	BOD 2	9	BOD 9	10	BOD 10	9	Not Used	10	Digital Ground
11	BOD 3	12	BOD 4	11	BOD 11	12	BOD 12	11	Not Used	12	Digital Ground
13	BOD 5	14	BOD 6	13	BOD 13	14	BOD 14	13	Not Used	14	Digital Ground
15	BOD 7	16	BOD 8	15	BOD 15	16	BOD 16 (LSB)	15	DATA READY	16	Digital Ground
17	Digital Ground	18	Digital Ground	17	Digital Ground	18	Digital Ground	17	54RQST	18	Digital Ground
19	Digital Ground	20	Digital Ground	19	Digital Ground	20	Digital Ground	19	Not Used	20	Digital Ground

Unterminated option: all inputs are standard TTL voltage with 1 unit load; all outputs are standard TTL with 20 unit fanout.
Terminated option: termination elements for inputs and outputs are as defined in Figure 3.

INTERCONNECTION NOTE

Ribbon mass termination mating connectors for J22, J23, and J24 are supplied. Most applications will require a transition from ribbon cable to some other form of wiring before connecting to the computer. *Potential cross coupling of signals can be minimized* by implementing this transition **as close to the computer** as possible. When operating over long distances (10 to 60 feet), cross coupling may be further minimized by the use of twisted pairs (one lead from each pair should be grounded).

PROGRAMMING NOTE

The host processor can drive the GPI via relatively simple software. Typical application programs are shown in a separate document, "GPI Programming Examples."

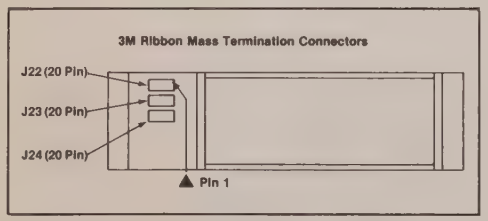


Figure 5. Interface Connector Locations on ANDS5400 Rear Panel

ORDERING GUIDE

For an ANDS5400 System, complete with a General Purpose Interface, simply specify

ANDS5400 — □ — B — □ — □
(Enter Power Supply Code see seperate configuration guide) — *Enter*

PDP11/LSI11 compatible via DR11C/DRV11	23
HP2100/21MX/1000 compatible via 12566B-002	24
General Automation SPC16 via General Purpose Input/Output Interface	25
Texas Instruments 990 via the CRU Interface	26
Modular Computer via 4805 General Purpose Interface	27
Interdata 3, 4, 5, 70, 7/16 + 8/16 via M48-013ULI	28
Computer Automation via 13213-00 16 bit I/O Module	29
Nova/Eclipse via 4066 (4065) Digital Interface Module	32
General Purpose Interface	34

Enter

Unterminated I/O	A
Terminated I/O	B

For interfaces to HP98 series calculators (with the 98032A Interface) and to other machines not listed above, contact your Analogic Representative.

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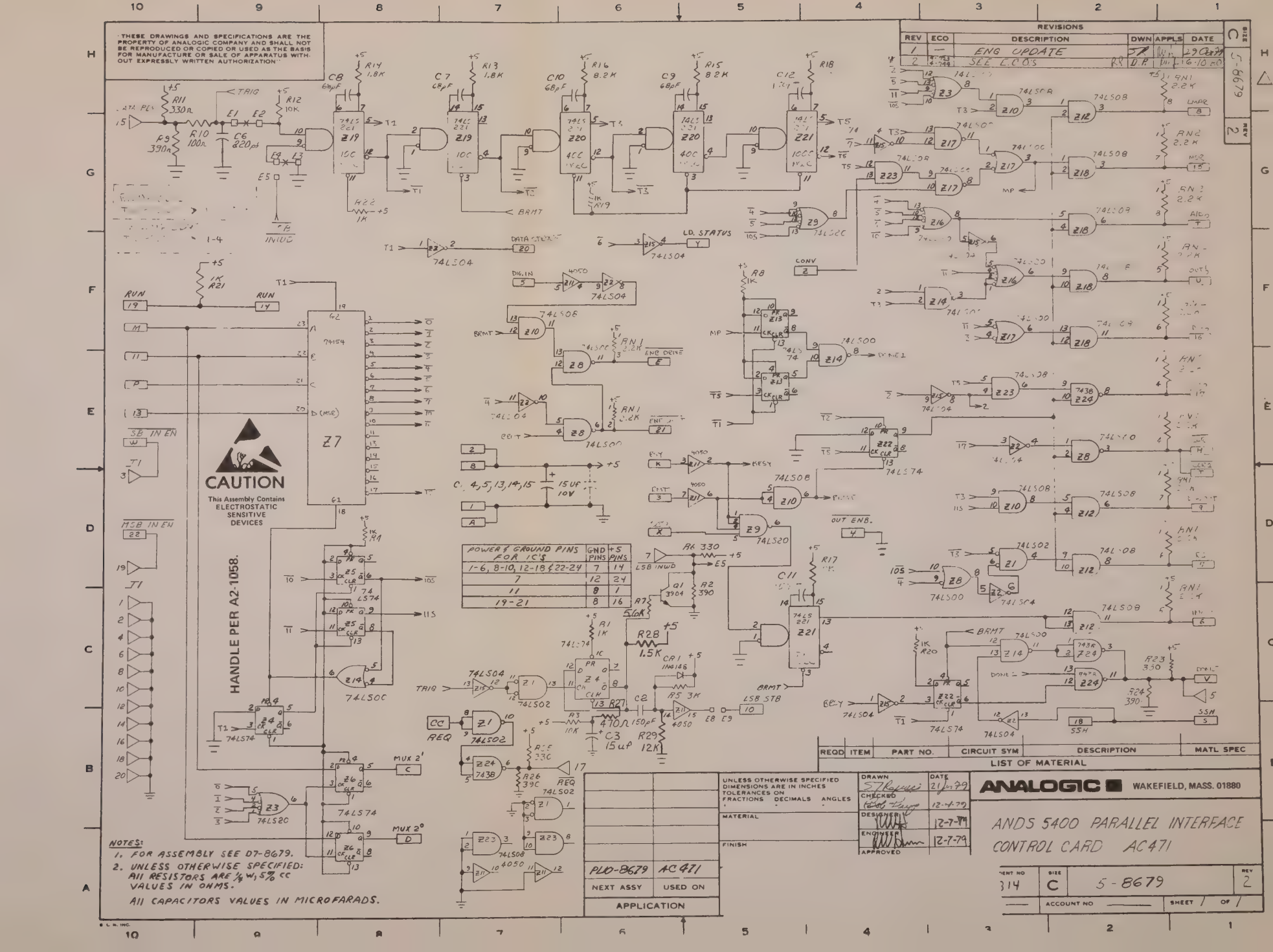
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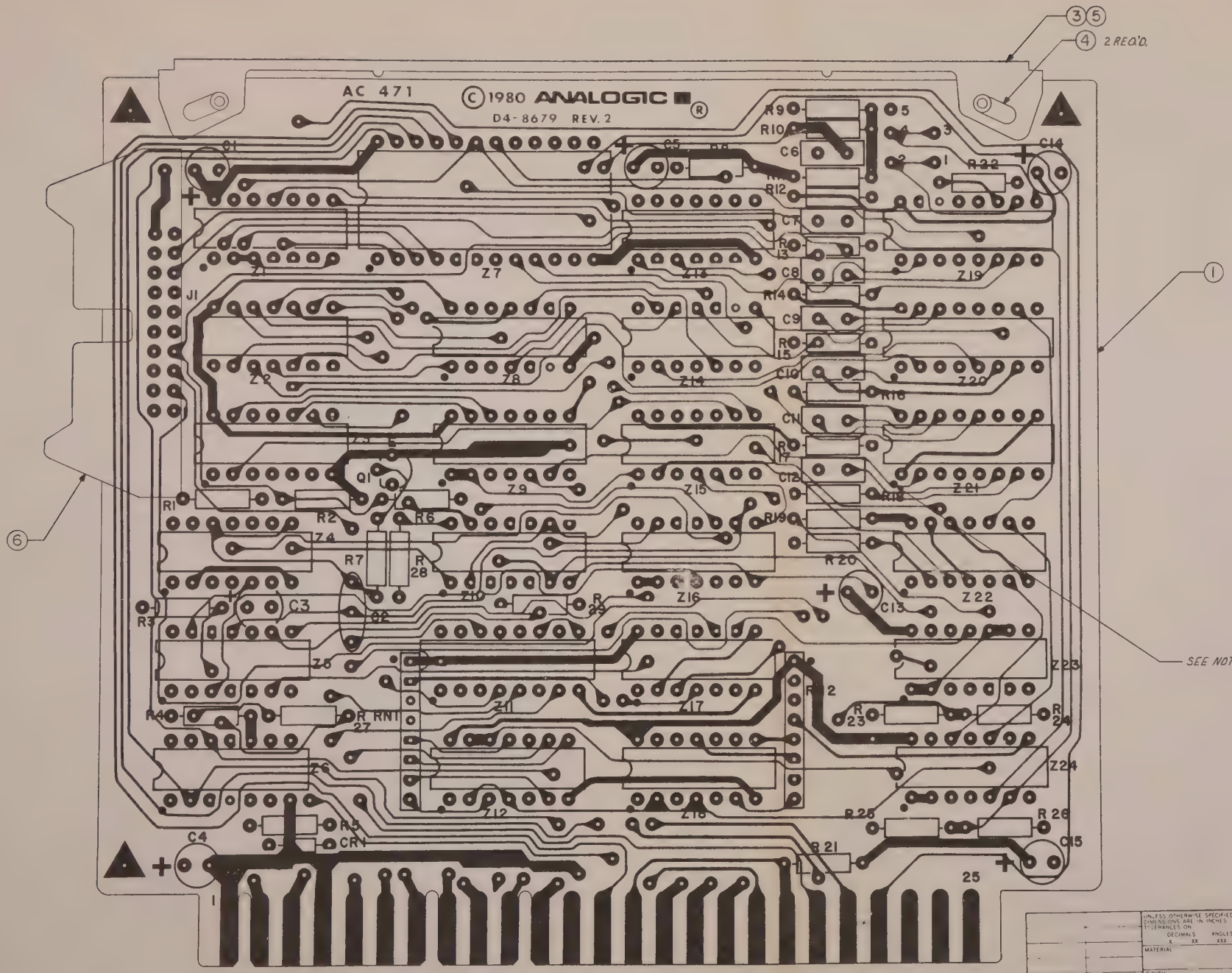
REVISIONS
REV | ECO | DESCRIPTION | DWN | APPLS | DATE
1 | — | ENG UPDATE | | | 29 Oct 79
2 | 4-743 4-744 | SLE E.C.O.s | | | 6-10-80
SIZE C 5-8679 REV 2
CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
Z7
74154
POWER & GROUND PINS FOR IC'S | GND PINS | +5 PINS
1-6, 8-10, 12-18 & 22-24 | 7 | 14
7 | 12 | 24
11 | 8 | 1
19-21 | 8 | 16
NOTES:
1. FOR ASSEMBLY SEE D7-8679.
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE 1/4 W, 5% CC VALUES IN OHMS.
ALL CAPACITORS VALUES IN MICROFARADS.
REQD | ITEM | PART NO. | CIRCUIT SYM | DESCRIPTION | MATL SPEC
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
DRAWN S.T. Kawai 21 Jun 79
CHECKED 12-4-79
DESIGNER 12-7-79
ENGR 12-7-79
APPROVED
PLO-8679 AC471
NEXT ASSY USED ON
APPLICATION
ANALOGIC WAKEFIELD, MASS. 01880
ANDS 5400 PARALLEL INTERFACE CONTROL CARD AC471
DRAWING NO 314 SIZE C 5-8679 REV 2
ACCOUNT NO SHEET 1 OF 1



REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPLS	DATE	
2	4723 4744		RP	DP	11-16-80	

D 7-8679 2

NOTES:
1. FOR SCHEMATIC SEE C5-8679.
2. DOT INDICATES PIN 1 OF I.C.'S AND R.N.'S.
3. ASSEMBLE PER A2-1027.
4. MAXIMUM COMPONENT HEIGHT TO BE .500"

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

COMPONENT SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON DECIMALS X .1 XX .01 XXX .005 ANGLES 1°	DRAWN S.T. REPUCCI	DATE 11-1-79	ANALOGIC WAKEFIELD, MASS. 01880
	CHECKED R. ROSS	11-29-79	ASSEMBLY
MATERIAL	ENGINEER R.W. HAVENER	12-7-79	ANDS 5400 PARALLEL INTERFACE CONTROL CARD AC 471
FINISH	ENGINEERING MGR R.W. HAVENER	12-7-79	
PL10-8679 AC 471	QUALITY CONTROL		CODE IDENT NO 31814 SIZE D 7-8679 REV 2
NEXT ASSY USED ON	APPLICABLE SPECIFICATIONS	PRODUCTION	SCALE 4:1 SHEET OF
APPLICATION		WEIGHT	

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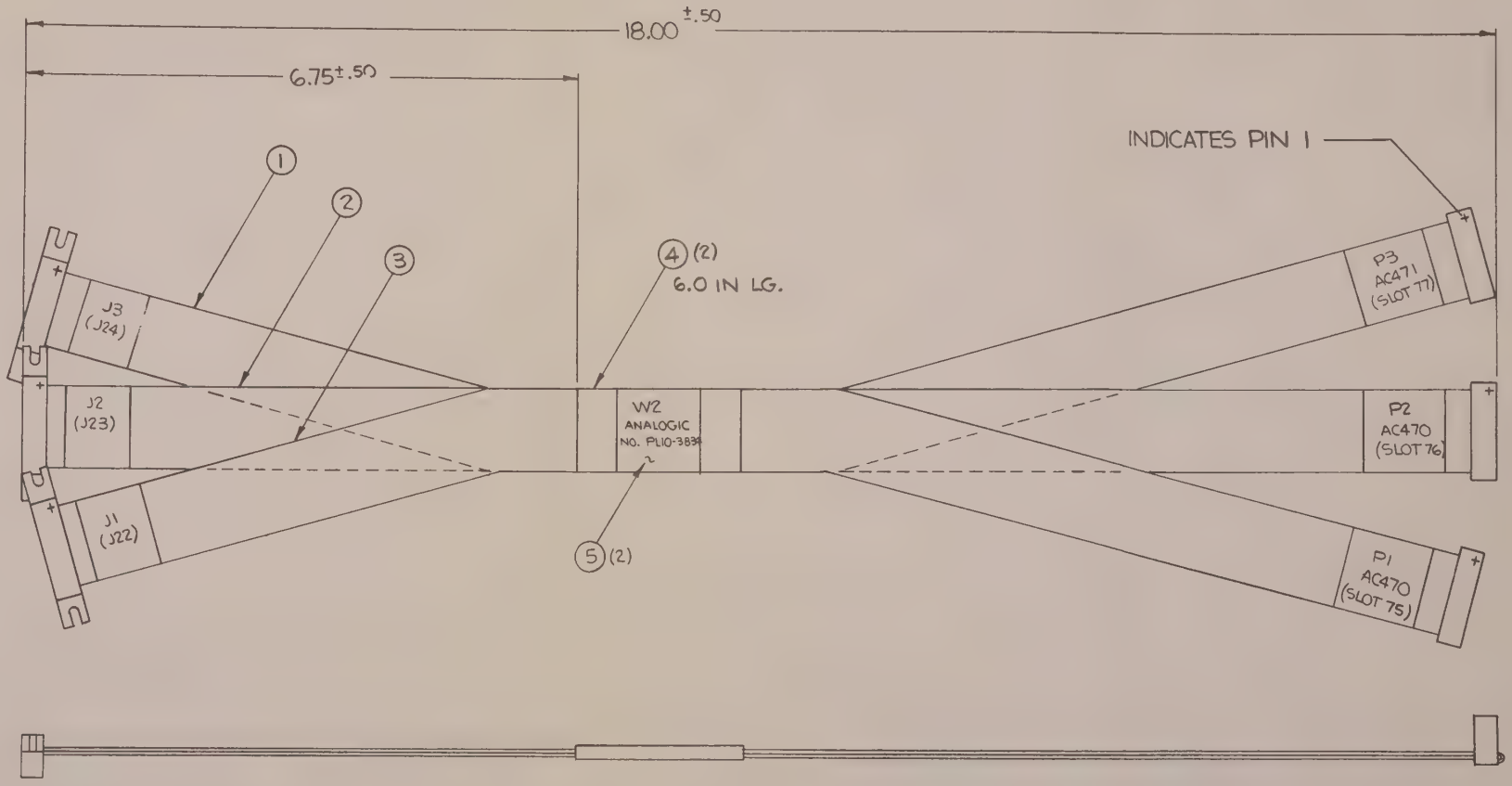
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C 7-2387 REV O



PL10-3834	AND5400
PL10-3834	AN5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± .XXX ±
ANGLES

MATERIAL: N/A

FINISH: N/A

APPLICABLE SPECIFICATIONS

DRAWN		12-5-79
CHECKED		12-7-79
ENGINEER		12-7-79
ENGINEERING MGR.		12-7-79
QUALITY CONTROL		
PRODUCTION		
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY (INT.)

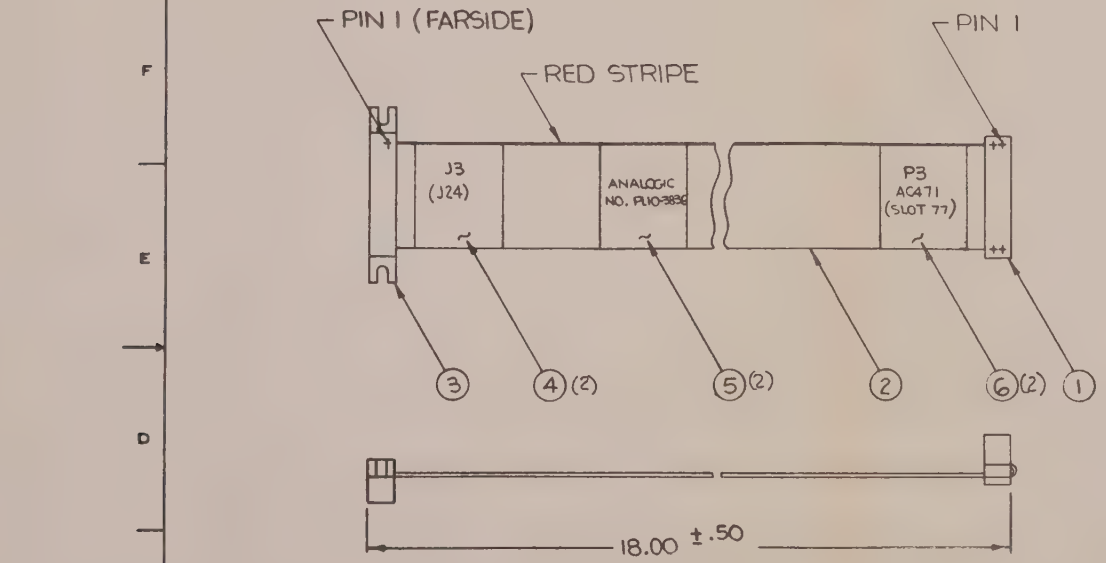
CODE IDENT NO	SIZE		REV
31814	C	7-2387	O

SCALE 1/1 SHEET 1 OF 1

"THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF ANALOGIC COMPANY AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION."

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C 7-2389 REV O



NOTES:

1. ALL WIRING IS STRAIGHT BUS (EG PIN 1 TO PIN 1)

PL10-3836	AND55400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: X ± .1, XX ± .01, XXX ± .005
ANGLES ±

MATERIAL: N/A

FINISH: N/A

APPLICABLE SPECIFICATIONS

		DATE
DRAWN	A.H. Bailey	12-5-79
CHECKED	Bob Berry	12-7-79
ENGINEER		12-7-79
ENGINEERING MGR.		12-7-79
QUALITY CONTROL		
PRODUCTION		
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY

CODE IDENT NO	SIZE		REV
31814	C	7-2389	O
SCALE N/A		SHEET 1 OF 1	

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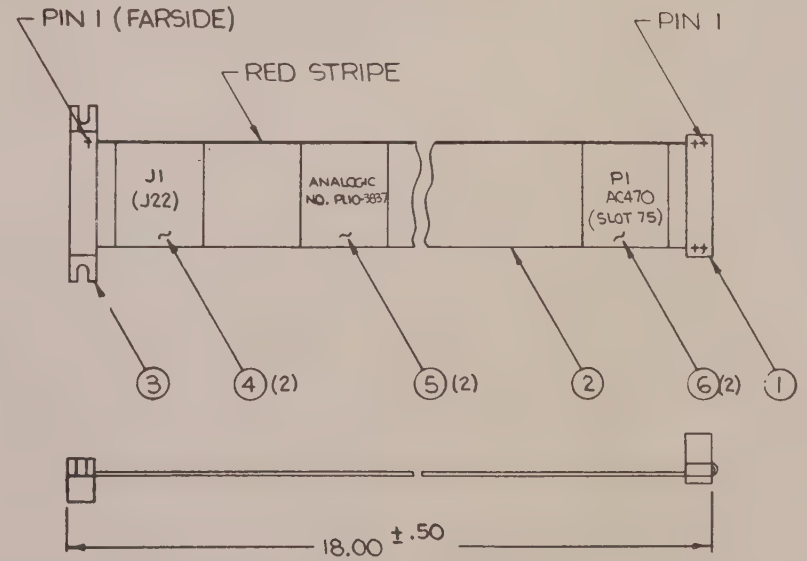
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C | 7-2390 | REV O



NOTES:

1. ALL WIRING IS STRAIGHT BUS (EG PIN 1 TO PIN 1)

PL10-3837	AND5S400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± .XX ± .XXX ± ANGLES ±

MATERIAL: N/A

FINISH: N/A

APPLICABLE SPECIFICATIONS

		DATE
DRAWN	A.P. Bailey	12-5-79
CHECKED		12-7-79
ENGINEER		12-7-79
ENGINEERING MGR.		12-7-79
QUALITY CONTROL		
PRODUCTION		
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSEMBLY

CODE IDENT NO	SIZE		REV
31814	C	7-2390	O

SCALE N/A SHEET 1 OF 1

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ASYNCHRONOUS SERIAL LINE INTERFACE

FOR AN5400

GENERAL

The Asynchronous Serial Line Interface (ASLI) provides the basic AN5400 Data Acquisition and Distribution System with the capability of operating remotely from some controlling device, such as a mini-computer, at any of a wide range of data rates. Data is transferred to and from the AN5400 using ASCII character strings. This enables the AN5400 to be used with commonly used devices; it may even be operated directly from a teletype.

The ASLI interface will operate for short distances via RS232-C or 20 mA current loops. For long distances and high baud rates, the ASLI will be used with a modem or dedicated lines via RS-422.

PHYSICAL

The ASLI is constructed on three standard AN5400 System modules located in slots 75, 76, and 77. The serial line is cabled internally from one interface module to the rear connector.

BAUD RATE

Data rate is selectable by a small PC-mounted switch to be one of the following:

110 baud
150 baud
300 baud
600 baud
1200 baud
2400 baud
4800 baud
9600 baud
19200 baud

Baud rate is derived from a source clock, stable to better than ±0.01%.

TRANSMISSION MODE

The ASLI will operate in full duplex with the format shown in Figure 1.

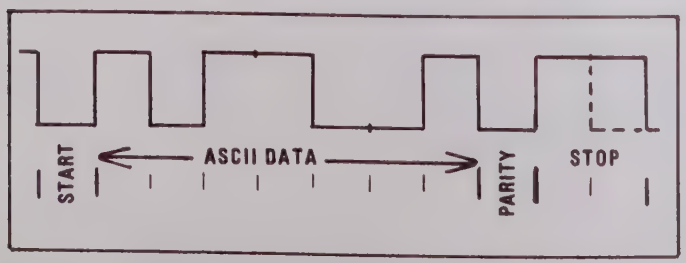

Figure 1. Character format for ASLI interface.

A mark-to-space transition signifies the start of a character. The character consists of one start bit, seven data bits, one parity bit, and one or two stop bits. Data will be received with the same format. Parity may be even, odd, or disabled, as programmed by a PC mounted switch. The number of stop bits (one or two) is also switch selectable.

STATUS REGISTER

A three bit register is provided for system debugging that will show the operational state of the AN5400. The three bits will indicate; **protocol mode,** front panel **lockout,** and **remote** or **local** operation, as shown in Figure 2.

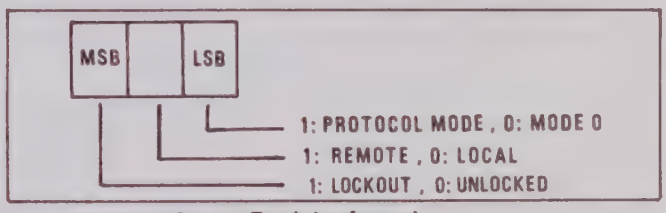

Figure 2. ASLI Status Register format.

The status register output may be transmitted on the 0 or W command, and is sent as an ASCII 0 thru 7.

Reading the register has no effect on its contents.

ERROR REGISTER

The ASLI also contains a three-bit error register for diagnostic purposes. The three bits indicate; **overrun** error, **parity** error, and **framing** error as shown in Figure 3. If an error occurs, it will set the appropriate bit high until the error register is transmitted. After transmission, all error bits are reset automatically. The error register is read using an "N" or "V" command, and is sent as an ASCII 0 thru 7.

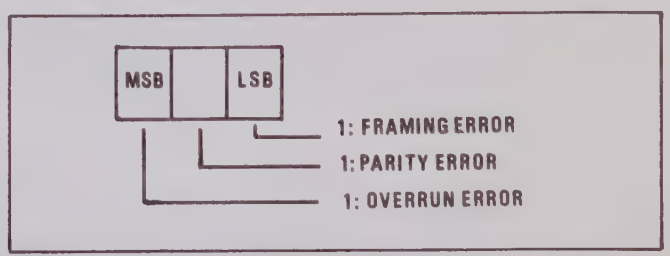

Figure 3. ASLI Error Register format.

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PROTOCOL MODE

The ASLI may function under either of two optional protocols; Mode 0 or Mode 1. In **Mode 0** all data and command characters will be echoed. All other ASCII characters, including data control characters, will not be echoed. Also, data from the AN5400 will be transmitted in octal blocks only upon receipt of the command for that block. See note below.

In **Mode 1,** only command characters B, @, F, I, M, N, and O will be echoed. The ASLI will respond to all data and command characters but not to data control characters. When characters B, @, F, I, M, N, or O are received they will be echoed as soon as past data is transmitted, and the data generated will be transmitted automatically in one 6 character block, or one character in the cases of error, and status. **Mode 0** may be used in applications requiring error checking and correction. **Mode 1** may be used where greater thruput is required.

CHARACTER DEFINITIONS

1. Data Characters
"**d**" is used to indicate an ASCII character 0 thru 7. "**u**" is used to indicate an ASCII character 0 or 1. Each character is an octal data block.

2. Command Characters
Command characters cause the AN5400 to perform the indicated operation. See Table 1.

3. Data Control Characters
These characters cause data from the AN5400 to be transmitted one octal block at a time, permitting redundancy and variable data resolutions. See Table 2.

4. All other characters have no effect on the AN5400, are not echoed by the ASLI, and are reserved as to their possible use.

Table 1.
ASLI COMMAND CHARACTERS

Data Field	Char.	Description
	@	Read digital data
dddd	A	Load D/A address
dddd	B	Load A/D address, measure
	C	Clear
uddddd	D	Load digital data
	E	Mode 0 (echo)
uddddd	F	Load range, address, measure
ud	G	Load range
	H	Mode 1 (high speed)
	I	Increment, Measure
	J	Unlock front panel
	K	Master clear
	L	Lock out front panel
	M	Measure
	N	Read error reg.
	O	Read status reg.

Characters A, B, D, F, and G must be preceded by a data field of length indicated. The ASLI accepts only the last characters sent if the data field is overfilled.

Table 2
DATA CONTROL CHARACTERS *

Character	Description
P	Read Data MSB (u)
Q	Read 10,000's (d1)
R	Read 1,000's (d2)
S	Read 100's (d3)
T	Read 10's (d4)
U	Read 1's (d5)
V	Read Error register
W	Read Status register

Only used in Protocol Mode 0

Note: The Error and Status register outputs are transmitted immediately after "N" and "O" are echoed, respectively, in either protocol mode. In Mode 0, V and W may also be used, but without being echoed.

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Cincinnati, Ohio (606) 371-0064

AVAILABLE FROM:

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

D 5-8682 0

DIN RB1 RB2 RB3 TB1 TB2 TB3

Z11 C174 · Z19 C174 · Z20 C174 · Z21 C173 · Z17 C173 · Z13 C173 · Z9 C173 · Z5 C173 · Z1 C173

Z15 80C97 · Z24 80C97 · Z23 80C97 · Z16 80C97

Z22 C157 · Z18 C157 · Z14 C157 · Z10 C157 · Z7 74C42 · Z9 74C00 · Z3 74C00 · Z8 C163

ERE SRE

A/D DATA

POWER PINS						
REF DES	I.C. TYPE	+5	DIG GROUND	ANA GROUND	-15	+15
Z1,2	74C74	14	7			
Z15,16,23 Z9	80C97	16	8			
Z3,9	74C00	14	7			
Z7	74C42	16	8			
Z10-14, 18,22	74C157	16	8			
Z8	74C163	16	8			
Z5,6,9 13,17,21	74C173	16	8			
Z1,6,15,20	74C174	16	8			

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

CLOCK SND SRD EOS DONE MODE SEQ ECHO

TRN DKT

P2 RIBBON CAN. J1 MOTHER BD. CON

DIGITAL BUSS

SPARES

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-8682	AC 474
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES

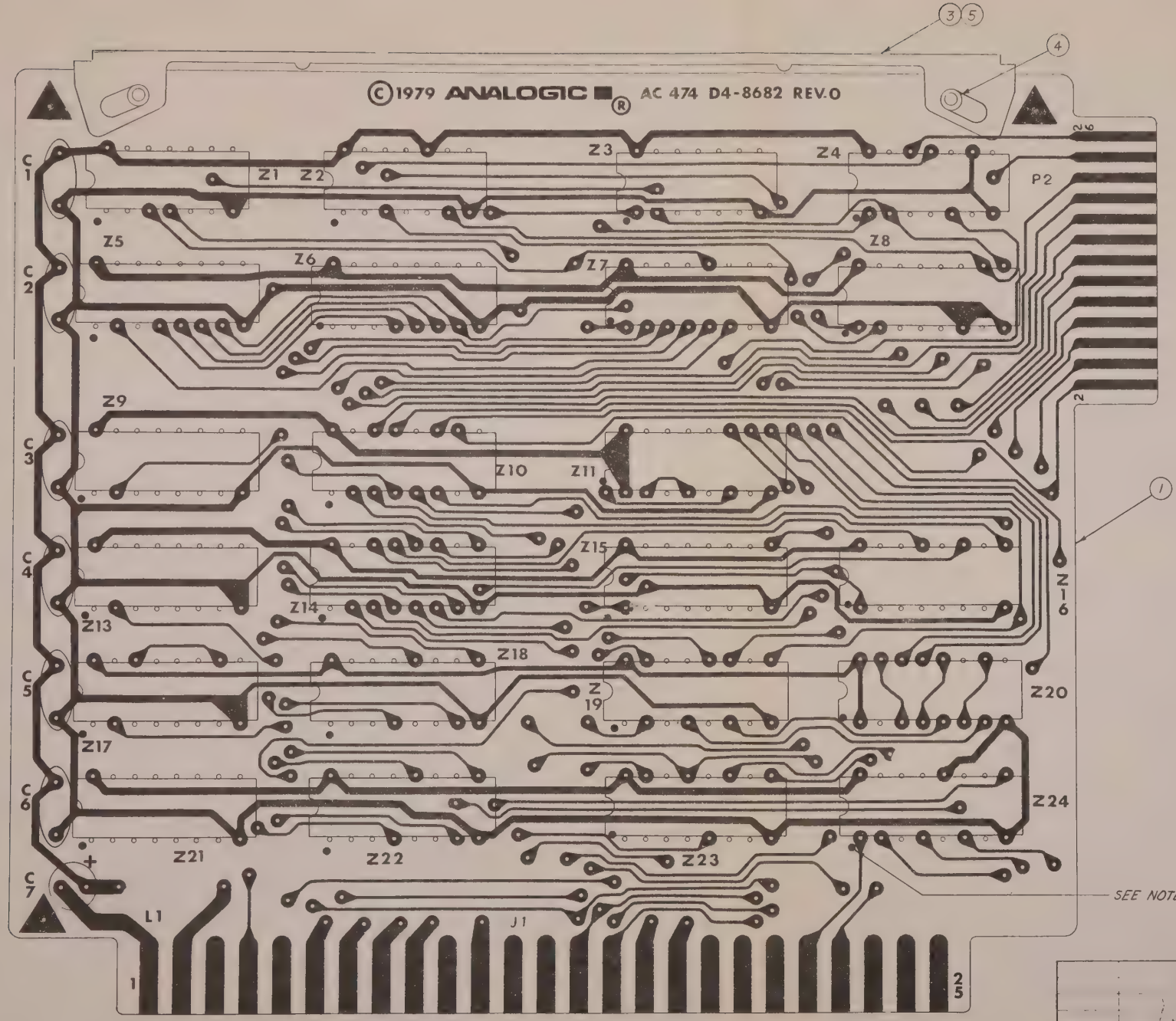
MATERIAL · FINISH · APPLICABLE SPECIFICATIONS

DRAWN	L. MULLER	7-5-77
CHECKED		4/8/80
DESIGNER	L. Muller	4/11/80
ENGINEER		4-11-80
APPROVED		
RELEASED		
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC
AND5400 ASYNCHRONOUS SERIAL LINE INTERFACE DATA CARD AC 474

CODE IDENT NO.	SIZE		REV
31814	D	5-8682	0
SCALE —	ACCOUNT NO.		SHEET 1 OF 1



REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE

D 7-8682 REV O

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

NOTES:
1. FOR SCHEMATIC SEE DS-8682
2. DOT INDICATES PIN 1 OF I.C.'S.
3. ASSEMBLE PER A2-1027.

COMPONENT SIDE

PL10-8682 AC474 APPLICATION		57 Rpcs. ea 13 Sep 79 Robert Foley 4/9/80 L. Mueller 4/11/80 [illegible] 4-11-80	ANALOGIC MARKET E.S. MASS. 01880 ASSEMBLY SERIAL LINE INTERFACE DATA BOARD AC474 31814 D 7-8682 REV O SCALE 4:1 ACCOUNT NO SHEET 1 OF 1

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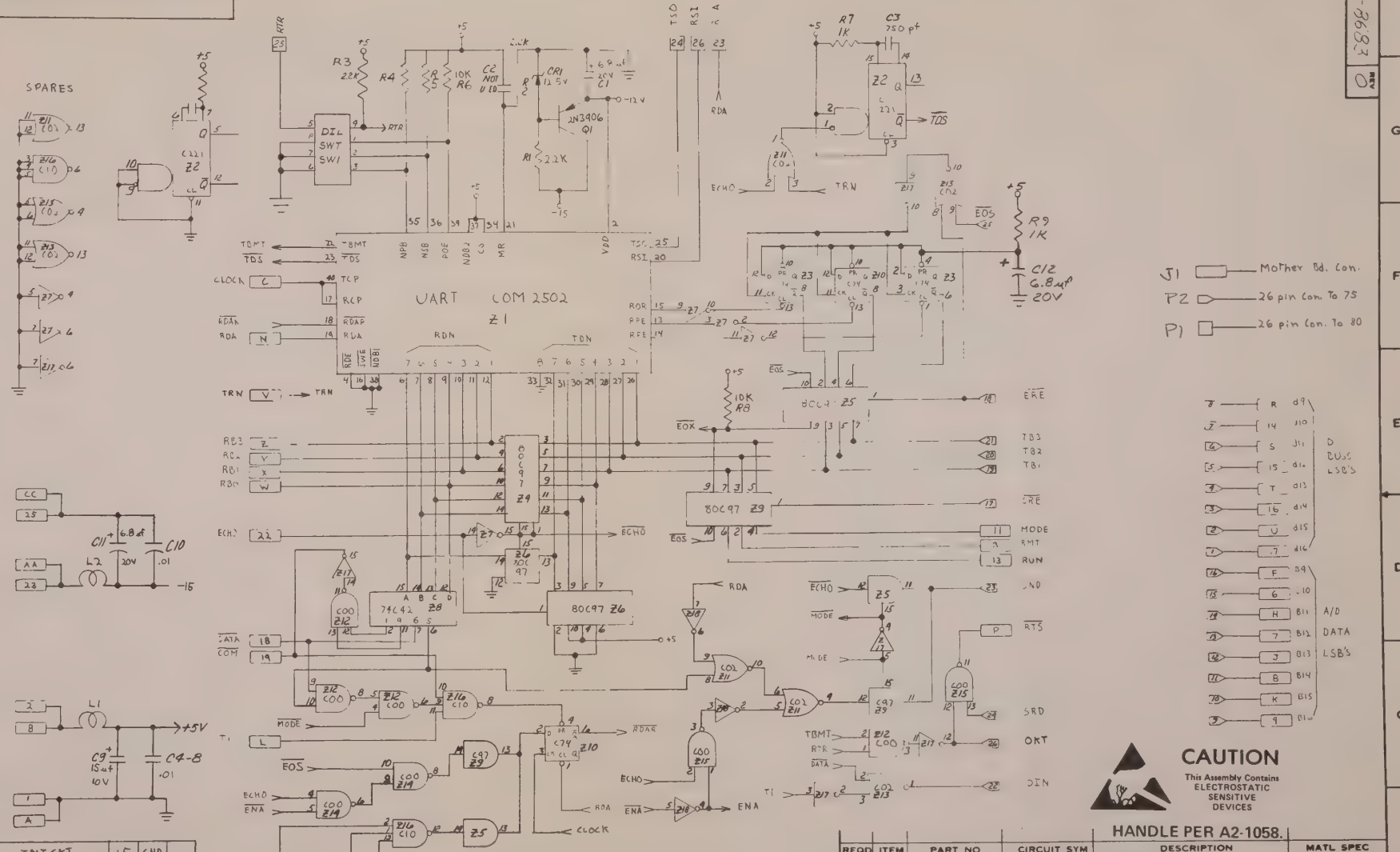
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C — 5-8683 — REV O



CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES

HANDLE PER A2-1058.

INT. CKT.		+5	GND
Z12,14,15	74C00	14	7
Z11,13	74C02	14	7
Z16	74C10	14	7
Z8	74C42	16	8
Z3,10	74C74	14	7
Z4,5,6,9	80C97	16	8
Z7,17,18	4049 16 P.in	1	8
Z1	2502 40 P.in	1	3
Z2	74C221	16	8

LIST OF MATERIAL

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

PL10-8683	AC475
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	L. MULLER	20-9-79
CHECKED	Gilbert Berry	4/8/80
DESIGNER	Lon Mullen	4/11/80
ENGINEER		
APPROVED		
RELEASED		
WEIGHT		

ANALOGIC — WAKEFIELD, MASS. 01880

ANDS 1771 ASYNCHRONOUS SERIAL LINE INTERFACE UART CARD AC-475 SCHEMATIC

CODE IDENT NO	SIZE		REV
31814	C	5-8683	O
SCALE —	ACCOUNT NO —	SHEET 1 OF 1	

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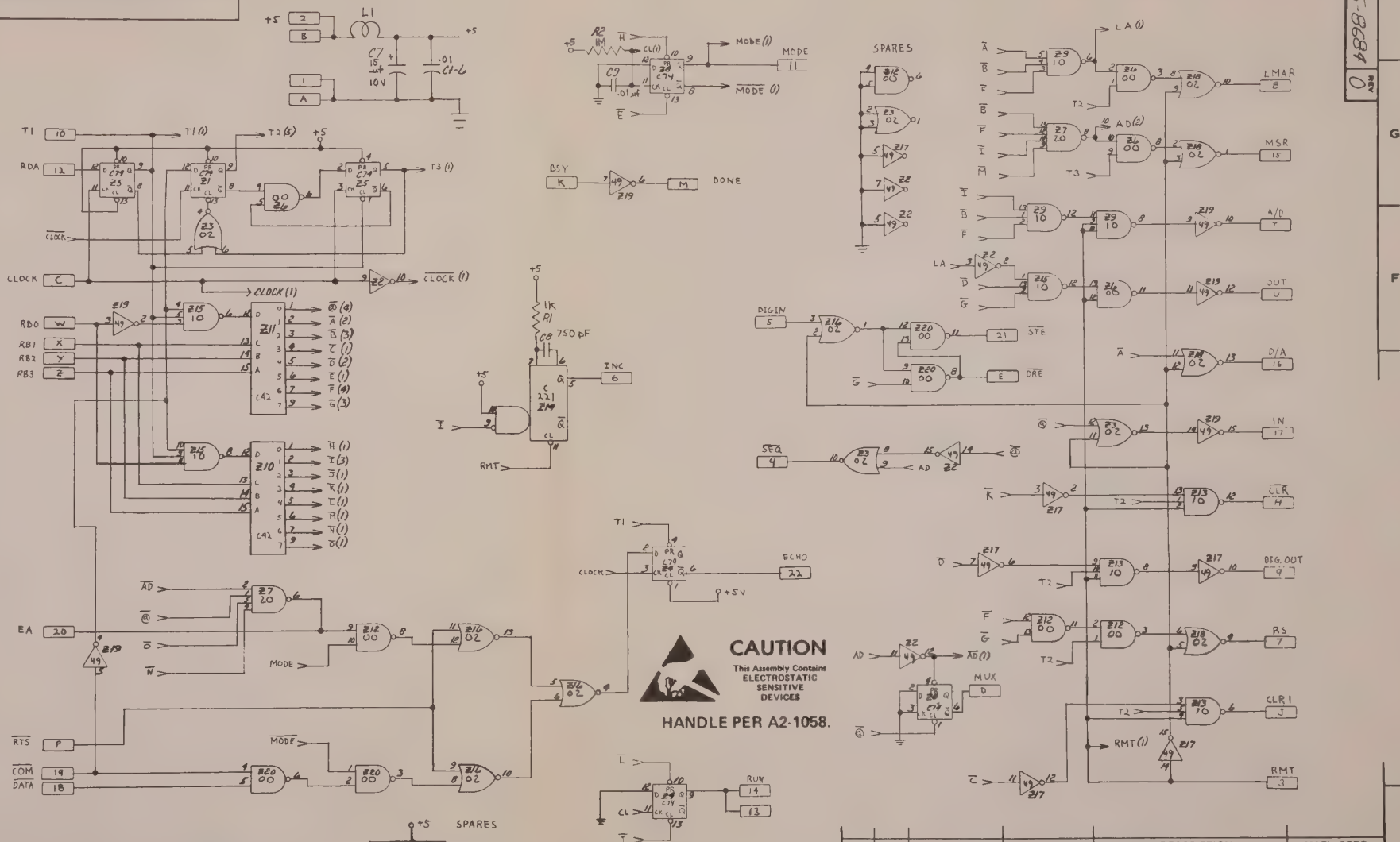
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C 5-8684 REV 0



INT. CKT.	+5	GND	REF. DES.
74C00	14	7	Z6,12,20
74C02	14	7	Z3,16,18
74C10	14	7	Z9,13,15
74C42	16	8	Z10,11
74C74	14	7	Z1,9,5,8
74C221	16	8	Z14
4049 16pin	1	8	Z2,17,19
74C20	14	7	Z7

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

P.I.O.-8684	AC476
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

		DATE
DRAWN	L. MULLER	7-8-77
CHECKED	Robert Perry	4/8/80
DESIGNER	L. Muller	4/11/80
ENGINEER		4-11-80
APPROVED		
RELEASED		
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

ANDS 5400 ASYNCHRONOUS SERIAL LINE INTERFACE CONTROL CARD AC-476 SCHEMATIC

CODE IDENT NO	SIZE		REV
31814	C	5-8684	0
SCALE	ACCOUNT NO	SHEET	
		1 OF 1	

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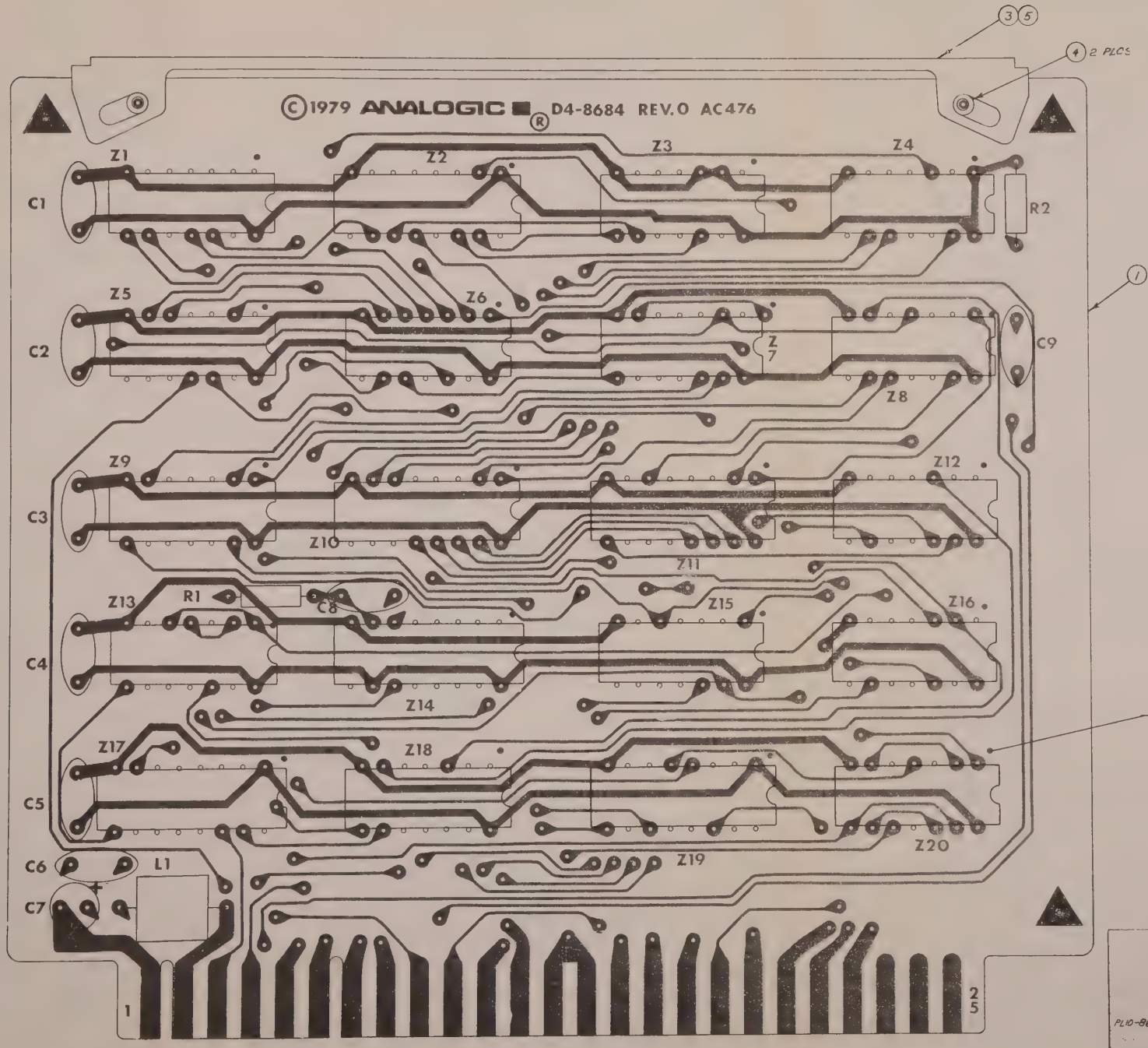

NOTES:
1. FOR SCHEMATIC SEE C5-8684
2. DOT INDICATES PIN 1 OF I.C.'S.
3. ASSEMBLE PER A2-1027.

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

COMPONENT SIDE

			ANALOGIC ■ WAKEFIELD MASS 01880	
			ASSEMBLY ANDS 5400 ASYNCHRONOUS SERIAL LINE INTERFACE CONTROL CARD AC-476	
PL10-8684 AC476 APPLICATION			31814 D 7-8684	REV 0
			4:1	SHEET 1 OF 1

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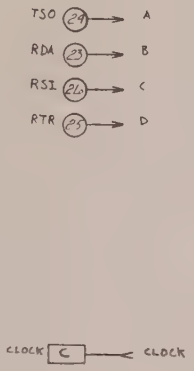
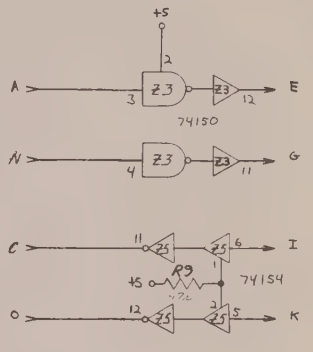
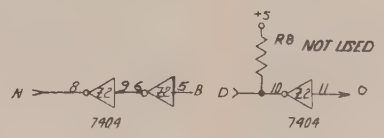
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

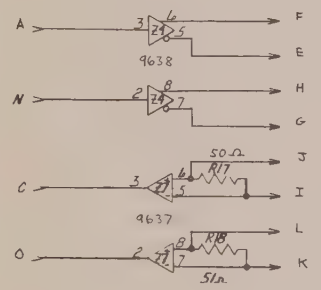
SIZE C | 5-8685 | REV 0



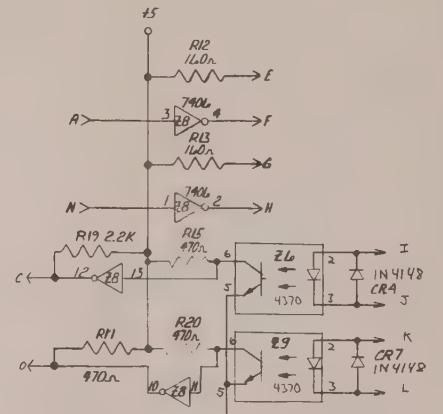


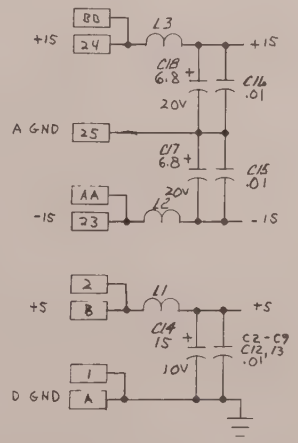
EIA RS-232 C

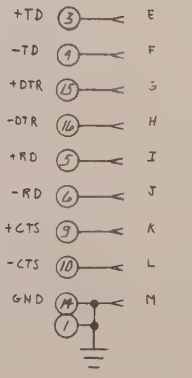


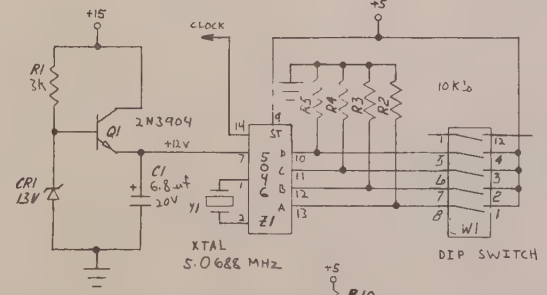


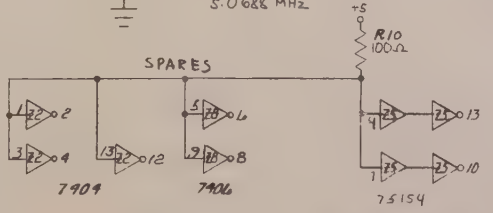
RS-422

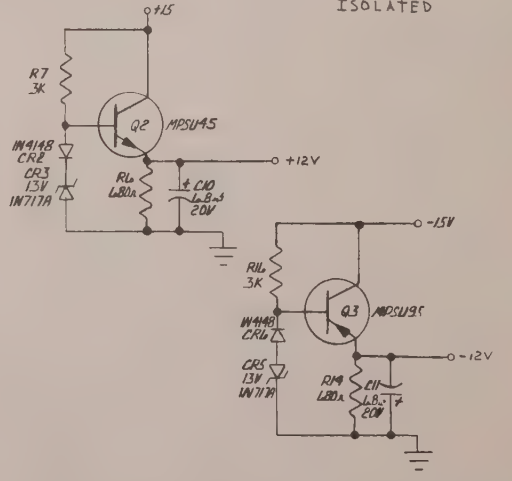












			+5	GND	#12	-12
Z6	7404		14	7		
Z7	9637	8 p.n	1	4		
Z9	9638	8 p.n	1	4		
Z5	75150	14 p.n	2	5	13	10
Z5	75154	16 p.n	15	8		
Z4,9	4370	8 p.n	8	5		
Z1	5046		3	5		
Z8	7406		14	7		

P1 ○ CABLE TO CHASSIS

J1 ▭ MOTHER BD CONNECTOR

PL10 8685	AC-477
NEXT ASSY	USED ON
APPLICATION	

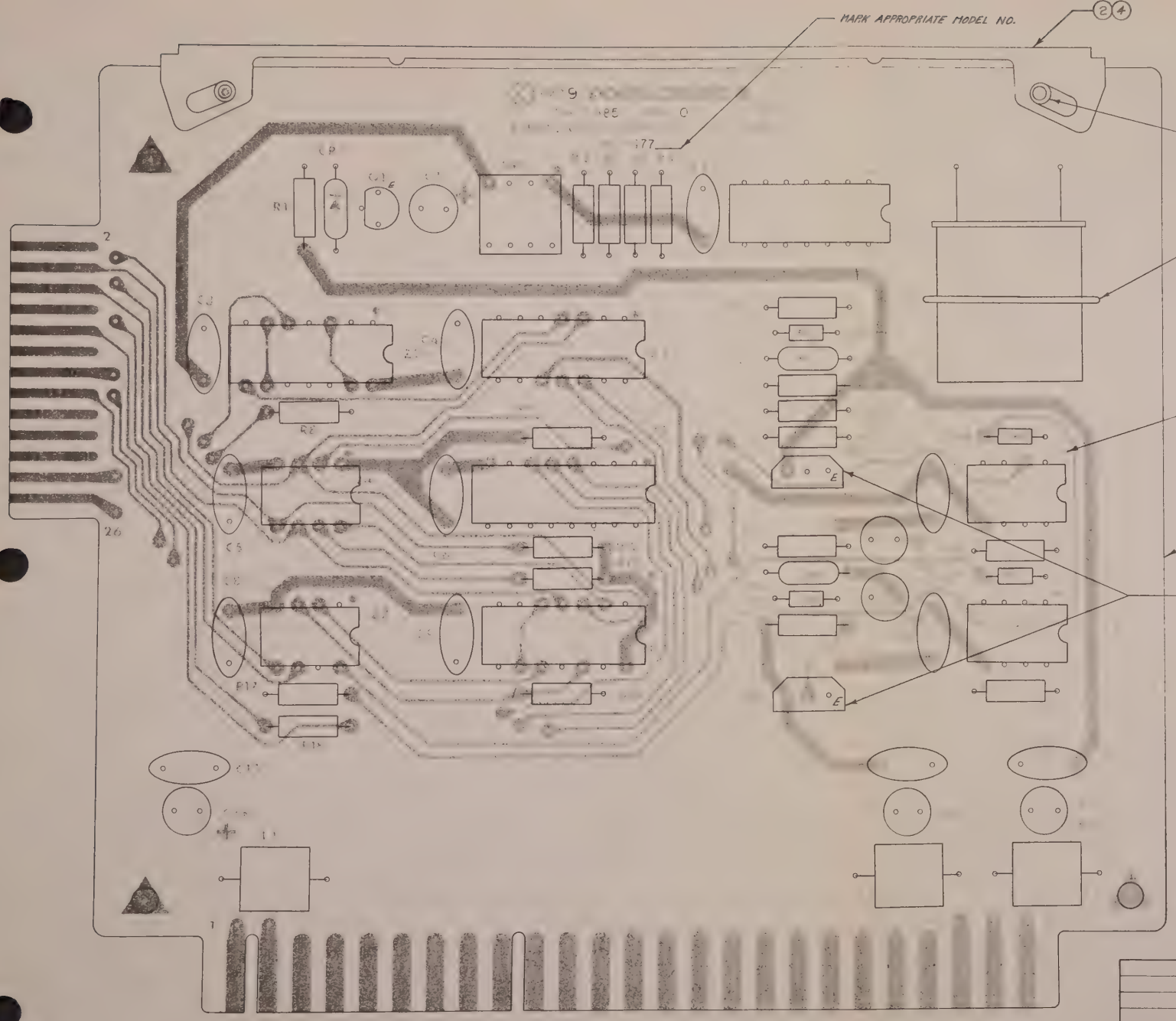
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± ANGLES XXX °
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	S Ryerse	10/3/79
CHECKED	Peter Berry	4/8/80
ENGINEER	J Mueller	4/11/80
ENGINEERING MGR.		4-11-80
QUALITY CONTROL		
PRODUCTION		
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

ANDS 5400 ASYNCHRONOUS SERIAL LINE INTERFACE R/T CARD AC-477
SCHEMATIC

CODE IDENT NO	SIZE		REV
31814	C	5-8685	0
SCALE ——		SHEET 1 OF 1	



REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE

SIZE D 7-8685 REV 0

NOTES:
1. FOR SCHEMATIC SEE C5-8685.
2. DOT INDICATES PIN 1 OF I.C.'S.
3. ASSEMBLE PER A2-1040.

COMPONENT SIDE

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS X: ± XX: ± XXX: ANGLES	DRAWN	DATE 2-9-77	ANALOGIC WAKEFIELD, MASS. 01880
			CHECKED		ASSEMBLY ANDS 5400 ASYNCHRONOUS SERIAL LINE INTERFACE R/T CARD AC 477
		MATERIAL	ENGINEER	4/10/80	
		FINISH	ENGINEERING MGR.	4-11-80	
			QUALITY CONTROL		
FWD-8686	AC 477	APPLICABLE SPECIFICATIONS	PRODUCTION		CODE IDENT NO 31814 | SIZE D | 7-8685 | REV 0
NEXT ASSY	USED ON		WEIGHT		SCALE 4:1 | SHEET 1 OF 1
APPLICATION					

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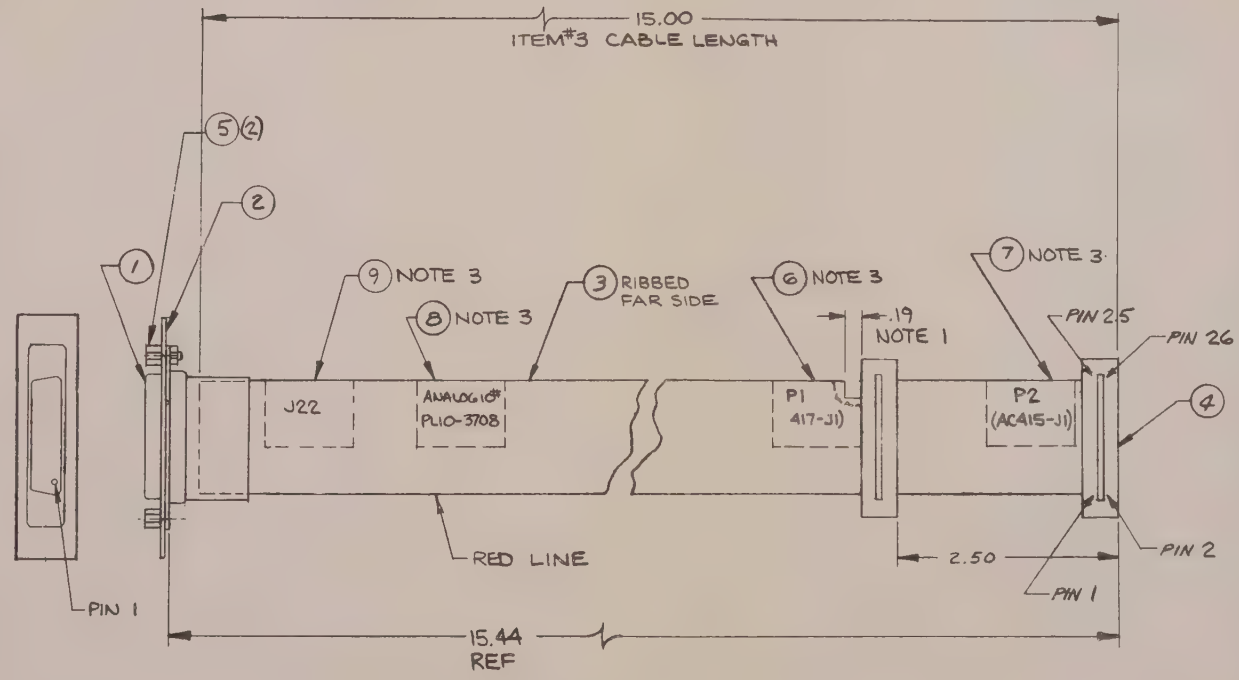
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C | 7-2308 | REV 0



WIRE NO.	FROM	TO	TO	FUNCTION
1	J22-1	P1-1	P2-1	GND
2	14	2	2	
3	2	3	3	+ TRANSMIT DATA
4	15	4	4	- TRANSMIT DATA
5	3	5	5	+ RECEIVE DATA
6	16	6	6	- RECEIVE DATA
7	4	7	7	
8	17	8	8	
9	5	9	9	+ CTS
10	18	10	10	- CTS
11	6	11	11	
12	19	12	12	
13	NC	13	13	
14	7	14	14	GND
15	20	15	15	+ DTR
16	8	16	16	- DTR
17	21	17	17	
18	9	18	18	
19	22	19	19	
20	10	20	20	
21	23	21	21	
22	J22-11	22	22	
23	NC	23	23	
24	NC	24	24	
25	NC	25	25	
26	NC	P1-26	P2-26	

NOTES:

1. CUT CONDUCTORS 23, 24, 25 & 26 TO DIM. SHOWN
2. ASSEMBLE ITEM 4 USING 3M PRESS AND LOCATOR PLATE 3M # 3443-11 WITH PLATEN 3M # 3442-7
3. LABEL MARKING TO APPEAR ON RIBBED SIDE OF CABLE. CUT CLEAR SIDE OF LABEL AND COVER MARKING.

PL10-3708	AN5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± .XX ± .03 .XXX ±
ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	N. CARTER	9-13-77
CHECKED	R. Irwin	10-17-77
ENGINEER	Len Muller	10-17-77
ENGINEERING MGR.	W. Irwin	10-17-77
QUALITY CONTROL	Lou Letta	10-20-77
PRODUCTION		
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSY CONN. INTERFACE (ASI)

CODE IDENT NO	SIZE		REV
31814	C	7-2308	0
SCALE 1/1		SHEET 1 OF 1	

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BASE ADDRESS 764000 w JUMPER E1 - E2
765000 w/o JUMPER

+ 0 CSR
2 TRR
4 FPR
6 SP
10 DMAR1
12 DMAR2
14 SP
16 SP
400 ↕ MASTER REGISTERS
776

POWER PINS							
REF DES	I.C. TYPE	+5	DIG GND	ANA GND	-15	+15
21, 38	74L242	16	8			
22, 42, 44, 45, 46	74LS11	14	7			
23, 18, 19, 34	74LS74	14	7			
24, 25, 47	74LS04	14	7			
27, 40	74LS10	14	7			
26, 9, 22, 28, 27	74LS00	14	7			
31, 21, 29, 39	74LS02	14	7			
20	74LS11	14	7			
11, 12, 29, 33, 36	7417	14	7			
13	7438	14	7			
15, 16	74LS20	14	7			
15, 20	74LS183	16	8			
17	74LS51	14	7			
226	74LS86	14	7			

POWER PINS							
REF DES	I.C. TYPE	+5	DIG GND	ANA GND	-15	+15
230	74LS174	16	8			
231	74LS08	14	7			
232	74LS05	14	7			
239	74LS27	14	7			
241, 42, 45, 52, 54, 67, 55	74LS157	16	8			
#49, 50, 51, 52	DS8837	16	8			
254, 56, 58, 60	DS8838	16	8			

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
2	4-681 4-703	SEE E.C.O.'S	RK	AP	1-14-80 4-25-80

SIZE D 5-8681 REV 2

MRADREN/ #37-3(E12SA2)
TQ3/ 29-10(E8SA2)
FPR/ #38-3(B12SA2)
FPMR/ #21-12(E6SA2) #17-1 (D5)
TS/ #1-C(E9SA2)
Ø DATA EN/ #31-3(A11SA2)

AD2 BUS DIS
AE2 DI4
AF2 DI3
AH2 DI2
AH1 DI1
AJ2 DI0
AK2 DO9
AL2 DO8
AM2 DO7
AV2 DO6
AP2 DO5
AN2 DO4
AT2 DO3
AU2 DO2
AR2 DO1
AS2 BUS DOO

8838 (×4)
258 (F2)
256 (E2)
255 (E2)
254 (D2)
253 (D2)
LS161 (×4)
298 (H2)
296 (F2)
299 (E2)
292 (D2)
LS157 (×4)
259 (H2)
257 (F2)
243 (E2)
241 (D2)
LS00 LS04 LS08 LS09 LS20 LS27 7417

FPR
RQ 5.6K
J1-19 NPRSTR/
TRR/ #38-2 (B13SA2)
C1/ 22S-8 (C13SA2)
TARWRT/ #16-5 (H11SA2)
J5-7 TRRTC
BOD 1 BOD 5 BOD 9 BOD 13
J2-9 J2-10 J2-11 J2-12 J2-13 J2-14 J2-15 J2-16 J3-9 J3-10 J3-11 J3-12 J3-13 J3-14 J3-15 J3-16
11DI15 11DI11 11DI07 11DI03
11DO15 11DO11 11DO07 11DO03
260 (H2)
230-11(F9)
28-1(F9SA2)
25-5(E9SA2)
219-2(A2)
230-19(E9)
230-6(E9)
218-12(D7)
230-9(E9)
230-13(E7)
230-3(E7)
A09 A06 A05 A03 A02 A01
250 (D15SA2)
251 (D15SA2)
R31 5.6K
R21 5.6K

SPARE GATES
232 74LS05
213 7438
217 74LS51
226 74LS86
236 7417

AA2 BA2 CA2 DA2 AC2 AT1 GC2 BT1 CC2 CT1 DC2 DT1
+5V
GND
C1, 16, 17, 33, 34, 40, 41, 52, 57, 60, 64, 67 — 15uF 10V
C3-10, 12-15, 18, 19, 21, 23, 24, 27-29, 32, 35, 36, 38, 42-51, 53-56, 58, 59, 61-63, 65, 66, 68 — .01uF

+5V RN1 (330/390Ω) 10 R26 5.6K R27 5.6K C66 100pF C69 200pF R32 330Ω R40 390Ω
BSSN J4-16
BRMT J4-14
BSSH PLS/
11DI10 #28-6-G(F15)
CSR04 J5-8
LDCSR #27-10(G11SA2)
260-13(E15)
256 (E15)
254 (E15)
11DI 12 11DI 05 11DI 04 11DI 03 11DI 02 11DI 01
Z19 LS74
Z30 LS174
Z18 LS74
CSR10 CSR12 CSR05 CSR06 CSR07
11DI06 256-G(E15)
11DI00 259-13(C15)
SYS INIT/ 239-G(E5SA2)
CLRGO/ J5-9 24-5(C9SA2)
CSR06 J1-5
CSR05 J1-10
R28 5.6K
LS11

CSR15/ J5-11
CSR14/ J5-12
CSR13/ J5-13
CSR12 #12-11 (E3SA2)
CSR1/ #38-1 (B13SA2)
J2-1 J2-2 J2-3 J2-4 J2-5 J2-6 J2-7 J2-8
BI0 5 BI0 7 BI0 9 BI0 13
11DO15 11DO11 11DO07 11DO03
260 (H15) 258 (F15) 256 (E15) 254 (D15)
257 255 253
(CSR11) BRMT M CSR10 CSR07 M CSR03 M
REQ INT/ J1-8
DONE/ #6-G(E11SA2)
CLRSC/ J5-10
IMEN/ 22-G(E9SA2)
FPMR #28-H(E14) C1/ 22S-8 (C13SA2)
226-12(F9SA2)
226-13(F9SA2)
216-9(F8SA2)

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PLN-8681	AC473		
NEXT ASSY	USED ON		
APPLICATION			

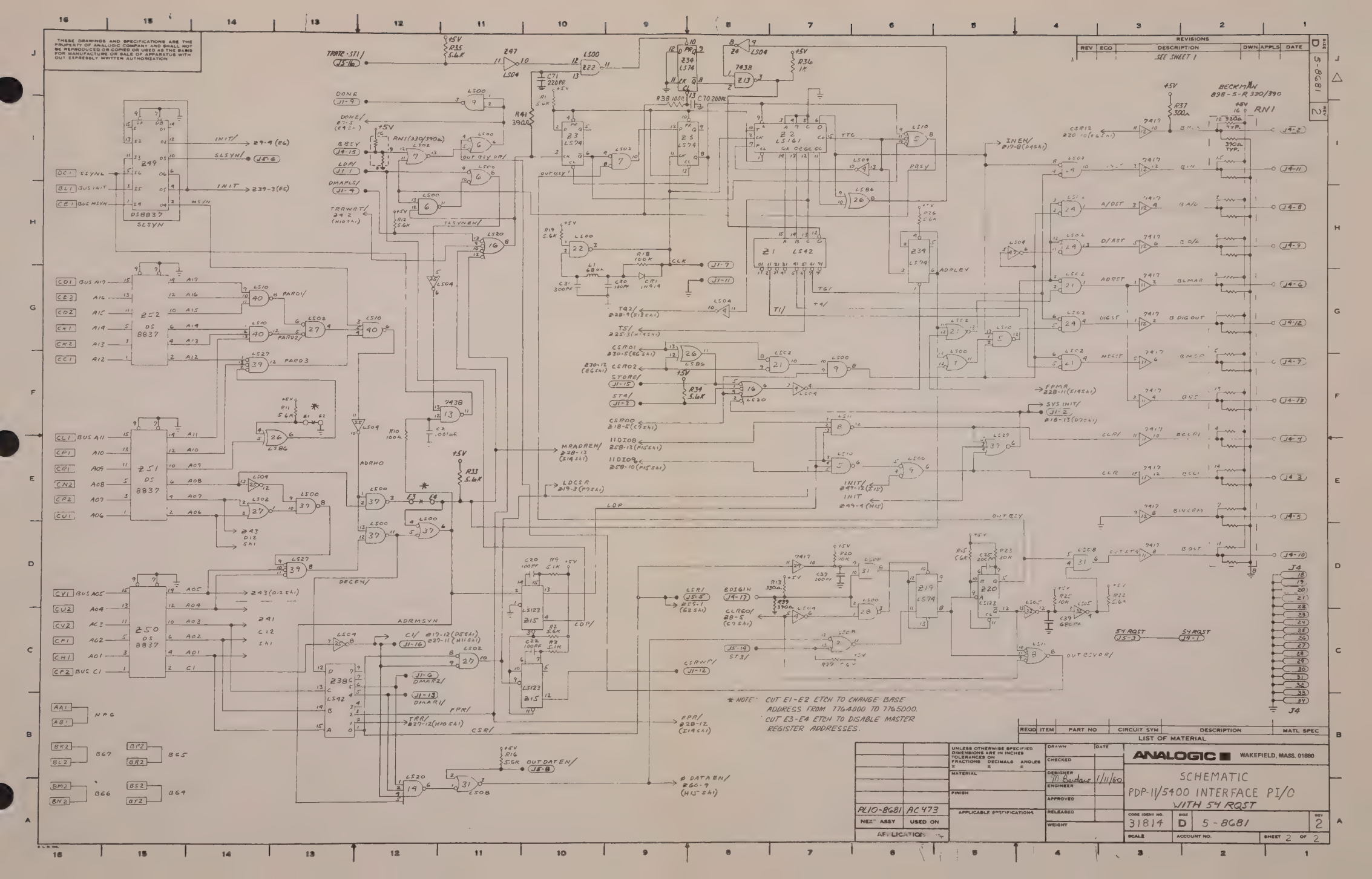
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	D.S.	1-1-80
CHECKED		1-11-80
DESIGNER	M. Bydalek	1/11/80
ENGINEER		1-11-80
APPROVED		6-17-80
RELEASED		6/18/80
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC
PDP-11/5400 INTERFACE PI/O
WITH 54 RQST

CODE IDENT NO.	SIZE	DWG NO.	REV
31814	D	5-8681	2
SCALE	ACCOUNT NO.	SHEET 1 OF 2	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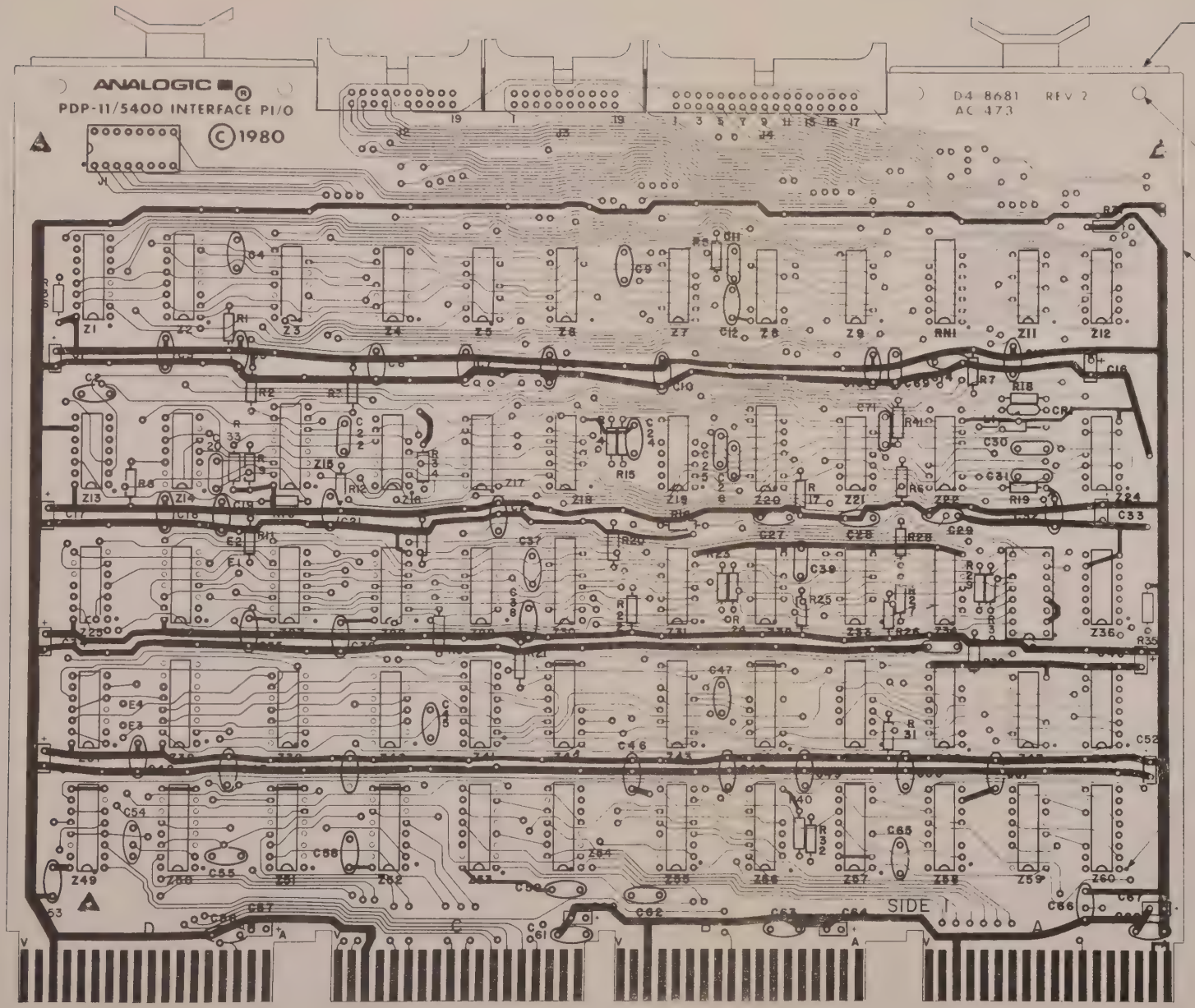
REVISIONS
REV ECO DESCRIPTION DWN APPL'S DATE
SEE SHEET 1
SIZE D 5-8681 REV 2
BECKMAN 898-5-R330/390
RN1
INIT/
SLSYN/
INIT
MSYN
SSYNL
BUS INIT
BUS MSYN
DS8837
SLSYN
Z49
Z52
Z51
Z50
BUS AI7
BUS AI1
BUS AC5
BUS C1
TRR12 -ST1/
DONE
DONE/
BBSY
LDP/
DMAPLS/
TRRWRT/
SLSYNEN/
OUT BSY ON/
OUTBSY'
INEN/
PBSY
ADPLEY
TG/
T4/
T1/
TQ2/
TS/
CSR01
CSR02
STORE/
ST4/
CSR00
11DIO8
11DIO9
MRADREN/
LDCSR
INIT
SYS INIT/
FPMR
ADRHO
ADRMSYN
DECEN/
OUTBSY
CSRI/
BDIGIN
CLRGO/
ST3/
CSRWT/
FPR/
CSR/
Ø DATAEN/
OUT DATEN/
54 RQST
OUTBSYOR/
* NOTE: CUT E1-E2 ETCH TO CHANGE BASE ADDRESS FROM 7764000 TO 7765000. CUT E3-E4 ETCH TO DISABLE MASTER REGISTER ADDRESSES.
J4
REQD ITEM PART NO CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN DATE
CHECKED
DESIGNER
ENGINEER
APPROVED
RELEASED
WEIGHT
PL10-8681 AC473
NEXT ASSY USED ON
APPLICATION
ANALOGIC WAKEFIELD, MASS. 01880
SCHEMATIC
PDP-11/5400 INTERFACE PI/O WITH 54 RQST
CODE IDENT NO. 31814
SIZE D
5-8681
REV 2
SCALE
ACCOUNT NO.
SHEET 2 OF 2

REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPLS	DATE	
2	4681 4703	SEE E.C.O.'S	RR	CF	LVH	5 2 80

SIZE D 7-8681 REV 2



(5) 2 REQ'D

(6) 4 REQ'D.

(1)

NOTES:
1. FOR SCHEMATIC SEE D5-8681
2. DOT INDICATES PIN 1 OF I.C.'S AND CONNECTORS.
3. ASSEMBLE PER A2-1027.
4. MAX. COMPONENT HEIGHT IS .375 AFTER WAVE SOLDER.

SEE NOTE 2

COMPONENT SIDE

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS X.= .XX= .XXX= ANGLES
		MATERIAL
		FINISH
PLI0-8681	AC 473	APPLICABLE SPECIFICATIONS
NEXT ASSY	USED ON	
APPLICATION		

DRAWN W.BASICK	DATE 1	ANALOGIC WAKEFIELD, MASS. 01880	
CHECKED R.ROSS	1-10-80	ASSEMBLY PDP-11/5400 INTERFACE PI/O WITH 54 ROST.	
ENGINEER M.BARLHAM	1-11-80		
ENGINEERING MGR K.A.HAANES	1-11-80		
QUALITY CONTROL			
PRODUCTION CONTROL	1/14/80	CODE IDENT NO 31814	SIZE D 7-9681 REV 2
WEIGHT		SCALE 2:1	SHEET OF

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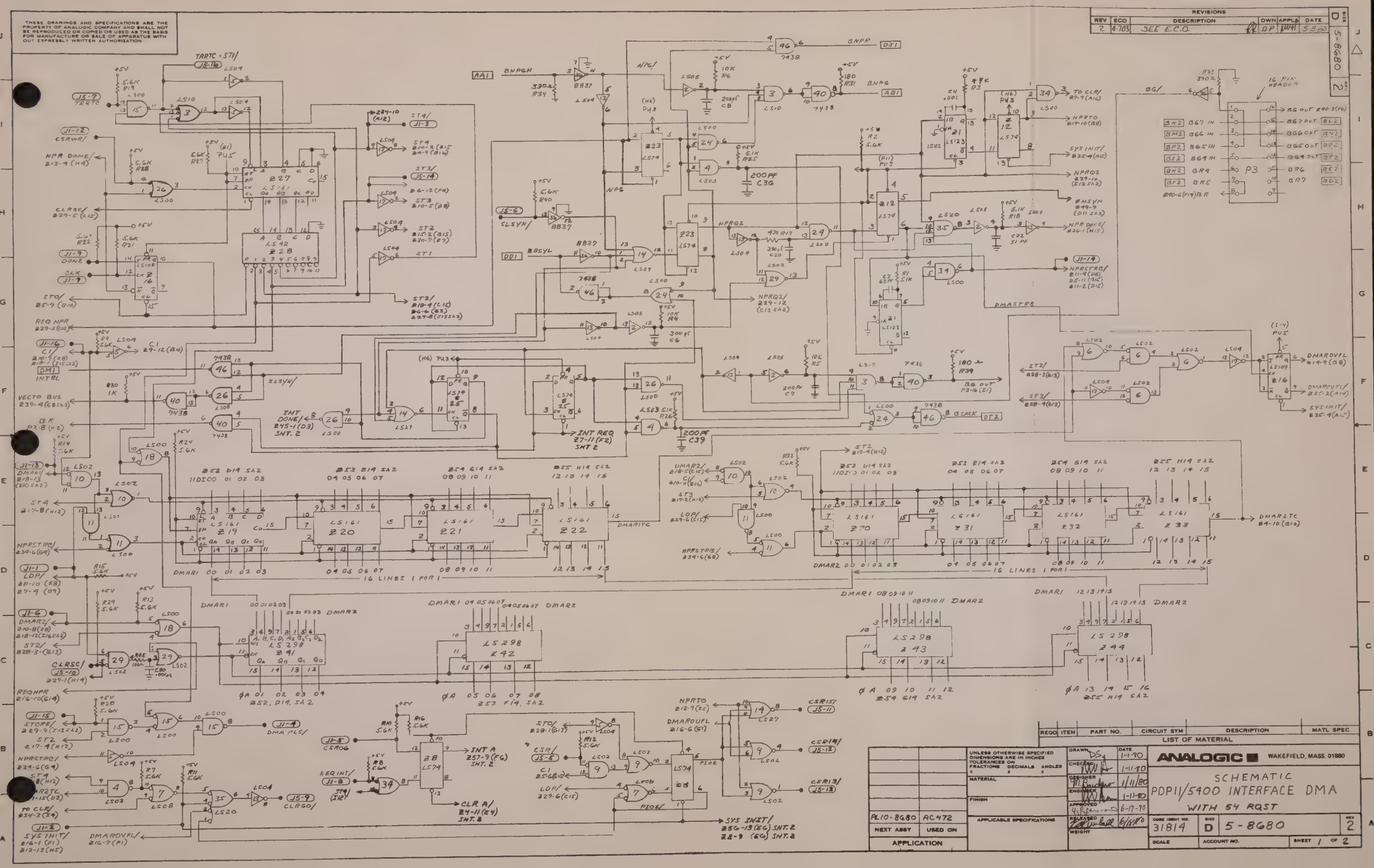
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPL'D	DATE
2	4-703	SEE E.C.O.	DP	[illegible]	5-8-80

SIZE D 5-8680 REV 2



LIST OF MATERIAL

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

PL10-8680	AC472		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
WEIGHT

DRAWN	DS	1-1-80
CHECKED	[illegible]	1-11-80
DESIGNER	M. Buckner	1/11/80
ENGINEER	[illegible]	1-11-80
APPROVED	[illegible]	6-17-80
RELEASED	[illegible]	6/18/80

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC
PDP11/5400 INTERFACE DMA
WITH 54 RQST

CODE IDENT NO.	SIZE		REV
31814	D	5-8680	2
SCALE	ACCOUNT NO.	SHEET 1 OF 2	

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
		SEE SHEET 1			

SIZE D 5-8680 REV 2

POWER PINS						
REF DES	I.C. TYPE	+5	DIG GND	ANA GND	-15	+15
Z1	74LS123	16	8			
Z2	74LS05	14	7			
Z3	74LS10	14	7			
Z4	74LS03	14	7			
Z5, 13, 17	74LS04	14	7			
Z6, 9, 10, 29	74LS02	14	7			
Z7	74LS08	14	7			
Z12, 28, 12, 23, 25	74LS74	14	7			
Z11, 15, 18, 24, 26, 30	74LS00	14	7			
Z14	74LS27	14	7			
Z16	74LS109	16	8			
Z19, 20, 21, 22, 27, 30, 31, 32, 33	74LS161	16	8			
Z28	74LS42	16	8			
Z35	74LS20	14	7			
Z36	DS8837	16	8			
Z37, 38, 39, 40, 46, 47, 48, 49, 50	7438	14	7			
Z41, 42, 43, 44	74LS298	16	8			
Z52, 53, 54, 55	DS8838	16	8			
Z45	74LS821	16	8			
Z57	74LS32	14	7			

SPARE GATES

Z22 — 74LS05

Z5 — 74LS04

Z57 — 74LS32

Z45 — 74LS821

Z36 — DS8837

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

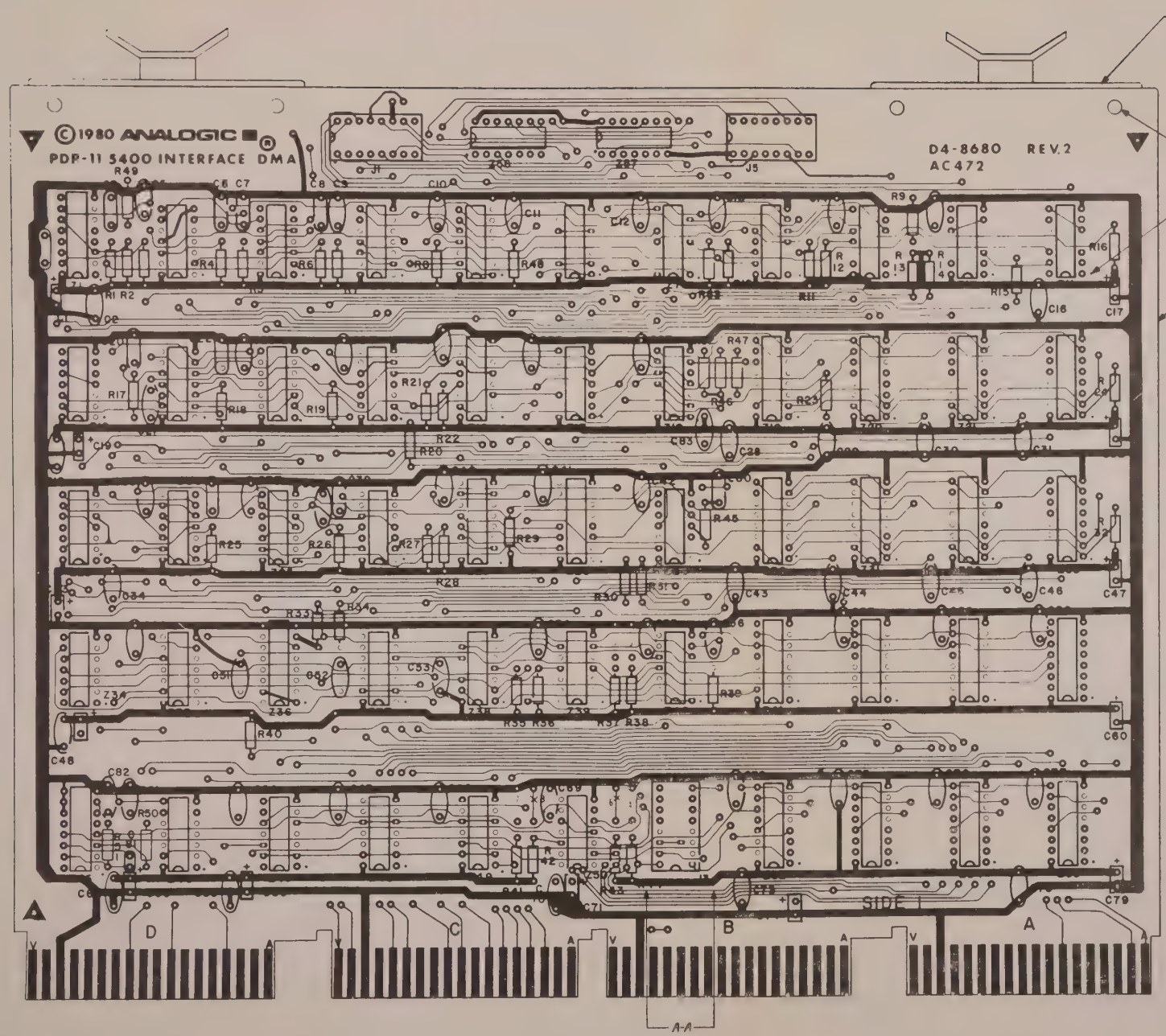
LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±	DRAWN	DATE	ANALOGIC WAKEFIELD, MASS. 01880
MATERIAL	CHECKED		SCHEMATIC PDP-11/5400 INTERFACE DMA WITH 54 RQST
FINISH	DESIGNER / ENGINEER	M. Bardour 11/11/80	
APPLICABLE SPECIFICATIONS	APPROVED		
	RELEASED		
	WEIGHT		

PL10-8680 AC 472	CODE IDENT NO. 31814	SIZE D	5-8680	REV 2
NEXT ASSY / USED ON	SCALE	ACCOUNT NO.	SHEET 2 OF 2	
APPLICATION				

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
2	4703	SEE EC.O	DP		5-8-80

D 7-8680 2



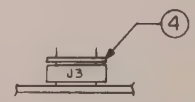
5 2 REQ'D

6 4 REQ'D

SEE NOTE 2

1

NOTES:
1. FOR SCHEMATIC SEE D5-8680.
2. DOT INDICATES PIN 1 OF I.C.S AND CONNECTORS.
3. ASSEMBLE PER A2-1027.
4. MAX. COMPONENT HEIGHT .375" AFTER WAVE SOLDERING.



VIEW A-A

COMPONENT SIDE

PL10-8680	AC472
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± .1 XX ± .03 XXX ±
ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN W. BROOKS	DATE 1-8-80	ANALOGIC WAKEFIELD MASS 01880
CHECKED R. ROSS	1-9-80	ASSEMBLY PDP-11/5400 INTERFACE DMA WITH 54 RAST.
ENGINEER M. BARDARO	1-11-80	
ENGINEERING MGR R. W. HAVENER	1-11-80	
QUALITY CONTROL	6-17-80	
PRODUCTION	6/18/80	
WEIGHT		CODE IDENT NO 31814 · SIZE D · 7-8680 · REV 2
		SCALE 2:1 · SHEET 1 OF 1

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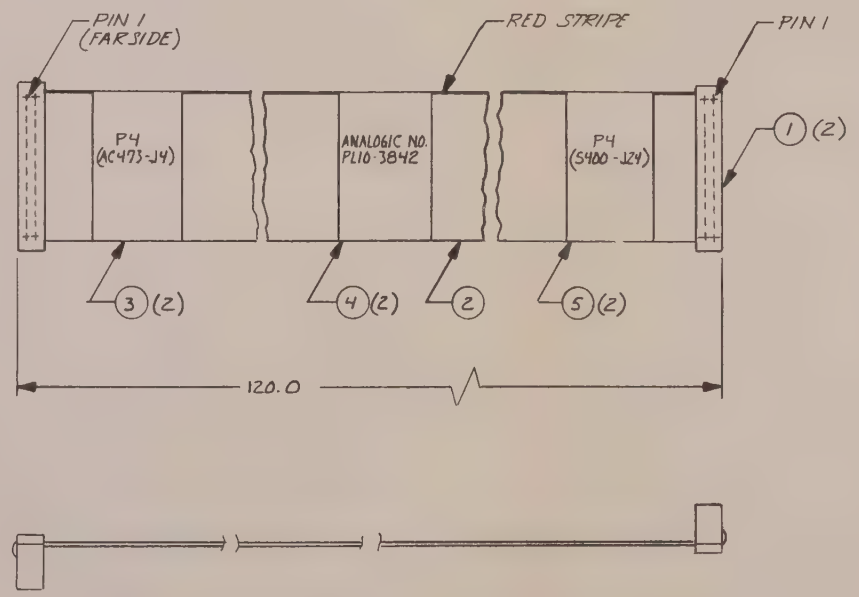
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C | 7-2395 | REV 0



ITEM NO.	WIRE NO.	FROM	TO	SIGNAL
2	1	P4 -1	P4 -1	
	2	-2	-2	
	3	-3	-3	
	4	-4	-4	
	5	-5	-5	
	6	-6	-6	
	7	-7	-7	
	8	-8	-8	
	9	-9	-9	
	10	-10	-10	
	11	-11	-11	
	12	-12	-12	
	13	-13	-13	
	14	-14	-14	
	15	-15	-15	
	16	-16	-16	
	17	-17	-17	
	18	-18	-18	
	19	-19	-19	
	20	-20	-20	
	21	-21	-21	
	22	-22	-22	
	23	-23	-23	
	24	-24	-24	
	25	-25	-25	
	26	-26	-26	
	27	-27	-27	
	28	-28	-28	
	29	-29	-29	
	30	-30	-30	
	31	-31	-31	
	32	-32	-32	
	33	-33	-33	
2	34	P4-34	P4-34	

PL10-3842	AN05400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ±1.0 .XX ± ANGLES .XXX ±
MATERIAL —
FINISH —
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	[illegible]	Jan 9, '80
CHECKED	R. Rose	1/11/80
ENGINEER	M. Bathum	1/11/80
ENGINEERING MGR.	[illegible]	1-11-80
QUALITY CONTROL	H. J. Garova	6-17-80
PRODUCTION	[illegible]	6/18/80
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASS'Y. P4
(PDP11 INTERFACE EXTERNAL 34 COND.)

CODE IDENT NO	SIZE		REV
31814	C	7-2395	0
SCALE 1/1		SHEET 1 OF 1	

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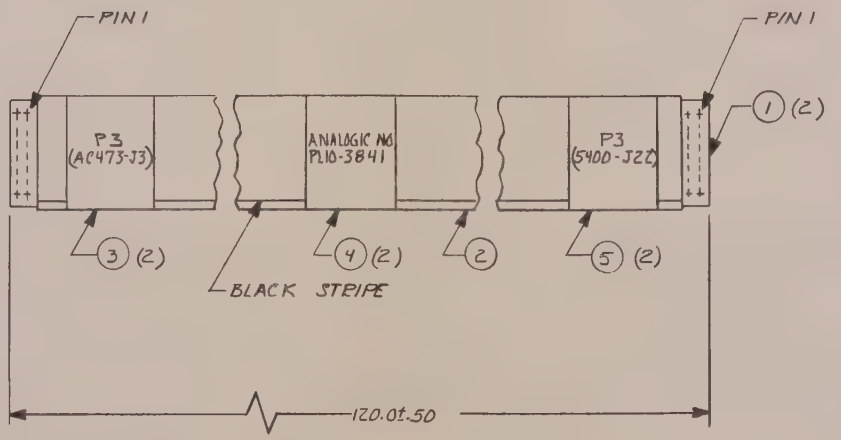
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C | 7-2394 | REV 0

ITEM NO.	WIRE NO.	FROM	TO	SIGNAL
2	1	P3-1	P3-1	
	2	-2	-2	
	3	-3	-3	
	4	-4	-4	
	5	-5	-5	
	6	-6	-6	
	7	-7	-7	
	8	-8	-8	
	9	-9	-9	
	10	-10	-10	
	11	-11	-11	
	12	-12	-12	
	13	-13	-13	
	14	-14	-14	
	15	-15	-15	
	16	-16	-16	
	17	-17	-17	
	18	-18	-18	
	19	-19	-19	
2	20	P3-20	P3-20	SHIELD



SHIELD TO BE WITHIN .06 FROM EDGE OF CONN. AND NOT EXPOSED 2 PLACES

PL10-3841	AND85400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± .OI .XXX ±
ANGLES ±
MATERIAL —"—
FINISH —"—
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	Bob Berg	Jan 11, '80
CHECKED	R. Rood	1/11/80
ENGINEER	M. Rayburn	1/11/80
ENGINEERING MGR.		1-11-80
QUALITY CONTROL	H. G. Farrow	6-17-80
PRODUCTION	R. Rumbell	6/18/80
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASS'Y. P3
(PDP-11 INTERFACE EXTERNAL 20 COND)

CODE IDENT NO	SIZE		REV
31814	C	7-2394	0
SCALE 1/1		SHEET 1 OF 1	

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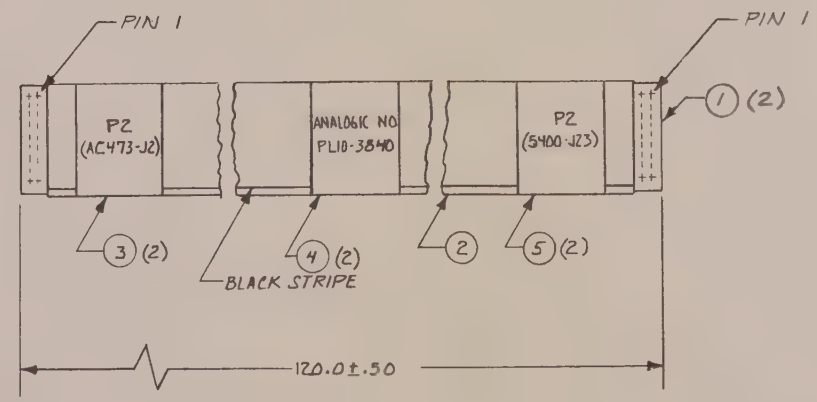
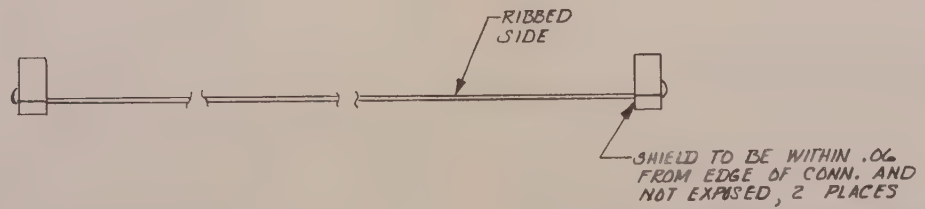
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE C | 7-2393 | REV 0

ITEM NO.	WIRE NO.	FROM	TO	SIGNAL
2	1	P2 - 1	P2 - 1	
	2	-2	-2	
	3	-3	-3	
	4	-4	-4	
	5	-5	-5	
	6	-6	-6	
	7	-7	-7	
	8	-8	-8	
	9	-9	-9	
	10	-10	-10	
	11	-11	-11	
	12	-12	-12	
	13	-13	-13	
	14	-14	-14	
	15	-15	-15	
	16	-16	-16	
	17	-17	-17	
	18	-18	-18	
	19	-19	-19	
2	20	P2 -20	P2 -20	SHIELD





PL10-3840	AND5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± .XX ± .01 .XXX ±
ANGLES ±
MATERIAL —//—
FINISH —//—
APPLICABLE SPECIFICATIONS

		DATE
DRAWN		Jan. 11, 80
CHECKED	R. Rossi	1/11/80
ENGINEER	M. Bardwell	1/11/80
ENGINEERING MGR	R.N. Dow	1-14-80
QUALITY CONTROL	H.F. Lawrence	6-17-80
PRODUCTION		6/17/80
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASS'Y. P2
(PDP11 INTERFACE EXTERNAL 20 COND.)

CODE IDENT NO	SIZE		REV
31814	C	7-2393	0
SCALE 1/1		SHEET 1 OF 1	

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IEEE488

INTERFACE BUS FOR AN5400

INTRODUCTION

The **IEEE Digital Bus Interface for the AN5400** provides the data acquisition system with intermediate speed data communications with a wide variety of devices using the IEEE 488-1975 standard bus. This enables the AN5400 to fit easily into existing instrumentation systems, and makes possible large data systems using several AN5400 masters.

Information is transmitted along the bus over 16 signal lines. Seven (7) lines are used for passing device addresses, command messages, and input-output data. Three (3) lines are used in the transfer of data in an interlocking handshake process. The remaining lines carry special interface control signals. The AN5400 Bus Interface does not provide all of the functions available within the IEEE specifications. Table 1 lists functions and signals that are used. For a complete description of the IEEE bus organization, refer to Standard 488-1975.

FUNCTIONAL DESCRIPTION

The AN5400 may be addressed as either a **talker** or a **listener.** As a **listener,** data may be received, and commands may be executed. After being addressed as a **talker,** data is automatically sent along the bus in four bytes. An **EOI** signal is sent with the last byte to indicate to the controller that the data sequence is over.

Addressing can only take place when the Attention **(ATN)** line is true. In this condition, commands are not executed and the input shift latch is unaffected. Table 2 shows all possible addresses to which the interface may be set using the PC switch. Note that only pairs of addresses may be selected. Each listen address in columns one or two corresponds to a talk address in columns three or four. Two special characters are used to unaddress the interface. **(?)** is the unlisten character and **(—)** is the untalk character.

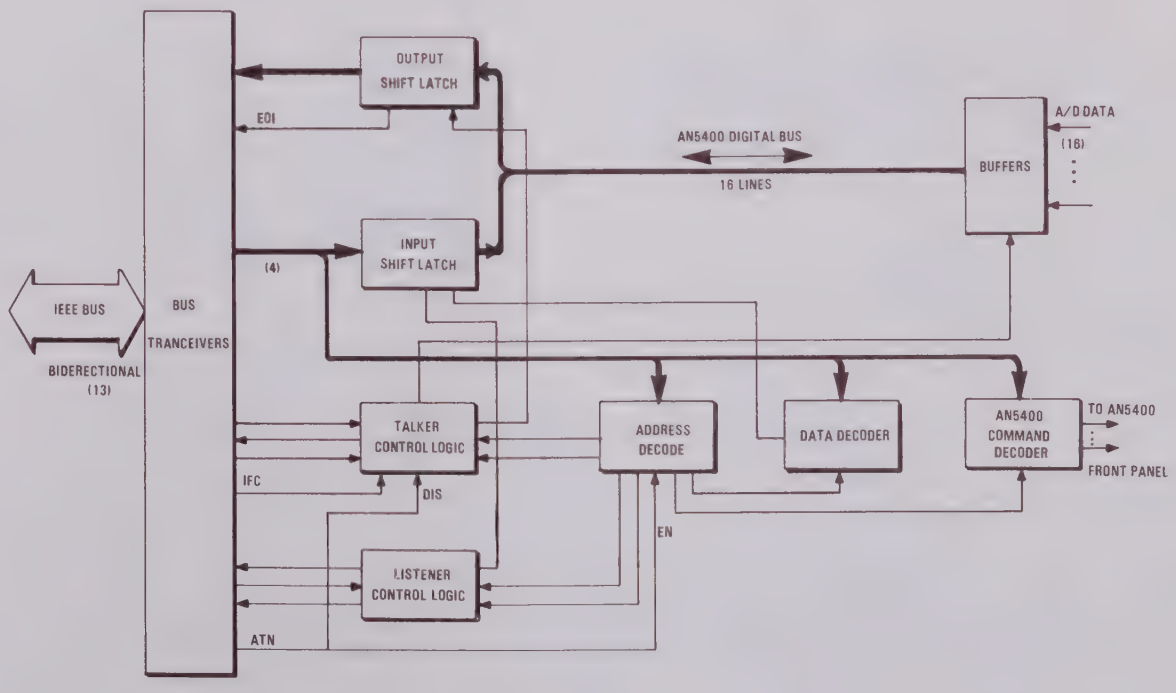

Figure 1. IEEE 488 — AN5400 Interface Block Diagram

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After addressing, the **ATN** line is set false to allow data and commands to be recognized. Command characters as listed in Table 3 cause the AN5400 to perform the indicated function. If a data character is detected, the four LSB's of the data byte will be loaded into the input shift latch, which is a 4 X 4 parallel shift register. The four outputs of each stage are tristated onto the 16-bit internal bus of the AN5400.

When addressed as a talker, data is loaded from the AN5400 bus in parallel to the output shift latch. The output shift latch is also a 4 X 4 parallel shift register which outputs 4-bit data blocks to the bottom 4 bits of the IEEE data bus. The top 3 bits are permanently wired to levels to represent the ASCII characters in Table 4.

Data is received and transmitted MSB byte first.

The interface clear (IFC) signal resets the talker control logic and listener control logic to the normal unaddressed condition. At **power turn on,** the interface automatically clears itself to the unaddressed condition.

PHYSICAL DESCRIPTION

The AN5400 Bus Interface is constructed on three internal AN5400 modules. They are an **MSB Data Latch** (AC407) located in slot 75, an **LSB Data Latch** (AC408) located in slot 76, and a **Control Module** (AC409) located in slot 77. Connection to the Bus is made via a 26 pin PC edge connector and ribbon cable from the Control module to a connector on the chassis back plate. The switch determining the Interface bus address is located on the Control module as shown in Figure 2.

Table 1
IEEE 488 SIGNAL LINES & FUNCTIONS

SIGNAL	PIN NO.	DESCRIPTION
DIO 1	1	DATA LSB
DIO 2	2	DATA
DIO 3	3	DATA
DIO 4	4	DATA
DIO 5	13	DATA
DIO 6	14	DATA
DIO 7	15	DATA MSB
DIO 8	16	NOT USED
EOI	5	END OF DATA BLOCK
IFC	9	INTERFACE CLEAR
ATN	11	ATTENTION
SRQ	10	NOT USED
REN	17	NOT USED
DAV	6	DATA AVAILABLE
NRFD	7	NOT READY FOR DATA
NDAC	8	DATA NOT ACCEPTED

FUNCTIONS PROVIDED

SOURCE HANDSHAKE
ACCEPTOR HANDSHAKE
TALKER
LISTENER
DEVICE CLEAR

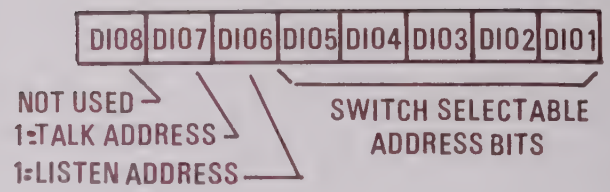


Table 2
AVAILABLE ADDRESS CODES AND EQUIVALENT ASC II

DIO4	DIO3	DIO2	DIO1	DIO7 0 DIO6 1 DIO5 0	0 1 1	1 0 0	1 0 1
0	0	0	0	SP	Ø	@	P
0	0	0	1	!	1	A	Q
0	0	1	0	"	2	B	R
0	0	1	1	#	3	C	S
0	1	0	0	$	4	D	T
0	1	0	1	%	5	E	U
0	1	1	0	&	6	F	V
0	1	1	1	'	7	G	W
1	0	0	0	(	8	H	X
1	0	0	1	)	9	I	Y
1	0	1	0	*	:	J	Z
1	0	1	1	+	;	K	[
1	1	0	0	,	<	L	\
1	1	0	1	-	=	M	]
1	1	1	0	.	>	N	^
1	1	1	1	/	NOTE	O	NOTE

NOTE: 0 1 1 1 1 1 1 is the Unlisten Character ?
NOTE: 1 0 1 1 1 1 1 is the Untalk Character _

Table 3
COMMAND CHARACTER DEFINITIONS

CHARACTER	DEFINITION
P or @	Reads digital input data from previously addressed source, i.e. user card or digiswitch
A	Changes AN5400 address decoding to A/D mode.
R or B	Starts a measurement sequence (Triggers A/D Converter)
S or C	Increments the AN5400 address register
T or D	Loads previously addressed D/A or digital output card with the 16 bit contents of the input shift latch
U or E	Loads the 4 MSB bits of the input shift latch into the AN5400 range register
V or F	Loads the 12 LSB bits of the input shift latch into the AN5400 address register
W or G	Clears AN5400 address and range registers, sets A/D address decoding
Q	Changes AN5400 address decoding to D/A mode

Table 4
DATA CHARACTERS TRANSLATION

DATA ELEMENTS							ASC II	HEX
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1		
0	1	1	0	0	0	0	Ø	0
0	1	1	0	0	0	1	1	1
0	1	1	0	0	1	0	2	2
0	1	1	0	0	1	1	3	3
0	1	1	0	1	0	0	4	4
0	1	1	0	1	0	1	5	5
0	1	1	0	1	1	0	6	6
0	1	1	0	1	1	1	7	7
0	1	1	1	0	0	0	8	8
0	1	1	1	0	0	1	9	9
0	1	1	1	0	1	0	:	A
0	1	1	1	0	1	1	;	B
0	1	1	1	1	0	0	<	C
0	1	1	1	1	0	1	=	D
0	1	1	1	1	1	0	>	E
0	1	1	1	1	1	1	?	F

Figure 2 also shows the chassis connector pinout with numbers as listed in Table 1.

The AN5400 Bus Interface is supplied with a 4-meter stackable molded cable.

HANDSHAKE OPERATION

All data transfers on lines DI01 thru DI07 are accomplished using a handshake process. Data available **(DAV)** is produced by the current talker when data is on the bus. Not ready for data **(NRFD)** and Data accepted **(DAC)** are produced by all current listeners. Note that the bus itself performs an **AND** function, making the transfer process dependent on the response of all current listeners. The bus performs an **OR** function on the **DAV** line enabling any device alone to assert this signal.

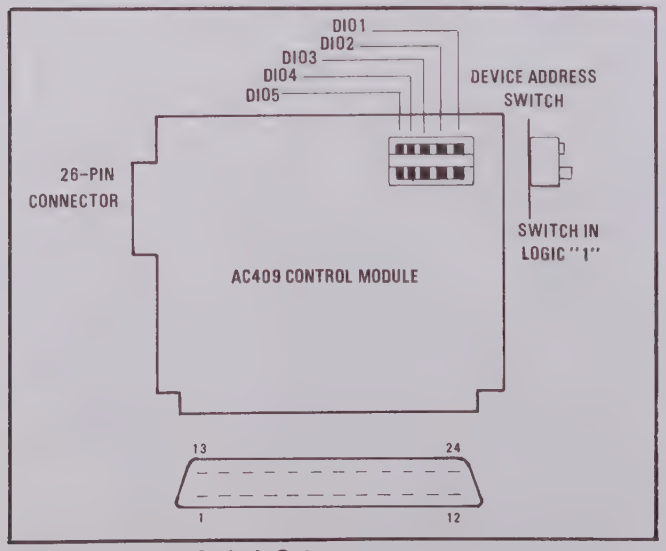


Figure 2. AC409 Switch Setups

Figure 3 shows this handshake timing sequence for the interface when it is the only listener on the bus.

Note that the speed of the data transfers is determined by the slowest device on the bus.

Figure 4 shows the timing sequence for the interface when it is a talker and includes the **EOI** signal timing.

MESSAGE SEQUENCE

The following is a summary of typical message transfers to the AN5400. Symbols used are:
MLA: AN5400 receives its listen address
MTA: AN5400 receives its talk address
UNT: AN5400 is unaddressed from talk mode
UNL: AN5400 is unaddressed from listen mode
RG: ASC II range character (Table 4)
AD1-AD3: ASCII address character (Table 4)
AD1 is the MSB byte, AD3 is the LSB byte
DT1-DT4: ASCII data character (Table 4)

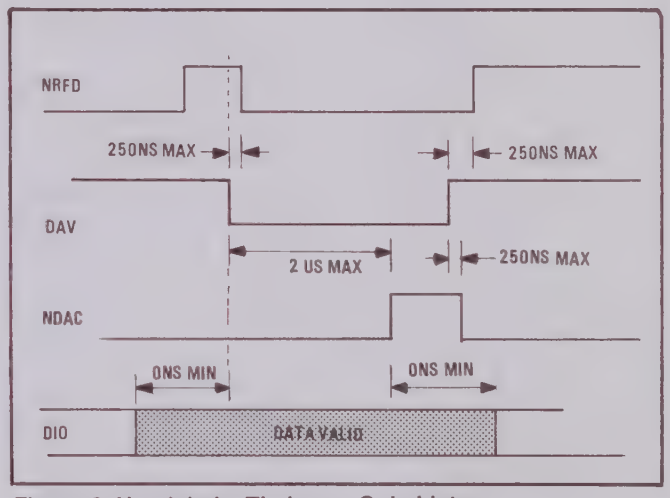


Figure 3. Handshake Timing — Only Listener

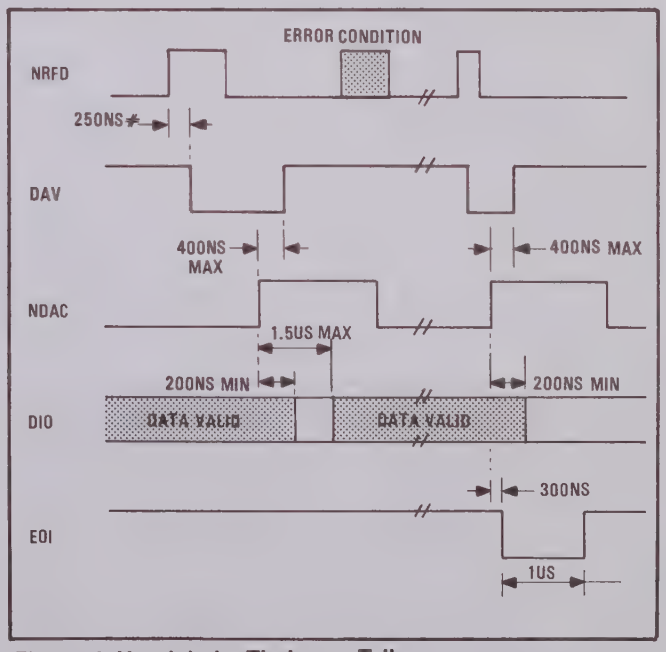
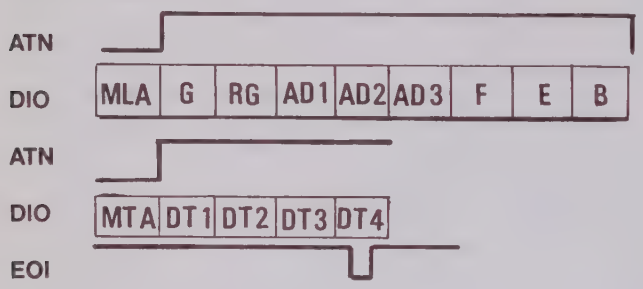


Figure 4. Handshake Timing — Talker

PROBLEM 1

It is desired to measure channel 30_8 on the first 4720 multiplexer in the master chassis. It will be measured in a single ended mode with a gain of two (2).

Byte Sequence will be:



NOTES: It is good practice to clear **(G)** the AN5400 front panel at the start of a program.

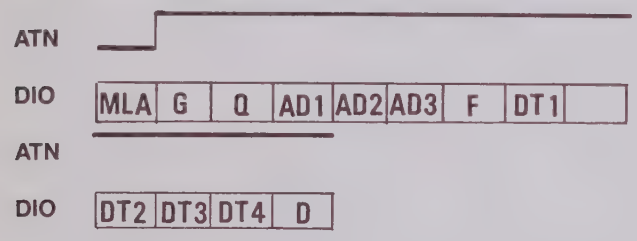
RG = 1 (ASC II)
AD1 = Ø (ASC II)
AD2 = 1 (ASC II)
AD3 = 8 (ASC II)

DT1 thru DT4 will be A/D data, left justified.

PROBLEM 2

It is desired to send data to channel 3_8 of an AC-1562 D/A in the first slot of the first slave box.

Byte Sequence will be:

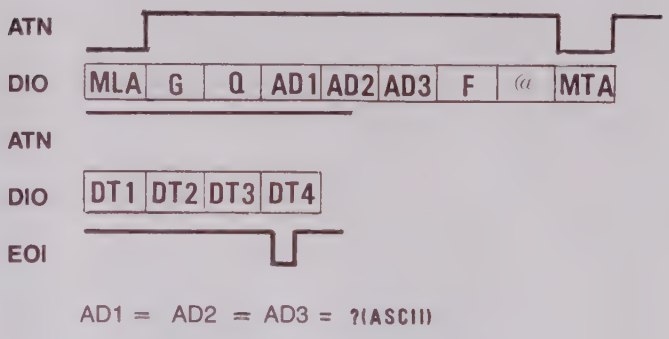


NOTE: DT4 is a **Don't Care** data character. Since the AC-1562 is only 12 bits, and data is left justified. DT4 must be sent to fill out the data field.

AD1 = 1 (ASC II)
AD2 = Ø (ASC II)
AD3 = 3 (ASC II)

PROBLEM 3

It is desired to read the number set on the front panel digiswitch.



AD1 = AD2 = AD3 = ?(ASCII)

BUS ELECTRICAL SPECIFICATIONS

Bus transceivers are used on data lines DIO1 thru DIO8, **DAV, NDAC, NRFD,** and **EOI.** They use open collector outputs with termination resistors, and line receivers with input hyteresis. All other bus lines are unterminated.

When interconnecting devices, the user should follow the rules set forth in the IEEE standard 488-1975 pertaining to cable length and number of devices on the bus. In general, no more than 15 devices may be used with 2 meters of cable per device, or a maximum of 20 meters of cable in total.

NOTE: All bus signals are low true.

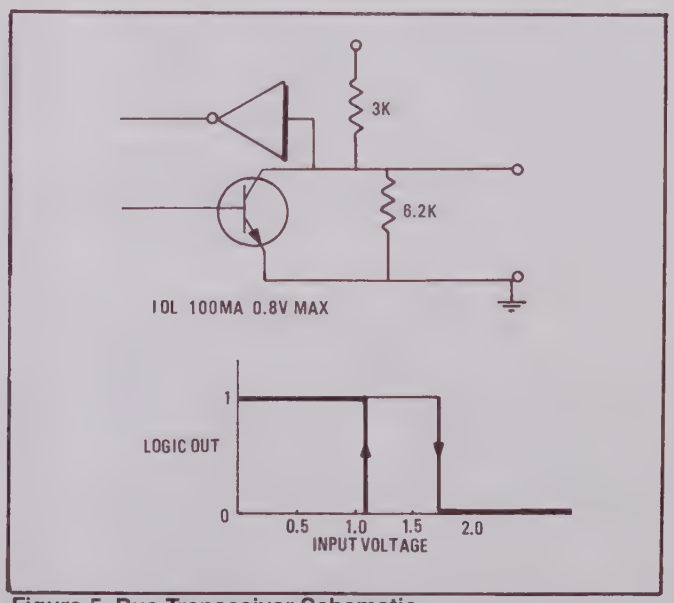


Figure 5. Bus Transceiver Schematic

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Audubon Road ■ Wakefield, Massachusetts 01880
Tel. (617) 246-0300 ■ TWX (710) 348-0425 ■ Telex 94-9307
ANALOGIC LIMITED
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Tel. Wey 41251 ■ Telex (851) 928030
ANALOGIC REGIONAL OFFICES
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Cincinnati, Ohio (606) 371-0064

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
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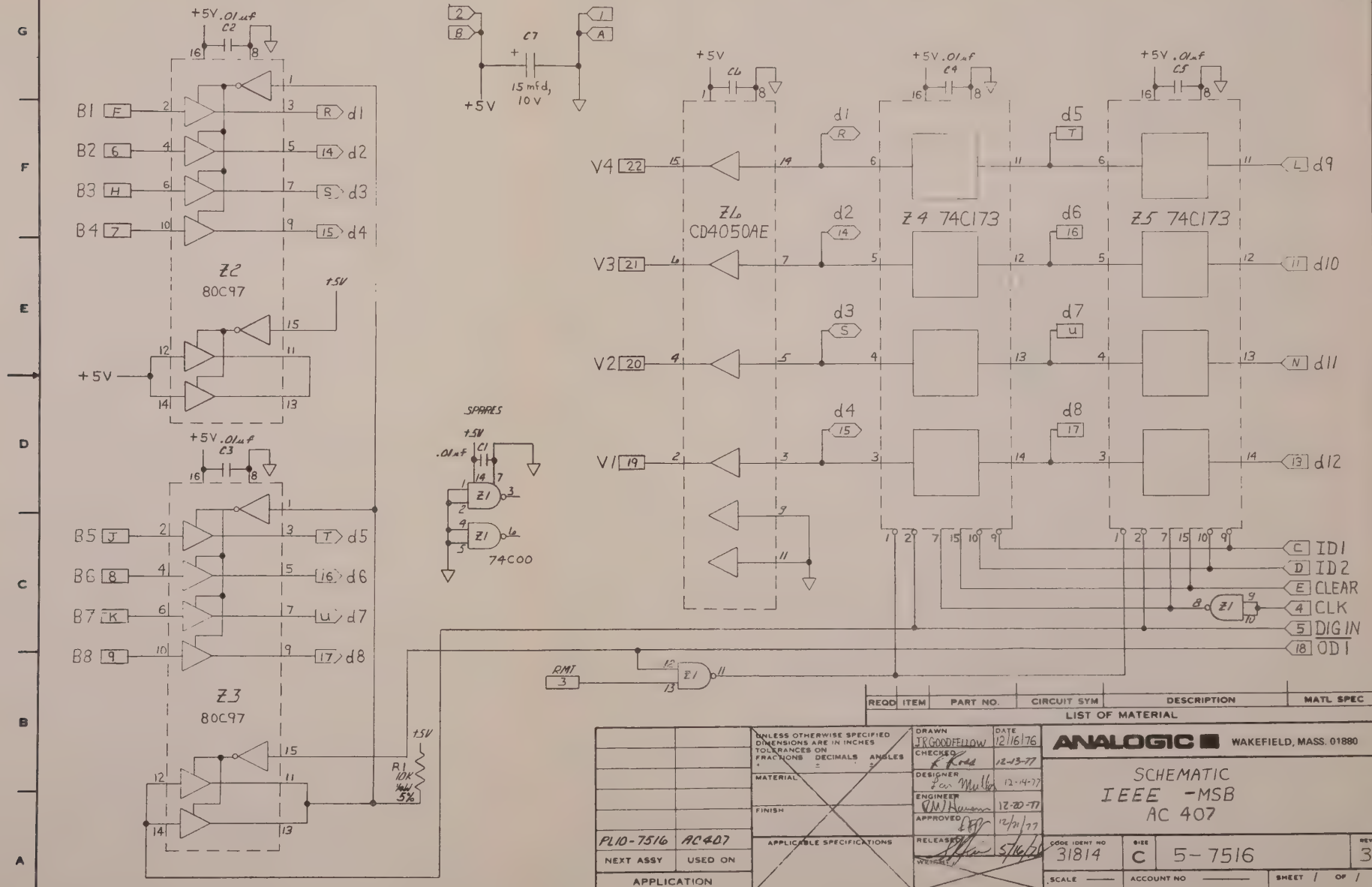
2	-	ENG. UPDATE	JI		11-22-77
3	4561	SEE E.C.O	RODP		12-9-80

SIZE C | 5-7516 | REV 3



REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-7516	AC407		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	JR GOODFELLOW	12/16/76
CHECKED	K Krall	12-13-77
DESIGNER	Jan Mullin	12-14-77
ENGINEER	RWJ Hansen	12-20-77
APPROVED	[illegible]	12/21/77
RELEASED	[illegible]	5/16/80
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC
IEEE -MSB
AC 407

CODE IDENT NO	SIZE		REV
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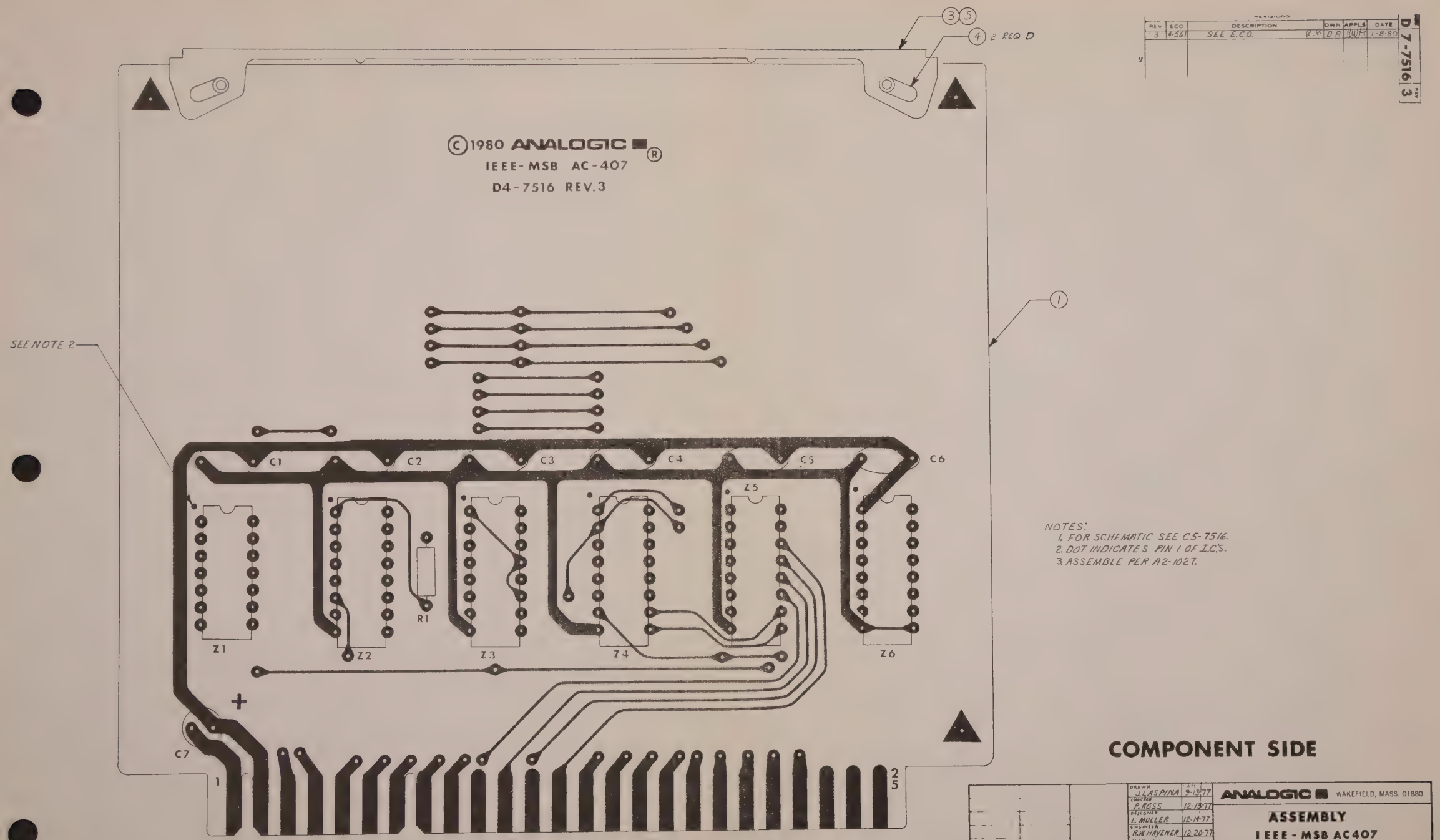
SCALE —	ACCOUNT NO —	SHEET 1 OF 1	



REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPR	DATE	
3	4-561	SEE E.C.O.	R.R.	D.R.	1-8-80	

D 7-7516 3

NOTES:
1. FOR SCHEMATIC SEE C.S- 7516.
2. DOT INDICATES PIN 1 OF I.C.'S.
3. ASSEMBLE PER A2-1027.

COMPONENT SIDE

DRAWN	J.LASPINA	9-13-77
CHECKED	R.ROSS	12-13-77
DESIGNED	L.MULLER	12-14-77
ENGINEER	R.W.HAVENER	12-20-77
	R.F.POWELL	12-21-77
	S.LEE	5-16-78

PL10-7516 AC407
APPLICATION

ANALOGIC WAKEFIELD, MASS. 01880

ASSEMBLY
IEEE-MSB AC407

31814 | D 7-7516 | REV 3

4:1 | ACCOUNT NO | SHEET 1 OF 1

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLD	DATE
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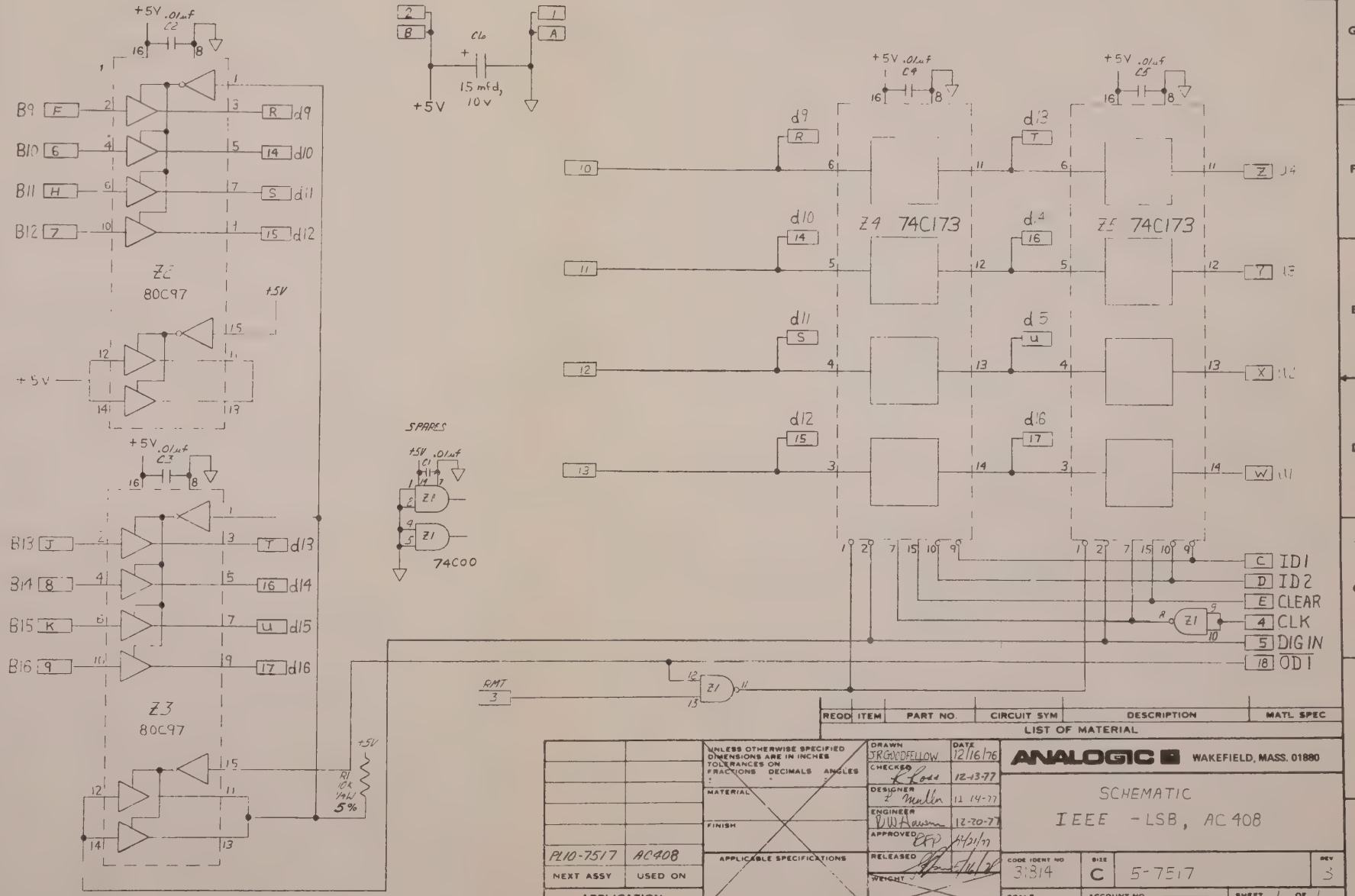
2	-	ENG UPDATE	JRL		11-22-77
3	4-562	SEE E.C.O	DP	MWB	1-13-80



REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-7517	AC408
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

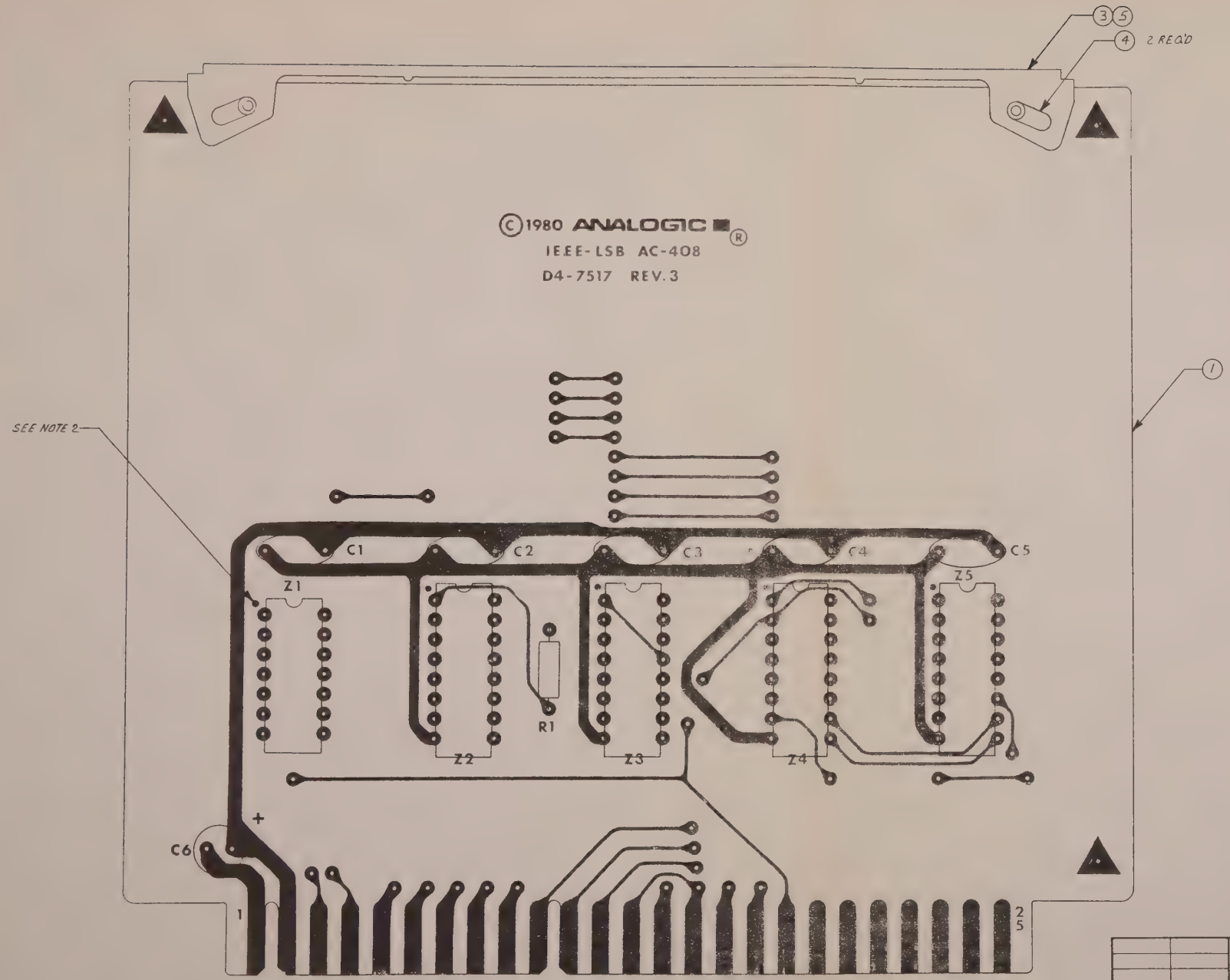
DRAWN	D.R.GOODFELLOW	DATE 12/16/76
CHECKED	K Rodd	12-13-77
DESIGNER	T Mullin	12 14-77
ENGINEER	D.W.Aaron	12-20-77
APPROVED	DEP	12/21/77
RELEASED		
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC

IEEE -LSB, AC 408

CODE IDENT NO	SIZE		REV
31814	C	5-7517	3
SCALE —	ACCOUNT NO —	SHEET 1 OF 1	



REVISIONS					
REV	E.C.O.	DESCRIPTION	DWN	APPD	DATE
3	4-562	SEE E.C.O.	R.L.D.R	[illegible]	7-10-80

D 7-7517 3

NOTES:
1. FOR SCHEMATIC SEE C5-7517.
2. DOT INDICATES PIN 1 OF I.C.'S.
3. ASSEMBLE PER A2-1027.

COMPONENT SIDE

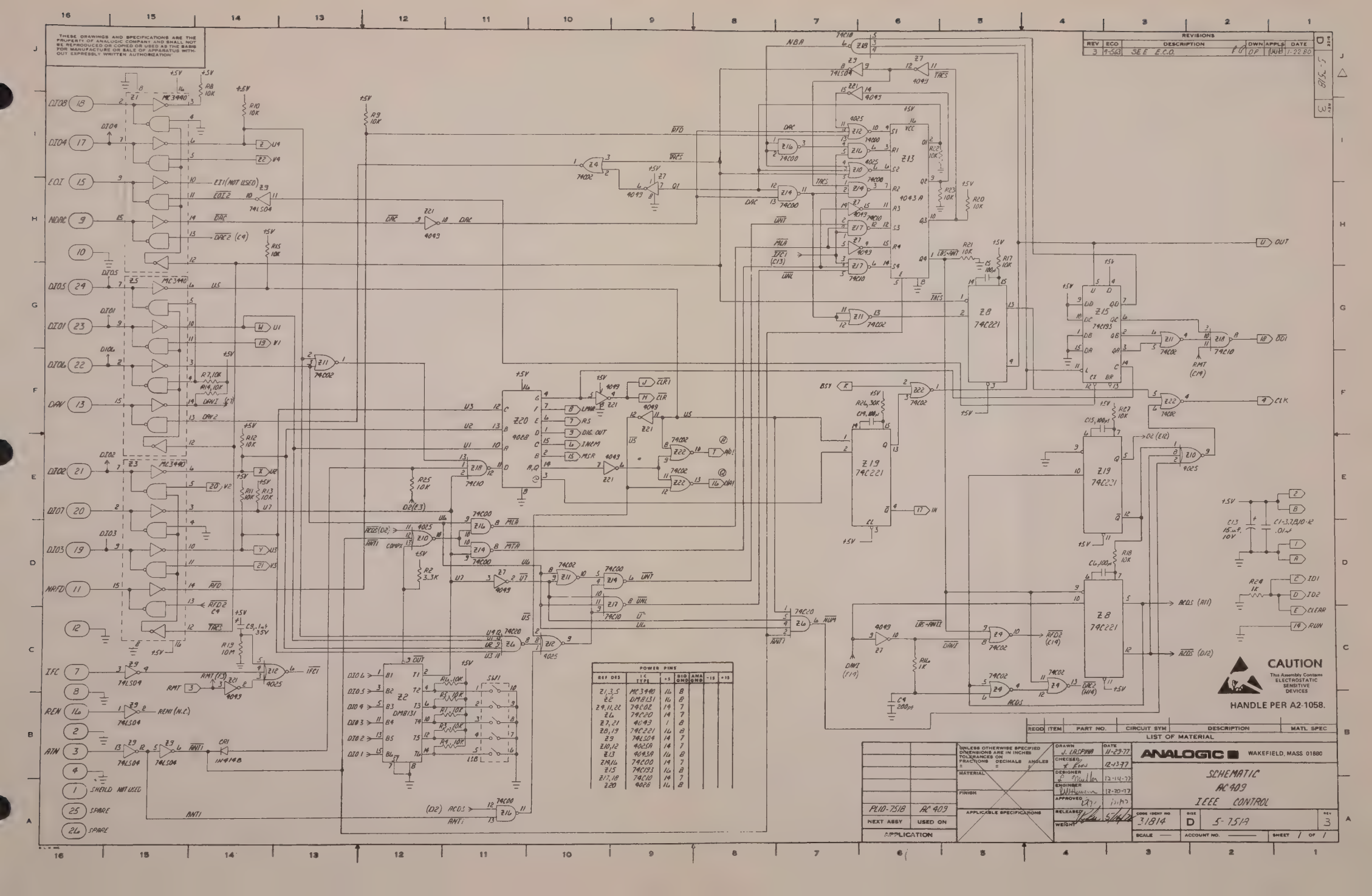
		DRAWN	W. LASPINA	9-13-77
		CHECKED	R. ROSS	12-13-77
		DESIGNER	L. MULLER	12-14-77
		ENGINEER	R.W. HAVENER	12-20-77
		APPROVED	R.F. POWELL	12-21-77
		RELEASED	S. LEE	5-16-78
		WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

ASSEMBLY
IEEE-LSB AC408

PL10-7517	AC408
NEXT ASSY	USED ON
APPLICATION	

CODE IDENT NO	SIZE		REV
31814	D	7-7517	3
SCALE 4:1	ACCOUNT NO		SHEET 1 OF 1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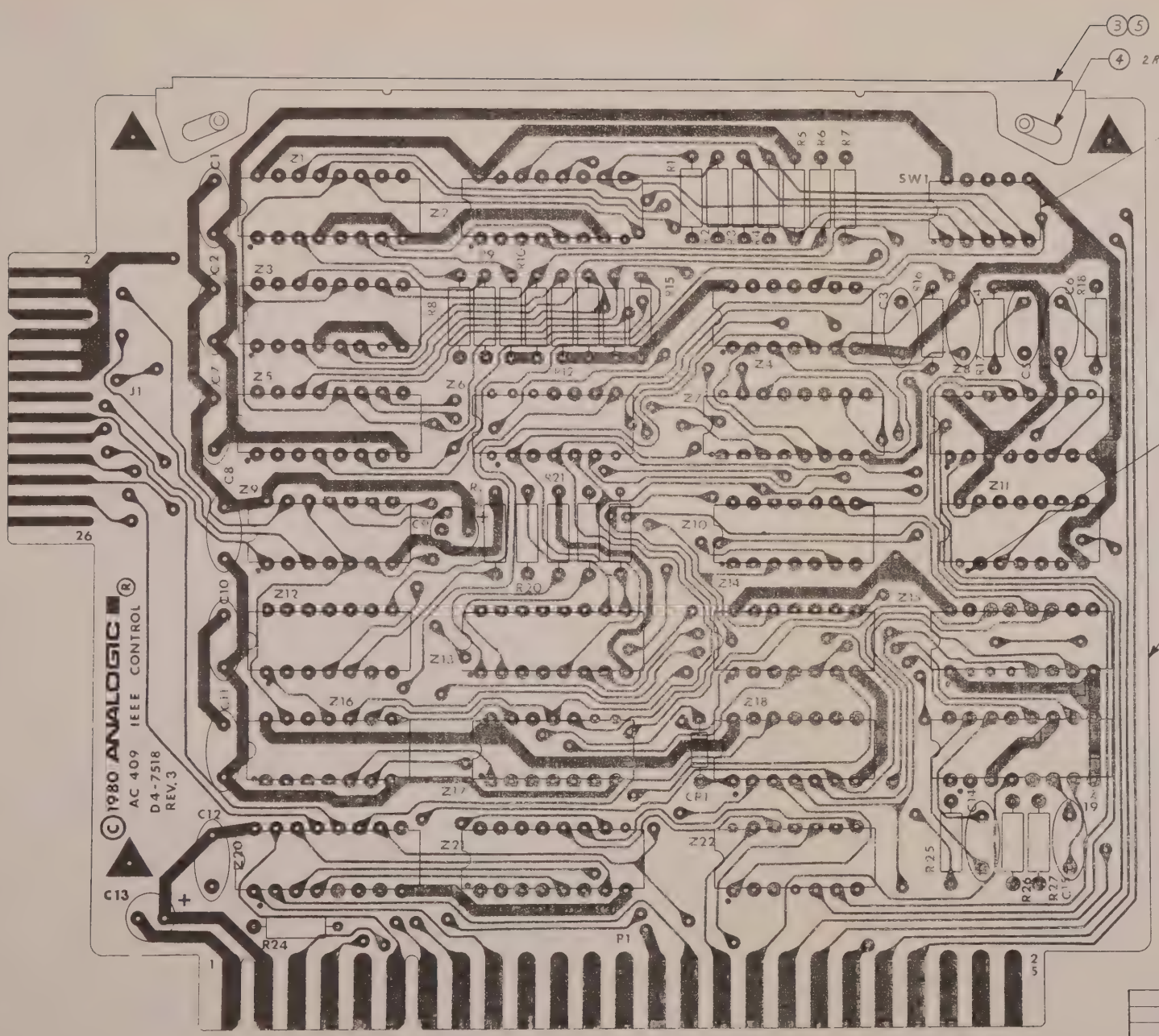
REVISIONS
REV ECO DESCRIPTION DWN APPD DATE
3 4-643 SEE E.C.O. PD DP WB 1-22-80
DIO8 DIO4 EOI NDAC DIO5 DIO1 DIOL DAV DIO2 DIO7 DIO3 NRFD IFC REN ATN SHIELD SPARE
MC3440 74LS04 74C02 74C00 74C10 74C20 74C221 74C193 4025 4049 4028 DM8131 4043A 74C00
R8 10K R9 10K R10 10K R12 10K R13 10K R15 10K R17 10K R18 10K R19 10M R20 10K R21 10K R22 10K R23 10K R24 1K R25 10K R2 3.3K
C9, 1mf 35V C13 15mf 10V C1-3,7,8,10-12 .01mf C4 200pf C5,100pf C6,100pf C14,100pf C15,100pf C19,30K C24,30K
IN4148 SW1 SIP
POWER PINS
REF DES I.C TYPE +5 BIG GND ANA GND -15 +15
Z1,3,5 MC3440 16 8
Z2 DM8131 16 8
Z4,11,22 74C02 14 7
Z6 74C20 14 7
Z7,21 4049 1 8
Z8,19 74C221 16 8
Z9 74LS04 14 7
Z10,12 4025A 14 7
Z13 4043A 16 8
Z14,16 74C00 14 7
Z15 74C193 16 8
Z17,18 74C10 14 7
Z20 4028 16 8
DIO1 DIO2 DIO3 DIO4 DIO5 DIO6 DIO7 DIO8
RFD DAC TACS LWT MLA UNL EOI1 EOI2 DAC2 RFD2 ANTI
BSY CLK DO1 DO2 IDO1 IDO2 CLEAR RUN
ACDS (A11) ACDS (D12) ACDS (H14)
LOAD RS DIG. OUT INCM MSR
CAUTION This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
LIST OF MATERIAL
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN J. LASPINA 11-29-77
CHECKED S. Lau 12-3-77
DESIGNER S. Mueller 12-14-77
ENGINEER W.H. Hansen 12-20-77
APPROVED 1/11/78
RELEASED 5/4/78
WEIGHT
ANALOGIC WAKEFIELD, MASS 01880
SCHEMATIC
AC 409
IEEE CONTROL
PL10-7518 AC 409
NEXT ASSY USED ON
APPLICATION
CODE IDENT NO 31814
SIZE D
5-7513
REV 3
SCALE —
ACCOUNT NO. ——
SHEET 1 OF 1



REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPR	DATE	
3	4563	SEE E.C.O.	DP	WR	1-22-80	

D 7-7518 3

NOTES:
1. FOR SCHEMATIC SEE D5-7518.
2. ASSEMBLE PER A2-1027.
3. DOT INDICATES PIN 1 OF I.C.'S & SWITCH.

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

COMPONENT SIDE

		DRAWN	J. ASPINA	12-2-77
			R. ROSS	12-13-77
		DESIGNED	L. MULLER	12-14-77
		ENGINEER	R.W. HAVENER	12-20-77
		APPROVED	R.F. POWELL	12-21-77
		QA	S. LEE	5-16-78
PL10-7518	AC 409			
APPLICATION				

ANALOGIC WAKEFIELD, MASS. 01880

ASSEMBLY
IEEE CONTROL
AC 409

SIZE	DWG NO	REV
31814	D 7-7518	3
SCALE 4:1	ACCOUNT NO	SHEET 1 OF 1

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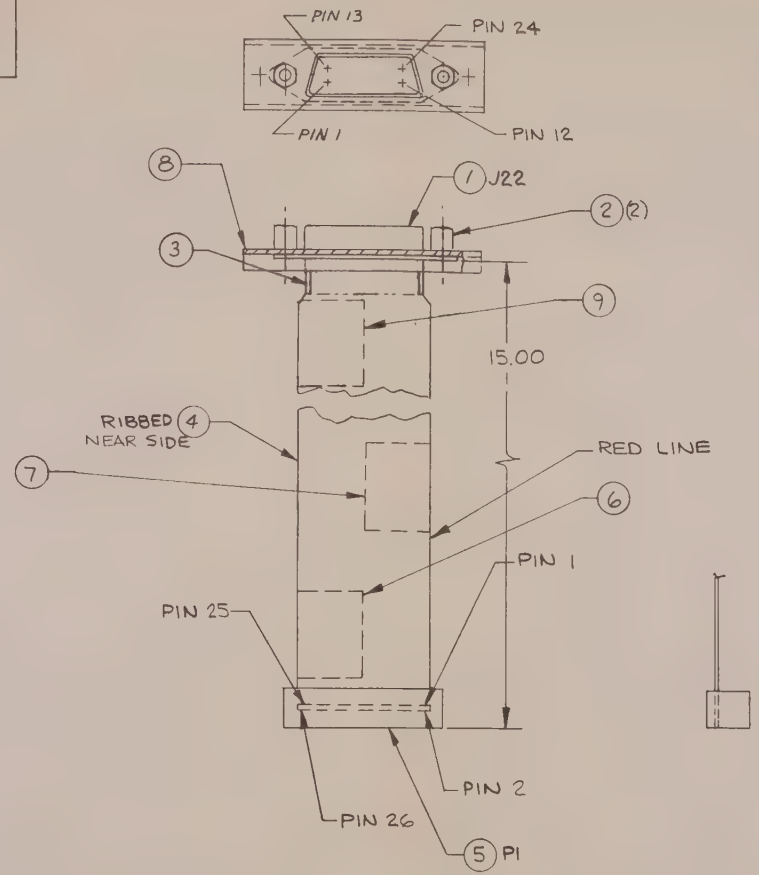
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1	—	REVISED WIRING TABLE	RJ		12DEC77

SIZE C 7-2307 REV 1



NOTES
1. ASSEMBLE ITEM 5 USING 3M PRESS OR EQUIV AND LOCATOR PLATE 3M # 3443-11 WITH PLATEN #3442-7
2. WIRE NO. 25 & 26 TRIM BACK APPROX. .25 FROM J22

WIRING TABLE

WIRE NO.	FROM	TO	FUNCTION
1	P1-1	J22-12	SHLD
2	2	24	GND(LOGIC)
3	3	11	ATN
4	4	23	GND(11)
5	5	10	SRQ
6	6	22	GND(10)
7	7	9	IFC
8	8	21	GND(9)
9	9	8	NDAC
10	10	20	GND(8)
11	11	7	NRFD
12	12	19	GND(7)
13	13	6	DAV
14	14	18	GND(6)
15	15	5	EIO
16	16	17	REN
17	17	4	DIO4
18	18	16	DIO8
19	19	3	DIO3
20	20	15	DIO7
21	21	2	DIO2
22	22	14	DIO6
23	23	1	DIO1
24	24	J22-13	DIO5
25	25	—	NOTE 2
26	P1-26	—	NOTE 2

PL10-3707	AN5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X ± .XX ± .25 .XXX ±
ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	K. CARTER	9-9-77
CHECKED	K. [illegible]	19 OCT 77
ENGINEER	J. Mull[illegible]	12-13-77
ENGINEERING MGR.	[illegible]	12-20-77
QUALITY CONTROL	[illegible]	12/21/77
PRODUCTION	[illegible]	12/16/77
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

CABLE ASSY CONN. INTERFACE(IEEE)

CODE IDENT NO	SIZE		REV
31814	C	7-2307	1
SCALE 1/1		SHEET 1 OF 1	

7.5 Signal Processor

7.5.0 General

Following the slot connections for the signal processor and A/D converter is an index of the data sheets, drawings, and schematics in this section.

7.5.1 J73 (Signal Processor) Slot Connections

Signal Name	Conn.	To	From	Function
DIG. GND.	J73-1		PS	Digital Ground
+5	J73-2		PS	+5 Volt Power
	J73-3			
TRIG	J73-4		J28	User Controlled Ext. Trigger
RDY TO MSR	J73-5	J28		Synchronizes Ext. A/D Trigger
	J73-6			
$\overline{BX0}$	J73-7		FP	Low When Chassis 0 Is Addressed
$\overline{SE}$	J73-8		FP	Low For Single-ended Operation
	J73-9			
	J73-10			
	J73-11			
	J73-12			
	J73-13			
	J73-14			
	J73-15			
SIG RTN	J73-16		UC	Analog Signal Return Bus
SIG RTN	J73-17		UC	Analog Signal Return Bus
EVEN	J73-18		UC	Analog Even (+) Bus
ODD	J73-19		UC	Analog Odd (−) Bus
	J73-20			
	J73-21			
ADC GND	J73-22		ADC	Clean, ADC Referenced Ground
−15	J73-23		PS	−15 Volt Power
+15	J73-24		PS	+15 Volt Power
ANA. GND.	J73-25		PS	Analog Ground
DIG. GND.	J73-A		PS	Digital Ground
$\overline{+5}$	J73-B		PS	+5 Volt Power
$\overline{EOC}$	J73-C		ADC	End Of Conversion From ADC
A/D TRIG	J73-D	ADC		Trigger A/D Conversion
BSY	J73-E	INT		High During Measuring Process
$\overline{MSR1}$	J73-F		FP	Starts Measuring Process
$\overline{CLR}$	J73-H		INT	General Clearing Pulse
$\overline{CLR1}$	J73-J		INT	Limited Clearing Pulse
	J73-K			
	J73-L			
	J73-M			
	J73-N			
	J73-P			
A12	J73-R		FP	LSB Of Address Register
M1	J73-S		FP	Gain Setting Bit
M2	J73-T		FP	Gain Setting Bit
$\overline{M3}$	J73-U		FP	Gain Setting Bit
$\overline{GA}$	J73-V		FP	Decoded Gain Bit
	J73-W			
ANA. GND.	J73-X		PS	Analog Ground
SP-ADC	J73-Y	ADC		Sig Proc Analog Output
ADC GND.	J73-Z		ADC	Clean, A/D Referenced Ground
−15	J73-AA		PS	−15 Volt Power
+15	J73-BB		PS	+15 Volt Power
ANA. GND.	J73-CC		PS	Analog Ground

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7.5.2 J74 (A/D Converter) Slot Connections

Signal Name	Conn.	To	From	Function
DIG. GND.	J74-1		PS	Digital Ground
+5	J74-2		PS	+5 Volt Power
$\overline{EOC}$	J74-3	SP		End Of Conversion (Low When Completed)
A/D TRIG	J74-4		SP	Trigger Pulse To Start Conversion
	J74-5			
B2	J74-6	INT,FP		A/D Output Bit 2
B4	J74-7	INT,FP		A/D Output Bit 4
B6	J74-8	INT,FP		A/D Output Bit 6
B8	J74-9	INT,FP		A/D Output Bit 8
B10	J74-10	INT,FP		A/D Output Bit 10
B12	J74-11	INT,FP		A/D Output Bit 12
B14	J74-12	INT,FP		A/D Output Bit 14
B16	J74-13	INT,FP		A/D Output Bit 16*
	J74-14			
	J74-15			
	J74-16			
	J74-17			
	J74-18			
	J74-19			
	J74-20			
SP-ADC	J74-21		SP	Analog Input Signal
ADC. GND.	J74-22	SP		A/D Referenced Ground
−15	J74-23		PS	−15 Volt Power
+15	J74-24		PS	+15 Volt Power
ANA. GND.	J74-25		PS	Analog Ground
DIG. GND.	J74-A		PS	Digital Ground
+5	J74-B		PS	+5 Volt Power
	J74-C			
	J74-D			
	J74-E			
B1	J74-F	INT,FP		A/D Output Bit 1
B3	J74-H	INT,FP		A/D Output Bit 3
B5	J74-J	INT,FP		A/D Output Bit 5
B7	J74-K	INT,FP		A/D Output Bit 7
B9	J74-L	INT,FP		A/D Output Bit 9
B11	J74-M	INT,FP		A/D Output Bit 11
B13	J74-N	INT,FP		A/D Output Bit 13*
B15	J74-P	INT,FP		A/D Output Bit 15*
	J74-R			
	J74-S			
	J74-T			
	J74-U			
	J74-V			
	J74-W			
	J74-X			
SP-ADC	J74-Y		SP	Analog Input
ADC. GND.	J74-Z	SP		A/D Referenced Ground
−15	J74-AA		PS	−15 Volt Power
+15	J74-BB		PS	+15 Volt Power
ANA. GND.	J74-CC		PS	Analog Ground

* These bits may not be used, depending on the resolution of the ADC.

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Section 7.5
Signal Processor & A/D Converter

Card Number	Drawing Number	Title
—	—	AC260/AC262 Signal Processor Data Sheet
AC260	D5-7430	Signal Processor Schematic
AC260	D7-7430	Signal Processor Assembly
AC262, AC265	C5-7462	Signal Processor Schematic
AC262, AC265	D7-7462	Signal Processor Assembly
AC2700/AC8000	—	AC2700/AC8000 Series ADC Data Sheet
MP2700	—	MP2700 C Series 10, 12, 13, and 14-bit ADC's Data Sheet
AC27XX	D5-7441	Mother Board for MP27XX Schematic
AC2XXX	D7-7441	Mother Board for MP27XX Assembly
—	—	MP8000 Series 14, 15, and 16-bit ADC's Data Sheet
AC8XXX	C5-7442	ADC Mother Board Schematic
AC8XXX	D7-7442	ADC Mother Board Assembly

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AC260/AC262

ANALOG SIGNAL PROCESSORS FOR ANDS5400

GENERAL DESCRIPTION

The **AC260** and the **AC262** are Analog Signal Processors for the ANDS5400 System. These cards receive analog signals from the Input Multiplexer Cards in the Master Box or Slave Boxes and buffer these signals to drive the A/D Converter. Additionally, certain timing and control functions related to the measurement process take place on the Signal Processor Card.

AC262

The **AC262** contains a Sample and Hold located just before the A/D Converter. This Sample and Hold is commanded into "HOLD" mode just before every conversion, returning to "SAMPLE" immediately after the conversion is complete. This Sample and Hold is necessary in all Data Acquisition Systems because of the nature of successive approximation A/D Converters. These converters must have a constant input during the conversion process. Valid measurements may be made on a changing signal only if the signal is temporarily held constant during the conversion process.

AC260

The **AC260** provides the Sample and Hold function as described for the **AC262** and a programmable gain amplifier circuit preceding the Sample and Hold. Prior to each conversion, the amplifier circuit executes an auto zero sequence. This is accomplished with the amplifier gain set at the value to be used for that measurement cycle. The auto zero function therefore compensates for the inherent amplifier offset at the selected gain.

OPERATION

The **AC260** and **AC262** perform different functions based on the code stored in the range register and displayed on the front panel range lights. The range codes control single-ended or differential operation. In the case of the **AC260**, they also establish the amplifier gain. (Gain settings of the **AC260** are detailed in Table 1). The measurement rate and accuracy of the system are unaffected by gain changes from channel to channel or on the same channel.

SPECIFICATIONS

Input Impedance	$>10^9\Omega$
Bias Current	<10nA @ 25°C
Signal + Common Mode Voltage	11.24V (10.24V SIG + 1V CMV)
Common Mode Rejection	>80dB (dc-60Hz)
Offset	Adjustable to zero
Gain Accuracy	±0.01% FSR
Linearity	±0.003% FSR
Noise (R.T.O.)*	<0.5mV p-p
Tempco of Offset	$<50\mu$V/°C
Tempco of Gain	<20ppm/°C
Settling Time to 0.01% FSR:	
AC260	12μs
AC260 & System	15μs
AC262	5μs
AC262 & System	6μs

*Referenced to Output

Octal Range Code	Function	Gain
0	SE	Unity
1	SE	2
2	SE	4
3	SE	8
4	Not Used	
5	Not Used	
6	Not Used	
7	Not Used	
10	DI	Unity
11	DI	2
12	DI	4
13	DI	8

SE = Single Ended Input
DI = Differential Input

TABLE 1. AC260 Amplifier Gain Settings

ANALOGIC®
...The Digitizers

CALIBRATION

Three potentiometers on each processor allow the user to set delays and offset (Figures 5 and 6). These are useful for calibration and for optimizing system performance.

R17 = Auto Zero Delay (T1) Control
R19 = System Settling Time (T1) Control
R31 = Sample & Hold Offset Control
∗ = Factory Set. Do Not Use.

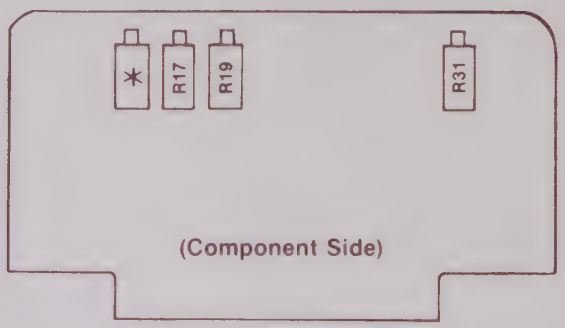

Figure 5. AC260 Controls

R15 = System Settling Time (T1) Control (Present to 6μs)
R16 = Sample & Hold Offset Control
R14 = Differential Amplifier Offset Control
∗ = Factory Set. Do Not Use.

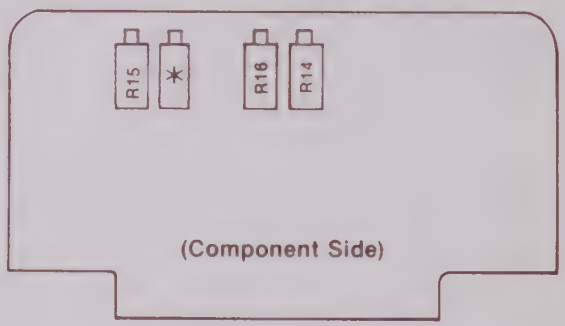

Figure 6. AC262 Controls

ORDERING GUIDE

Simply Specify
Analogic AC260
(With Programmable Gain Amplifier)
or AC262
(Without Programmable Gain Amplifier)

An Invitation...

The products and system supported by this data sheet are intended to be general purpose in nature and to offer maximum flexibility for solving the wide variety of problems typically found in Industrial and Scientific applications. Analogic recognizes that these specific products do not necessarily solve all types of requirements since each may have individual technical and economic criteria. Analogic maintains an experienced staff of professional engineers committed to providing unique engineering solutions to those data acquisition needs. The Analogic staff, which has been responsible for hundreds of patents, and many times that number of proprietary circuits and devices, is prepared to serve you. We believe that you will find us eminently qualified to work closely with you to develop and supply optimized solutions to your Data Acquisition problems. Call us!

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Tel. (617) 246-0300 ■ TWX (710) 348-0425 ■ Telex 94-9307
ANALOGIC AG ■ Kanalstrasse 15 ■ Postfach CH-8152 ■ Glattbrugg ■ Switzerland
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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1	—	ENG UPDATE	W.M	[illegible]	[illegible]
2		ENG UPDATE	BR	[illegible]	5-5-76
3	—	ENG UPDATED	NC	[illegible]	7-26-76
4	[illegible]	REV UPDATE	[illegible]	J.L.	8-9-77
5	4-676	SEE E.C.O.	[illegible]	L.J.M.	2-3-78
6	4-551	SEE E.C.O.	[illegible]	D.P.	1-16-79
7	4-653	SEE ECO	[illegible]	D.P.	2-5-79

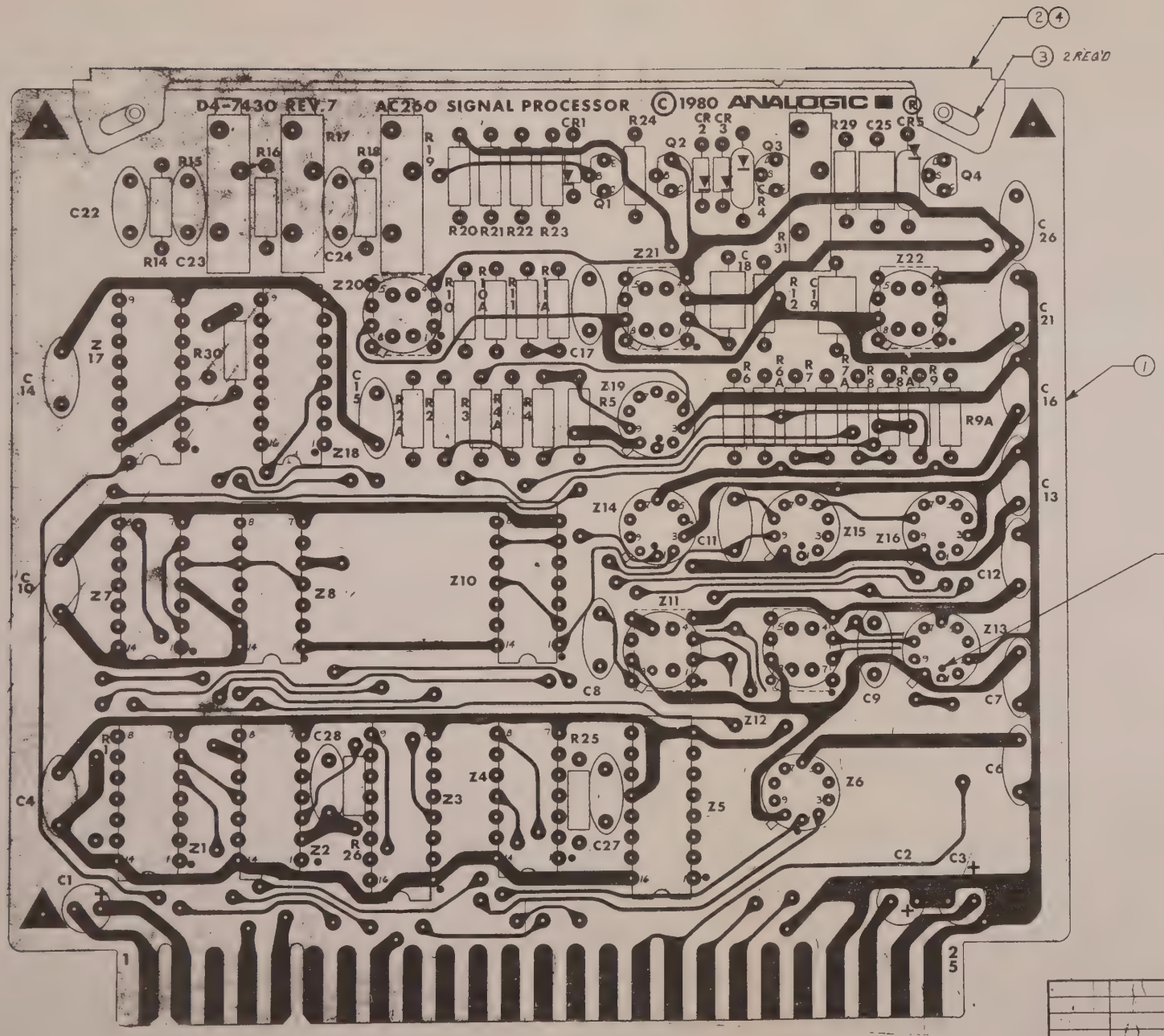
I.C.	DEVICE	+5V	GND	+15V	-15V	15RTN
Z17,18	74C221	16	8			
Z11,12,20 Z1,22	2605			7	4	
Z10,2	74C02	14	7			
Z7,14	74C74	14	7			
Z6,9 Z15,16,19	DG200			10	6	3
Z3	4049	1	8			
Z4	74C00	14	7			

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN	DATE	ANALOGIC WAKEFIELD, MASS. 01880
MATERIAL	CHECKED		SIGNAL PROCESSOR AC2260
FINISH	DESIGNER		
	ENGINEER		
	APPROVED		
PL10-7430 AC2260	RELEASED		CODE IDENT NO 31814 SIZE D 5-7430 REV 7
NEXT ASSY USED ON	WEIGHT		SCALE ACCOUNT NO. SHEET 1 OF 1
APPLICATION	APPLICABLE SPECIFICATIONS		

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2 1058.



REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE
7	4653	SEE E.C.O	R.B	O.R	2-19-80

D 7-7430 REV 7

NOTES:
1. FOR SCHEMATIC SEE D5-7430.
2. DOT INDICATES PIN 1 OF I.C.'S.
3. ASSEMBLE IN ACCORDANCE WITH A2-1027.

		DRAWN	B ROSS	5-5-76
		CHECKED	R PERRY	8-17-76
		DESIGNER	R.W. HAVENER	8-17-76
		ENGINEER	E. DINOWITZ	8-19-76
		APPROVED	R POWELL	8-19-76
		RELEASED	R PEARE	8-19-76
		WEIGHT		
PL10-7430	AC 260			
NEXT ASSY	USED ON			
APPLICATION				

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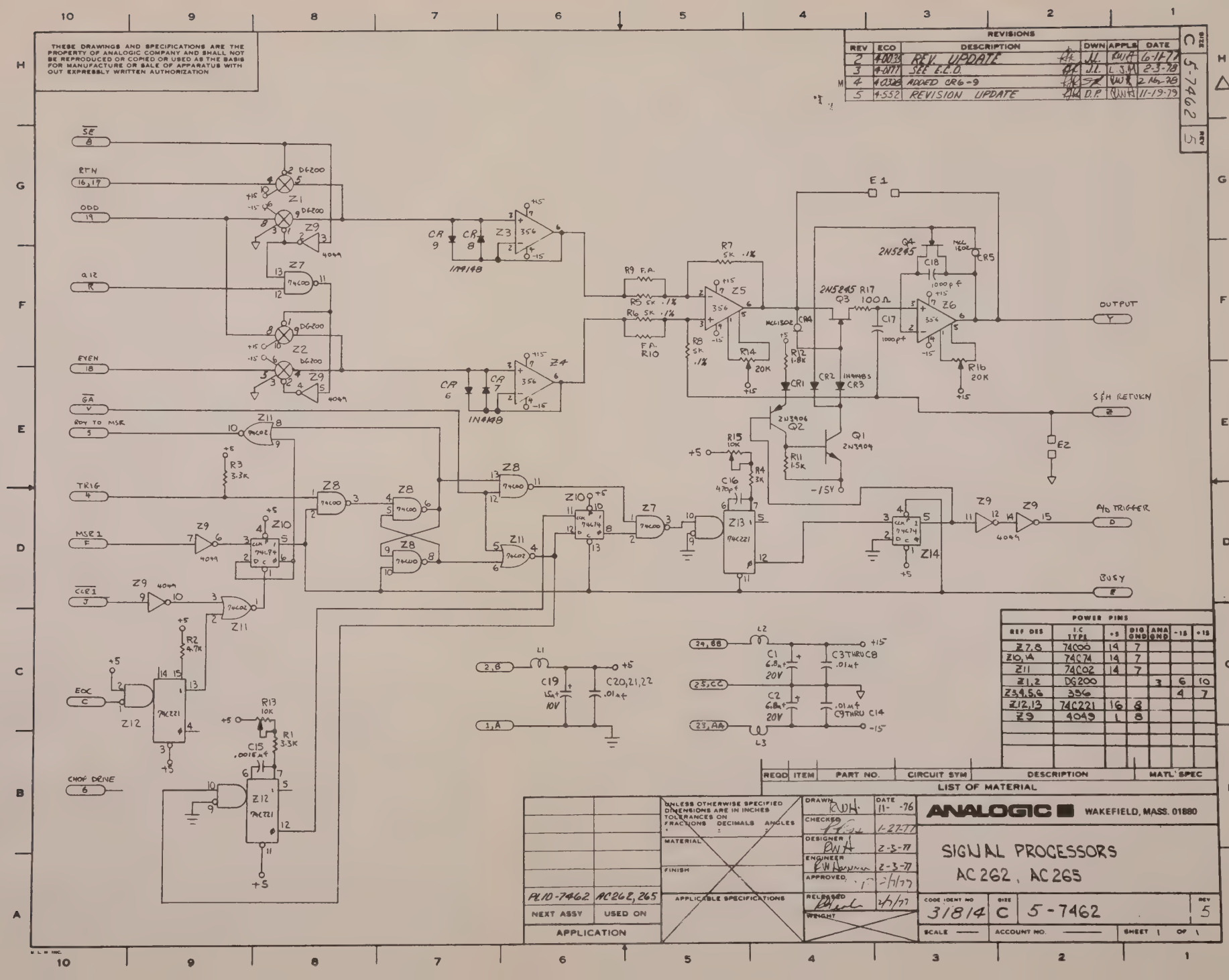
ANALOGIC WAKEFIELD, MASS. 01880

ASSEMBLY
SIGNAL PROCESSOR
AC 260

CODE IDENT NO	SIZE		REV
31814	D	7-7430	7
SCALE 4:1	ACCOUNT NO:		SHEET 1 OF 1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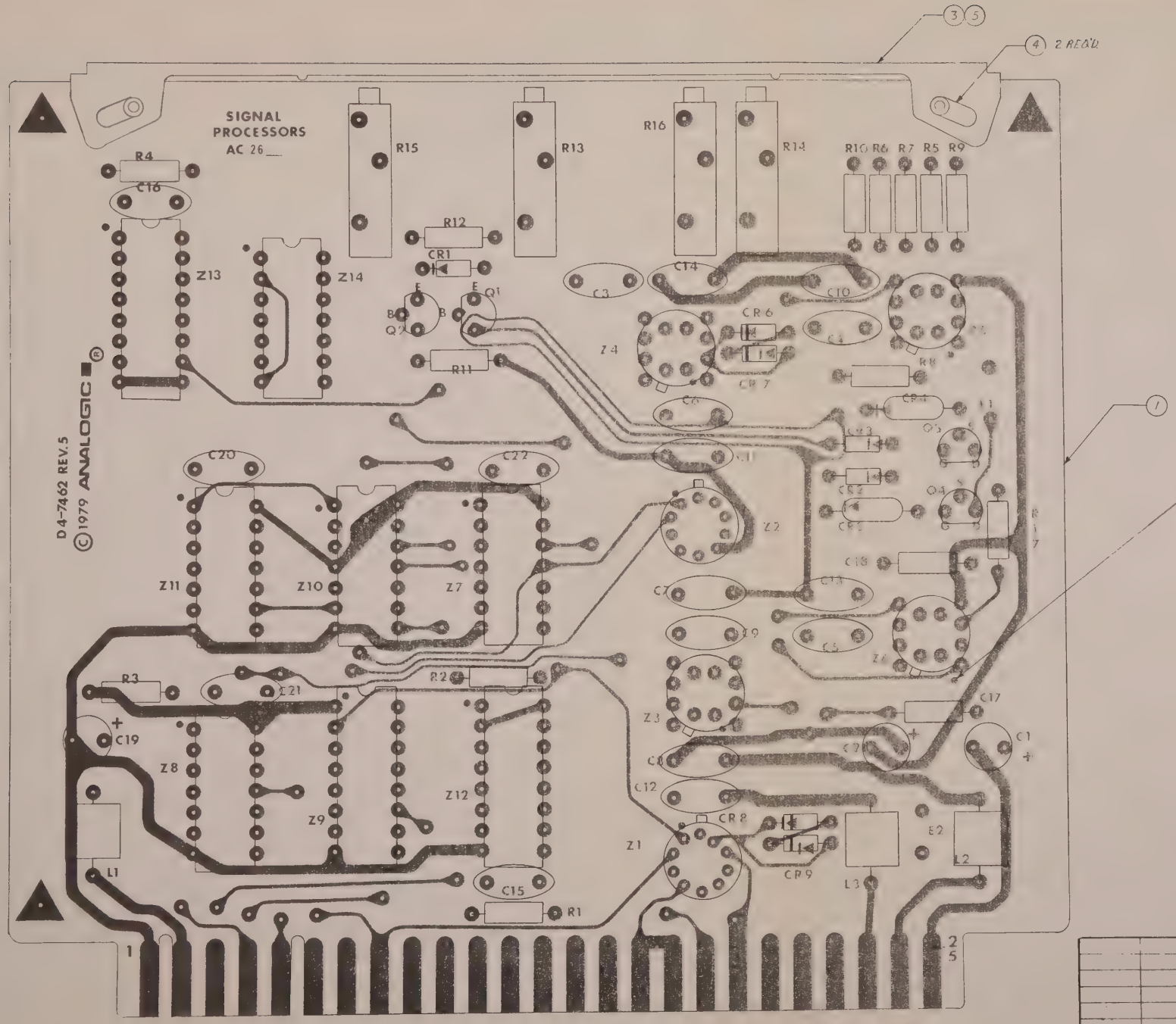
REVISIONS
REV ECO DESCRIPTION DWN APPR DATE
2 4-0038 REV. UPDATE RWH 6-14-77
3 4-0111 SEE E.C.O. RWH J.L. L.S.M. 2-3-78
4 4-0326 ADDED CR6-9 RWH S.R. W.K. 2 Nov 78
5 4-552 REVISION UPDATE RWH D.P. RWH 11-19-79
C 5-7462 5
SE B
RTN 16,17
ODD 19
Q 12
R
EVEN 18
GA V
RDY TO MSR 5
TRIG 4
MSR 1 F
CLR 1 J
EOC C
CHOP DRIVE 6
Z1 DG200
Z2 DG200
Z3 356
Z4 356
Z5 356
Z6 356
Z7 74C00
Z8 74C00
Z9 4049
Z10 74C74
Z11 74C02
Z12 74C221
Z13 74C221
Z14 74C74
CR 9
CR 8
CR 7
CR 6
IN4148
R1 3.3K
R2 4.7K
R3 3.3K
R4 3K
R5 5K .1%
R6 5K .1%
R7 5K .1%
R8 5K .1%
R9 F.A.
R10 F.A.
R11 1.5K
R12 1.8K
R13 10K
R14 20K
R16 20K
C15 .0015μf
C16 470pf
C17 1000pf
C18 1000pf
C19 15μf 10V
C20,21,22 .01μf
C1 6.8μf 20V
C2 6.8μf 20V
C3 THRU C8 .01μf
C9 THRU C14 .01μf
L1
L2
L3
2,B
1,A
24,BB
25,CC
23,AA
Q1 2N3904
Q2 2N3906
Q3 100Ω
Q4 2N5245
2N5245
MCL1502
CR1
CR2
CR3
CR4
CR5
E1
E2
OUTPUT Y
S&H RETURN Z
A/D TRIGGER D
BUSY E
+15
-15
+5
POWER PINS
REF DES I.C. TYPE +5 DIG GND ANA GND -15 +15
Z7,8 74C00 14 7
Z10,14 74C74 14 7
Z11 74C02 14 7
Z1,2 DG200 3 6 10
Z3,4,5,6 356 4 7
Z12,13 74C221 16 8
Z9 4049 1 8
REQD ITEM PART NO. CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN RWH DATE 11-76
CHECKED 1-27-77
DESIGNER RWH 2-3-77
ENGINEER RW Hannum 2-3-77
APPROVED 2/7/77
RELEASED 2/9/77
WEIGHT
PL10-7462 AC262,265
NEXT ASSY USED ON
APPLICATION
ANALOGIC WAKEFIELD, MASS. 01880
SIGNAL PROCESSORS
AC 262, AC 265
CODE IDENT NO 31814 SIZE C 5-7462 REV 5
SCALE ACCOUNT NO. SHEET 1 OF 1



REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
5	9552	SEE E.C.O.	G.P.		JULY 20 79

D 7-7462 5

NOTES:
1. FOR SCHEMATIC SEE C.S-7462.
2. DOTS INDICATE PIN 1 OF I.C.'s.
3. ASSEMBLE PER A2-1027.

COMPONENT SIDE

	DRAWN	1-27-77	ANALOGIC WAKEFIELD, MASS. 01880
	CHECKED R. ROSS	1-27-77	ASSEMBLY
	ENGINEER R. HAVENER	2-3-77	SIGNAL PROCESSORS AC 262, AC 265
	APPROVED R. HAVENER	2-3-77	
	RELEASED R. POWELL	2-7-77	
	WEIGHT R. PEAKE	2-7-77	
PL10-7462 AC 262, 265			CODE IDENT NO 31814 SIZE D 7-7462 REV 5
NEXT ASSY USED ON			SCALE 4:1 ACCOUNT NO SHEET / OF /
APPLICATION			

AC2700/AC8000 SERIES

ANALOG/DIGITAL CONVERTERS for the ANDS5400

GENERAL DESCRIPTION

The unusual flexibility of the ANDS5400 Data Acquisition System permits the use of a variety of high performance analog-to-digital (A/D) converters.Two standard A/D converter series, the AC2700 and AC8000, provide the combination of resolutions, output codes, accuracies, temperature coefficients, and conversion times required by a large variety of applications. With these series, resolutions of 12 to 16 bits and system speeds of up to 100,000* conversions per second are available. Basic system throughput rates for the various combinations of A/D's and signal processors are shown in Table 1.

AC2700 Series

The AC2700 series A/D converters provide high speed and superior performance with resolutions of 12 to 14 bits. The low temperature coefficients exhibited by these units assure monotonicity, linearity, and uniformity of code width over a wide operating temperature range. Their extremely conservative worst case design and exhaustive error budget analysis have resulted in differential linearity temperature coefficients as low as ±3ppm/°C FSR.

Using the AC2700 series A/D converters will yield system digitizing rates of up to 100,000 conversions per second.* This very high throughput capability offers economical solutions to requirements for high speed, accurate data conversion.

AC8000 Series

The AC8000 series A/D converters offer very high speed analog-to-digital conversion at resolutions of 14 to 16 bits. Premium components assure outstanding accuracy, linearity, speed, and stability.

Depending on the resolution, relative accuracies of ±0.006% to ±0.0015% FSR are provided. The AC8000 series assures long-term stability, and is characterized by tempco's of differential linearity, offset, and gain which are low enough to provide guaranteed monotonicity and no missing codes over the normal system operating temperature range.

*See Table 1.

SPECIFICATIONS [1]

	AC2700	AC8000
Analog Input	±10V, ±5V, 0-10V, 0-5V	0-10V, ±10V
Differential Linearity	±0.012%to ±0.006% FSR	±0.006% to ±0.003% FSR
Gain Tempco	12-8ppm/°C max.	6ppm/°C max.
Offset Tempco	12ppm/°C max.	1.5ppm/°C typ., 3ppm/°C max.
Differential Linearity Tempco	±3ppm/°C max.	1ppm/°C typ., 2ppm/°C max.
Missing Codes	None	None
Conversion Time [2]	4 μsec to 10 μsec	10 μsec to 32 μsec
Operating Temp.	0-70°C	0-60°C
Warm-Up to Specified Accuracy	5 minutes	10 minutes
Dimensions(Rounded)	4" x 5"	Same

Notes:

1. See also MP2700 and MP8000 Series Data Sheets
2. A/D only. See Table 1.

TABLE 1. BASE SYSTEM THROUGHPUT RATES

	A/D Used	Signal Processor Used	
		AC262	AC260
AC2700 Series	AC2712	100kHz	50kHz
	AC2713	60kHz	50kHz
	AC2714	60kHz	38kHz
AC8000 Series	AC8014	60kHz	38kHz
	AC8015	40kHz	30kHz
	AC8016	23kHz	18kHz

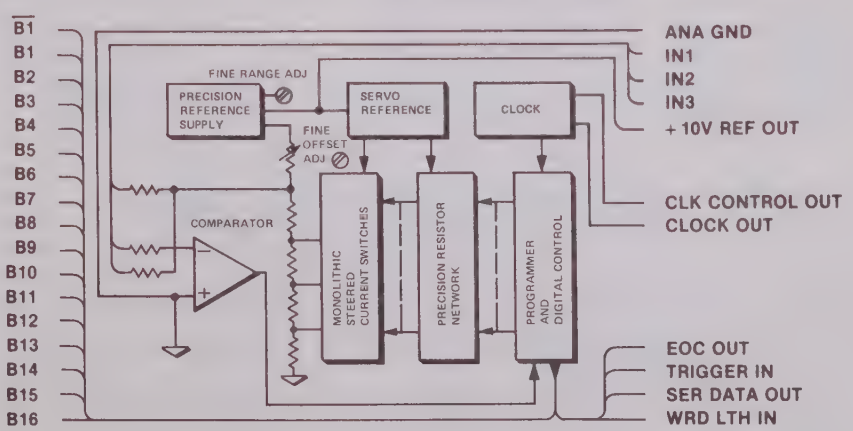


Figure 1. Typical A/D Block Diagram

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...The Digitizers

TABLE 2. OUTPUT CODING

12 BIT RESOLUTION (AC2712XX)		13 BIT RESOLUTION (AC2713XX)		14 BIT RESOLUTION (AC2714XX) (AC8014XX)		15 BIT RESOLUTION (AC8015XX)		16 BIT RESOLUTION (AC8016XX)	
Unipolar Binary		**Unipolar Binary**		**Unipolar Binary**		**Unipolar Binary**		**Unipolar Binary**	
Input	B1, B2.....B12	Input	B1, B2, ...B13	Input	B1, B2 .B13, B14	Input	B1, B2.....B14, B15	Input	B1, B2..... .B15, B16
+9.9976V	= 111 111 111 111	+9.9988V	= 1 111 111 111 111	+9.99939V	= 11 111 111 111 111	+9.99970V	= 111 111 111 111 111	+9.99985V	= 1 111 111 111 111 111
0.0000V	= 000 000 000 000	0.0000V	= 0 000 000 000 000	0.00000V	= 00 000 000 000 000	0.00000V	= 000 000 000 000 000	0.00000V	= 0 000 000 000 000 000
2's Complement*		**2's Complement***		**2's Complement***		**2's Complement***		**2's Complement***	
Input	$\overline{B1}$, B2.....B12	Input	$\overline{B1}$, B2.....B13	Input	$\overline{B1}$, B2 .B13, B14	Input	$\overline{B1}$ B2.....B14, B15	Input	$\overline{B1}$, B2.....B15, B16
+9.9951V	= 011 111 111 111	+9.9976V	= 0 111 111 111 111	+9.99878V	= 01 111 111 111 111	+9.99939V	= 011 111 111 111 111	+9.99970V	= 0 111 111 111 111 111
0.0000V	= 000 000 000 000	0.0000V	= 0 000 000 000 000	0.00000V	= 00 000 000 000 000	0.00000V	= 000 000 000 000 000	0.00000V	= 0 000 000 000 000 000
−10.0000V	= 100 000 000 000	−10.0000V	= 1 000 000 000 000	10.00000V	10 000 000 000 000	−10.00000V	= 100 000 000 000 000	10.00000V	= 1 000 000 000 000 000

*To change to Offset Binary, use B1 instead of $\overline{B1}$. B1 is the MSB. For calibration information, refer to MP2700 and MP8000 Series data sheets and ANDS5400 Manual

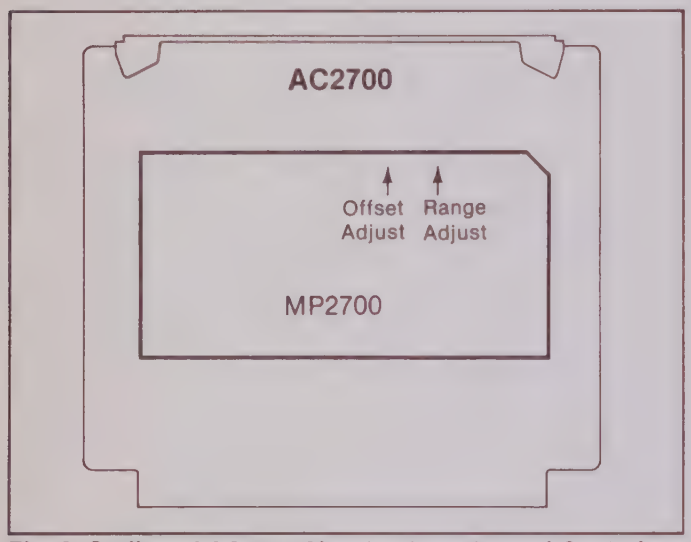

Fig. 2. Outline of AC2700 Showing Locations of Controls.

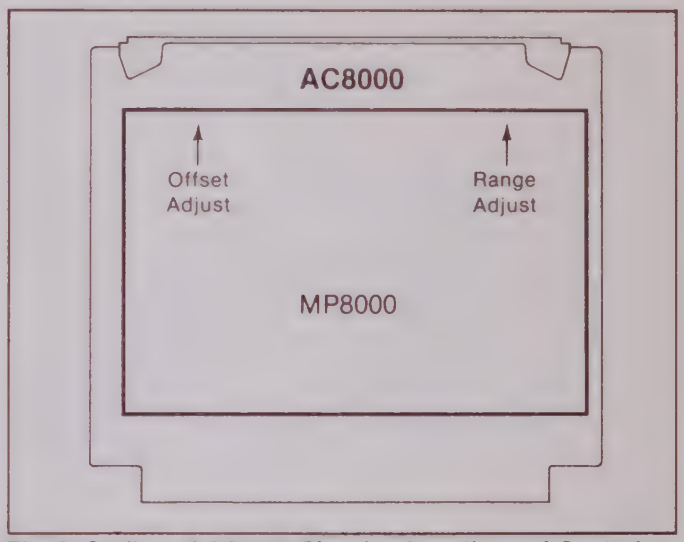

Fig. 3. Outline of AC8000 Showing Locations of Controls.

AC2700 ORDERING GUIDE

Simply Specify ——— AC27[ ][ ]

For Resolution Of:	Enter
12 Bits	12
13 Bits	13
14 Bits	14

For Full Scale Range Of:	Enter
0 to +10V (Binary Coding)	1A
−10V to +10V (2's Complement Coding)	2D
−5V to +5V (2's Complement Coding)	3D
0 to +5V (Binary Coding)	4A

AC8000 ORDERING GUIDE

Simply Specify ——— AC80[ ][ ]

For Resolution Of:	Enter
14 Bits	14
15 Bits	15
16 Bits	16

For Full Scale Range Of:	Enter
0 to +10V (Binary Coding)	1A
−10 to +10V (2's Complement Coding)	2D

ANALOGIC®

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Tel. (41) 1-810-0666 ■ Telex 845-59699
ANALOGIC LIMITED ■ 68 High Street ■ Weybridge, Surrey KT13 8BN ■ England
Tel. (44) 932-41251 ■ Telex 851-928030
ANALOGIC REGIONAL OFFICES ■
Cincinnati, Ohio (606) 371-0064 ■ San Jose, Calif. (408) 247-6401
Tustin, Calif. (714) 838-7243 ■ Garland, Texas (214) 681-0483
Houston, Texas (713) 777-6360

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Bulletin No. 16-0160 REV 0

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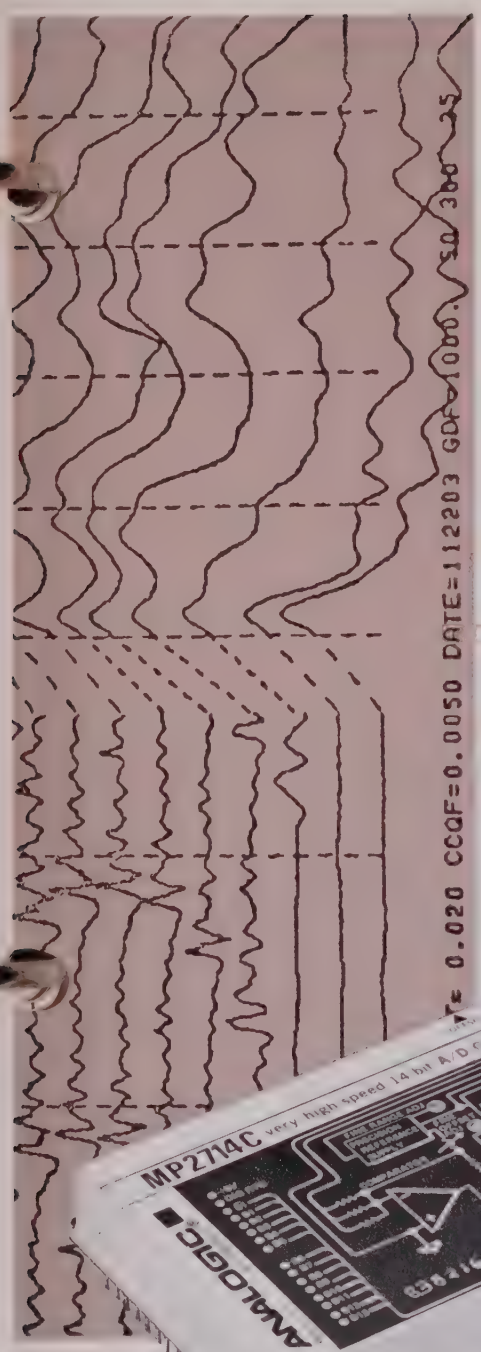
ACOUSTIC SYSTEMS

AUTOMATIC TEST

SPECTRAL ANALYSIS



2700 C Series 10, 12, 13 and 14-Bit A/D Converters

High Precision, Stability and Speed with Exceptional Linearity for Automatic Test, Spectral Analysis, Audio Digitizing, and Biomedical Systems.

ANALOGIC

...The Digitizers

2700C Series

A New Generation of Very High Speed A/D Converters Designed to Maintain Undegraded Accuracy, Linearity and Stability Over the Widest Possible Conditions.

USER ADVANTAGES

The 2700 Series successive approximation A/D converters offer new levels of accuracy, speed, and stability, and allow you to satisfy your overall design requirements for more functional, cost-effective data-acquisition systems. A close examination of the specifications will reveal that these converters have no cost/performance equal. Relative accuracies range from ±0.006% for 14 bits to ±0.05% for 10 bits, conversion times from less than 2.5μsec to 10μsec, and the differential linearity tempco of all four models of less than 4ppm/°C. In other words, you get true 10, 12, 13, and 14-bit performance even under worst-case conditions.

STABILITY

In thousands of installations, the 2700C Series has compiled an outstanding record of stability and accuracy. The "C" design exhibits very low noise, unusually low temperature coefficients and exceptional uniformity of code width.

These A/D converters provide built-in gain and offset adjustments and eliminate the need for external adjustments. In addition, the internal gain and offset adjustments are driven from a built-in precision reference supply rather than from external potentiometers driven by raw ±15V power supplies, as is commonly required by competitive units. In fact, total power supply sensitivity of these A/D converters is so low that the system engineer may select a less costly power supply.

SYSTEM-DESIGN FLEXIBILITY

- ☐ Four full-scale ranges provide a 4 to 1 sensitivity range. Choose the range best matched to the data system.
- ☐ Modupac™ construction provides electrostatic and electromagnetic shielding. Locate the A/D converter wherever needed.
- ☐ Each 2700 Series A/D converter shipped is computer tested to within guaranteed accuracy specifications, traceable to NBS Standards.

COMPATIBLE PRODUCTS

Many high speed analog-to-digital conversion applications require a sample and hold amplifier to relate the converted value to a point in relative time. The Analogic MP270 sample and hold complements the 2700 Series by its exceptionally low jitter, fast settling and high input impedance.

Other representative compatible products:

Multiplexers — MN4700, MP4100 Series; Power supplies — dc-dc converter MP3025 or Line-powered modules MP3315 for +5V @ 1A and MP33215 for ±15V @ 200mA.

SPECIFICATIONS

ANALOG INPUT
Input Voltage (Full Scale Range)
Input Impedance

ACCURACY (@23°C)
Absolute Accuracy (Traceable to NBS Standards)
Relative Accuracy
Differential Linearity
3 σ Noise(Includes Reference Noise)
Monotonicity

STABILITY
Tempco of Differential Linearity
Tempco of Gain
Tempco of Offset
Clock Stability
Power Supply Sensitivity
Recommended Recalibration Interval
Repeatability

CONVERSION TIME
Total Conversion

DIGITAL SIGNALS
Parallel Output (See Timing Diagram)
Serial Output (See Timing Diagram)
Coding
Trigger Input
Trigger Input Transition
End of Conversion, EOC
EOC Transition
Clock Output
Clock Output External Capacitance
Selectable Word Length

POWER SUPPLY
+15V ±3%
−15V ±3%
+ 5V ±5%

ENVIRONMENTAL, PHYSICAL, & RELIABILITY
Maximum Input Without Damage
Missing Codes
Warm-up Time to Stated Accuracy
Operating Temperature
Storage Temperature
Electrical Shielding
Packaging MP27xx
Packaging AN27xx

APPLIC

MP2710C	MP2712C	MP2713C	MP2714C
0 to +10V, ±5V, ±10V, or 0 to +5V 125Ω/volt of FSR	0 to +10V, ±5V, ±10V, or 0 to +5V 125Ω/volt of FSR	0 to +10V, ±5V, ±10V, or 0 to +5V 250Ω/volt of FSR	0 to +10V, ±5V, ±10V, or 0 to +5V 250Ω/volt of FSR
Calibrated to 0.05%. ±0.05% max. ±0.05% FSR. 0.01% FSR p-p, referred to input. Guaranteed.	Calibrated to 0.015%. ±0.012% max. **±0.012% FSR.** 0.01% FSR p-p, referred to input. Guaranteed.	Calibrated to 0.009%. ±0.006% max. ±0.006% FSR. 0.005% p-p, referred to input. Guaranteed.	Calibrated to 0.007%. ±0.006% max. ±0.006% FSR. 0.005% p-p, referred to input. Guaranteed.
< ±4PPM/°C FSR. < ±12PPM/°C. < ±17PPM/°C FSR. ±0.1%/°C. ±0.0012%/% change in supply voltage 6 months. Defined by Noise and Accuracy.	< ±3PPM/°C FSR. < ±10PPM/°C. < ±12PPM/°C FSR. ±0.1%/°C. ±0.0012%/% change in supply voltage. 6 months. Defined by Noise and Accuracy.	< ±3PPM/°C FSR. < ±10PPM/°C. < ±12PPM/°C FSR. ±0.1%/°C. ±0.0012%/% change in supply voltage. 6 months. Defined by Noise and Accuracy.	< ±3PPM/°C FSR. < ±8PPM/°C. < ±12PPM/°C FSR. ±0.1%/°C. ±0.0012%/% change in supply voltage. 6 months. Defined by Noise and Accuracy.
2.5μs.	4μs.	10μs.	10μs.
Binary $\overline{B1}$, B1 to B10. Standard TTL. 2 unit loads/line. Negative pulses simultaneous with clock pulse for "0". Max. load 30pF. Pin selectable. 3.5V ±1V pulse. See Timing Diagram. ≤200ns (90% to 10%). "1" to "0" level transition, nominally 100ns after LSB data pulse. TTL compatible, 9 loads. (See Timing Diagram). ≤20ns (10% to 90%). TTL compatible (See Timing Diagram). 30 pF maximum allowable. 2 to 10 bits (See Application Data).	Binary $\overline{B1}$, B1 to B12. Standard TTL. 2 unit loads/line. Negative pulses simultaneous with clock pulse for "0". Max. load 30pF. Pin selectable. 3.5V ±1V pulse. See Timing Diagram. ≤200ns (90% to 10%). "1" to "0" level transition, nominally 100ns after LSB data pulse. TTL compatible, 9 loads. (See Timing Diagram). ≤20ns (10% to 90%). TTL compatible (See Timing Diagram). 30 pF maximum allowable. 2 to 12 bits (See Application Data).	Binary B1, $\overline{B1}$ to B13. Standard TTL. 2 unit loads/line. Negative pulses simultaneous with clock pulse for "0". Max. load 30pF. Pin selectable. 3.5V ±1V pulse. See Timing Diagram. ≤200ns (90% to 10%). "1" to "0" level transition, nominally 100ns after LSB data pulse. TTL compatible, 9 loads. (See Timing Diagram). ≤20ns (10% to 90%). TTL compatible (See Timing Diagram). 30 pF maximum allowable. 2 to 13 bits (See Application Data).	Binary $\overline{B1}$, B1 to B14. Standard TTL. 2 unit loads/line. Negative pulses simultaneous with clock pulse for "0". Max. load 30pF. Pin selectable. 3.5V ±1V pulse. See Timing Diagram. ≤200ns (90% to 10%). "1" to "0" level transition, nominally 100ns after LSB data pulse. TTL compatible, 9 loads. (See Timing Diagram). ≤20ns (10% to 90%). TTL compatible (See Timing Diagram). 30 pF maximum allowable. 2 to 14 bits (See Application Data).
60mA. 60mA. 300mA.	60mA. 60mA. 300mA.	60mA. 60mA. 300mA.	60mA. 60mA. 300mA.
±200% of Full Scale Range. None. <5 minutes. 0°C to +60°C. −25°C to +85°C. RFI 6 sides; EMI 5 sides. 2"x 4"x 0.44" Metal Case Dimensions in mm: 51mm x 102mm x 11.3mm. MP27xx on plug-in PC card.	±200% of Full Scale Range. None. <5 minutes. 0°C to +60°C. −25°C to +85°C. RFI 6 sides; EMI 5 sides. 2"x 4"x 0.44" Metal Case Dimensions in mm: 51mm x 102mm x 11.3mm. MP27xx on plug-in PC card.	±200% of Full Scale Range. None. <5 minutes. 0°C to +60°C. −25°C to +85°C. RFI 6 sides; EMI 5 sides. 2"x 4"x 0.44" Metal Case Dimensions in mm: 51mm x 102mm x 11.3mm. MP27xx on plug-in PC card.	±200% of Full Scale Range. None. <5 minutes. 0°C to +60°C. −25°C to +85°C. RFI 6 sides; EMI 5 sides. 2"x 4"x 0.44" Metal Case Dimensions in mm: 51mm x 102mm x 11.3mm. MP27xx on plug-in PC card.

☐ High speed computer interfacing ☐ Wide band data digitizing ☐ Multi-channel process control ☐ Audio digitizing
☐ Mass spectroscopy ☐ Biomedical instrumentation ☐ Seismic array digitizing ☐ Telemetry

PERFORMANCE ACHIEVEMENTS

The high digitizing rates of 400,000 to 100,000 conversions per second (with accuracies and differential linearities to 0.006%) of the MP2710C, MP2712C, MP2713C, and MP2714C are achieved by incorporating a unique comparator. Implementing this and similar techniques with the optimum components available assures that these converters offer the highest accuracy and linearity consistent with their rated resolution and high speed conversion.

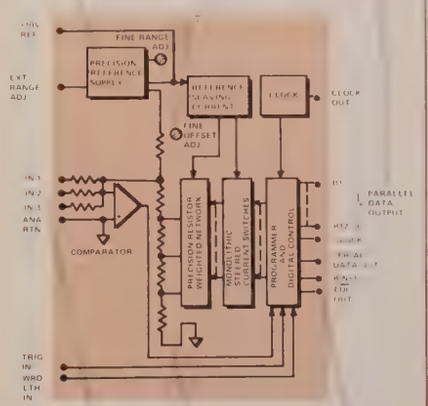
The major determinant of monotonicity over temperature is the tempco of differential linearity. For example, with a 30°C rise, the worst-case shift in differential linearity is less than 120 ppm or ½ LSB for a 12-bit word, thus preserving each individual code over this temperature range.

Combining the MP2712C with Analogic's 47XX Series Multiplexers and MP270 Sample and Hold module can provide a total data acquisition system throughput up to 200,000 per second. This very high throughput capability offers economical solutions to the valid conversion of high-spectral-content signals. Alternatively, one MP2712C will process three times as many channels of valid data, at the same speed and at the same cost, as similar modular A/D converters on the market today.

Zener controlled Reference Power Supply
- Assured accuracy and stability

Built in Range & Offset potentiometers
- Controlled stability

DTL/TTL Compatible
- Full system interfacing

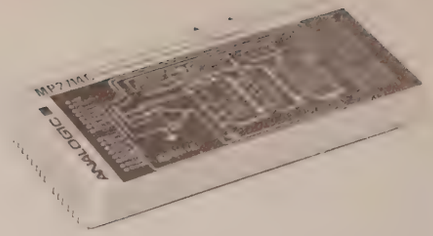


Bipolar or Unipolar Input voltages
- Pin selectable

4μs total conversion
- Up to 250 kHz thru-put

EOC after conversion
- Convenient system applications

Figure 1. MP2712C Functional Block Diagram



UNIQUE DESIGN FEATURES OF 2700C SERIES

Unique Modupac ™ construction — 5-sided electro-magnetic shielding, 6-sided electrostatic shielding for immunity to RFI and EMI — factory serviceability.

☐ Built-in range and offset adjustments — integrally packaged. The user saves cost of potentiometers and installation; controls are optimally selected by Analogic; units are calibrated prior to shipment; and absolute accuracy is guaranteed as specified.

Fully buffered outputs — vital at high conversion speeds to isolate digital programmer from load capacity.

Operating range selected (from 4 available) by "jumpering" pins — covers all standard signal input ranges.

Accuracy and stability unmatched for the price — relative accuracy of 0.006%; differential linearity less than 3ppm/°C — guarantees full performance to user expectations over widest possible temperature range. You can design with confidence.

Lowest power dissipation, consistent with extremely low noise and high speeds, yields low thermal rises; further minimized by low temperature coefficients.

ORDERING GUIDE

Simply Specify

Configuration	
For	*Enter*
Modupac ™	**MP27**
Card-Mounted Modupac ™	**AN27**

For Resolution of:	*Enter*
10 Bits	**10C**
12 Bits	**12C**
13 Bits	**13C**
14 Bits	**14C**

For Full Scale Range of:*	*Enter*
0 to +10V	1
−10V to +10V	2
− 5V to +5V	3
− 0 to +5V	4

For Output Code of;*	*Enter*
Offset Binary or Binary	**A**
1's Complement	**C**
2's Complement	**D**

*Applicable to AN27XX only. Card-mounted Modupacs are supplied with input range jumper.

ACTION REQUEST

My product interest is
- ☐ Model MP2710C
- ☐ Model MP2712C
- ☐ Model MP2713C
- ☐ Model MP2714C
- ☐ Card Mounted AN27___

I am interested in A/D converters with substantially different characteristics:
- ☐ more resolution
- ☐ less resolution
- ☐ higher speed
- ☐ lower speed
- ☐ still higher stability
- ☐ lower stability — lower cost
- ☐ other

Related Products — I am interested in the following products:
- ☐ Multiplexers
- ☐ Sample & Hold Amplifiers
- ☐ Modular Power Supplies
- ☐ DC/DC Converters
- ☐ Total Systems (please describe):

Other Products:

Technical Assistance
☐ Please have a senior applications engineer call to discuss:

☐ Please quote the following products/quantity:

Model No.	1-9	10-24	25-49	50-99	100 +
MP2710C					
MP2712C					
MP2713C					
MP2714C					
Card—Mounted Version					

My requirement is:
☐ Immediate ☐ 3-6 months ☐ For reference

NAME
TITLE
COMPANY
ADDRESS
CITY
STATE ZIP
PHONE ( ) Ext.

Please fold and staple before mailing.

A CASE FOR THE 2700C SERIES

Analogic's Applications Staff is pleased to provide the information you need.

Please check off the appropriate boxes on the other side of this reply card to receive information or technical assistance on conversion system design and the interpretation of A/D/A converter specifications.

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SET-UP

Input Voltage Range Selection

Three input pins are provided to allow user selection of one of four standard input voltage ranges. "IN 1", "IN 2", and "IN 3" must be connected in accordance with the following tables and illustrations to select the desired full-scale range.

Output Word Length Selection

The number of bits in the output word is pin selectable. To operate the ADC at its full capacity, B (N + 1) must be connected to WRD LTH IN. This connection is factory installed on the PC card for all AN versions ordered and must be removed when operating at less than its full digital output capacity. To operate the converter at less than its full digital output capacity, WRD LTH IN must be connected only to the terminal identified as one bit more than the desired number of bits out. EXAMPLE: When the ADC is operated as an 8-bit converter, connect WRD LTH IN to B9 only. Refer to the accompanying chart for the binary output coding.

CALIBRATION

Zero Offset Calibration

To recalibrate the OFFSET:

1. Apply input voltage shown in accompanying table and,
2. Adjust the OFFSET control so that the LSB of the output code 100...00/1 for bipolar units and 00...00/1 for unipolar units alternates equally between "1" and "0". Offset should be readjusted whenever the selected full scale range is changed.

Zero offset should be calibrated before recalibrating RANGE.

Range Calibration

Internal: A built-in 0.1% adjustment of the full scale voltage is provided. To recalibrate the RANGE:

1. Apply input voltage shown in the accompanying table and,
2. Adjust the RANGE control so that the LSB of the output code, 111...110/1 (B1,...B(N)), alternates equally between "1" and "0". RANGE should be readjusted whenever the selected full scale range is changed.

External Connection

A wider range adjustment may be implemented by connecting a 20kΩ potentiometer between "+10V REF" and "ANA RTN"; and connecting a resistor, R, between the wiper arm of the 20kΩ potentiometer and "RANGE ADJ". The adjustment range will be +5% to −0.3% for R = 470kΩ and +5% to −2.8% for R = 47kΩ. This latter value permits the calibration of a unit to be set for the so-called binary adjusted scale factors of 10.24V or 5.12V.

TYPICAL APPLICATION

An MP2712 Analog-to-Digital Converter is shown connected to a high speed-high resolution multiplexed data conversion subsystem. The subsystem provides 12-bit data conversion at thru-put rates up to 200,000 conversions per second.

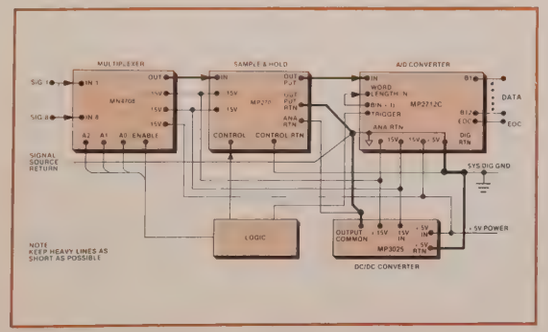

Figure 3. Typical Application of MP2712C A/D Converter

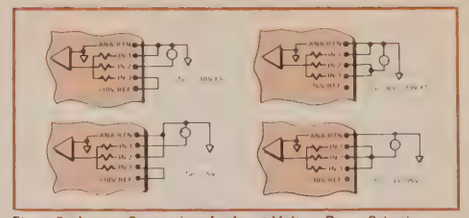

Figure 2. Jumper Connections for Input Voltage Range Selection

INPUT RANGE CONNECTION TABLE			
Nominal Full Scale Range	MP2710C, MP2712C, MP2713C, MP2714C		
	IN 1	IN 2	IN 3
10V to +10V	to ANA RTN	to ANA INPUT	to +10V REF
0V to +10V	to ANA RTN	to ANA INPUT	to ANA INPUT
5V to +5V	to ANA INPUT	to ANA RTN	to +10V REF
0V to +5V	to ANA INPUT	to ANA INPUT	to ANA INPUT
Nominal Full Scale Range	AN2710C, AN2712C, AN2713C, AN2714C Terminals on Card		
−10V to +10V	E29 to E28	E30 to E35	E31 to E32
0V to +10V	E29 to E28	E30 to E35	E33 to E34
−5V to +5V	E36 to E35	E30 to E28	E31 to E32
0V to +5V	E29 to E28	E30 to E35	E34 to E33

	INPUT VOLTAGES FOR CALIBRATION			
	MP2710C/AN2710C For		MP2712C/AN2712C For	
Nominal Full Scale Range	Zero Cal.	Range Cal.	Zero Cal.	Range Cal.
−10V to +10V	+0.0098V	+9.9707V	+0.0024V	+9.9927V
0 to +10V	+0.0049V	+9.9854V	+0.0012V	+9.9963V
−5V to +5V	+0.0049V	+4.9854V	+0.0012V	+4.9963V
0 to +5V	+0.0024V	+4.9927V	+0.0006V	+4.9982V
	MP2713C/AN2713C For		MP2714C/AN2714C For	
Nominal Full Scale Range	Zero Cal.	Range Cal.	Zero Cal.	Range Cal.
−10V to +10V	+0.0012V	+9.9963V	+0.00061V	+9.9982V
0 to +10V	+0.0006V	+9.9982V	+0.00031V	+9.9991V
−5V to +5V	+0.0006V	+4.9982V	+0.00031V	+4.9991V
0 to +5V	+0.0003V	+4.9991V	+0.00015V	+4.9995V

BINARY OUTPUT CODING	
10 BIT RESOLUTION	12 BIT RESOLUTION
Unipolar binary:	Unipolar binary:
+9.9951V = 1 111 111 111	+9.9976V = 111 111 111 111
0.0000V = 0 000 000 000	0.0000V = 000 000 000 000
Pin Label = B1, B2 . . . B10	Pin Label = B1, B2 . . . . B12
Two's complement**:	Two's complement**:
+9.9902V = 0 111 111 111	+9.9951V = 011 111 111 111
0.0000V = 0 000 000 000	0.0000V = 000 000 000 000
-10.0000V = 1 000 000 000	-10.0000V = 100 000 000 000
Pin Label = $\overline{B1}$, B2 . . . B10	Pin Label = $\overline{B1}$, B2 . . . . B12
13 BIT RESOLUTION	14 BIT RESOLUTION
Unipolar binary:	Unipolar binary:
+9.9988V = 1 111 111 111 111	+9.9994V = 11 111 111 111 111
0.0000V = 0 000 000 000 000	0.0000V = 00 000 000 000 000
Pin Label = B1, B2 . . . . . B13	Pin Label = B1, B2 B14
Two's complement**:	Two's complement**:
+9.9976V = 0 111 111 111 111	+9.9988V = 01 111 111 111 111
0.0000V = 0 000 000 000 000	0.0000V = 00 000 000 000 000
-10.0000V = 1 000 000 000 000	-10.0000V = 10 000 000 000 000
Pin Label = $\overline{B1}$, B2 . . . . . B13	Pin Label = $\overline{B1}$, B2 B14

**To change to offset binary, use B1 instead of $\overline{B1}$. For 5-volt units, divide input voltage by 2.

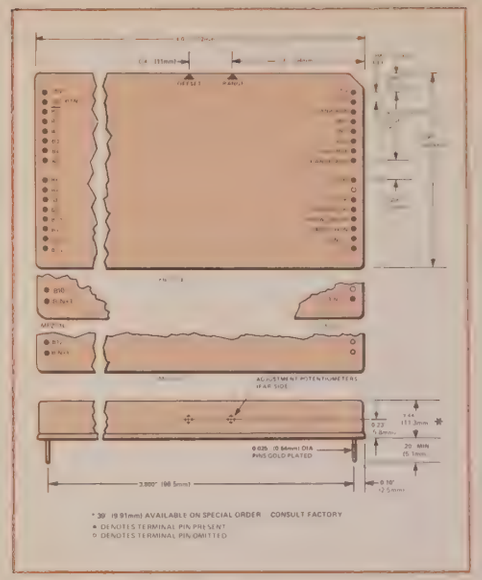
ADJUSTMENT POTENTIOMETERS (REAR SIDE)
* .39" (9.91mm) AVAILABLE ON SPECIAL ORDER CONSULT FACTORY
• DENOTES TERMINAL PIN PRESENT
○ DENOTES TERMINAL PIN OMITTED

Figure 5. Modupac Outline Drawing

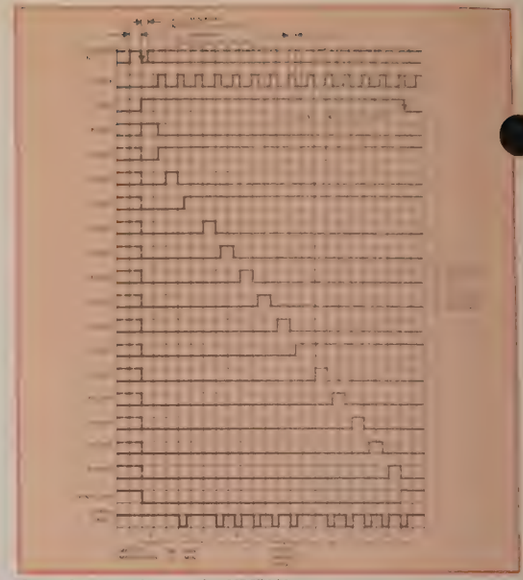

Figure 6. Timing Diagram for MP2714C

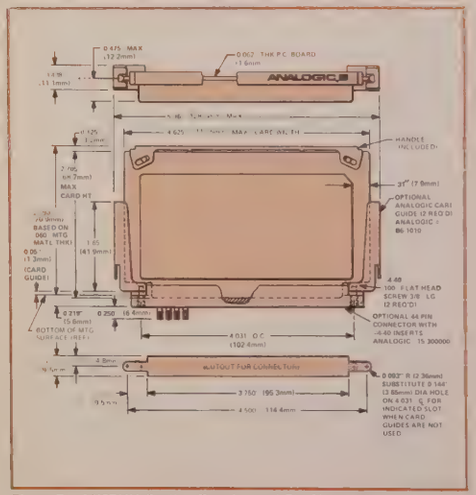
ANALOGIC
HANDLE (INCLUDED)
OPTIONAL ANALOGIC CARD GUIDE (2 REQ'D) ANALOGIC # 86-1010
CARD GUIDE
OPTIONAL 44 PIN CONNECTOR WITH 4-40 INSERTS ANALOGIC # 300000
BOTTOM OF MTG SURFACE (REF)
CUTOUT FOR CONNECTOR

Figure 7. AN27XX Outline Drawing and Pin Nomenclature

PC CARD PIN DESIGNATIONS

TRIGGER IN	A	1	EOC
	B	2	
WRD LTH IN	C	3	B(N+1)* (B13)**†
	D	4	
B2 OUT	E	5	B1 OUT
B4 OUT	F	6	B3 OUT
B12 OUT	H	7	B6 OUT
B5 OUT	J	8	B8 OUT
B7 OUT	K	9	
CLOCK	L	10	SERIAL DATA
+5V	M	11	+5V
DIG RTN	N	12	DIG RTN
B(N+1)†† B11 OUT	P	13	B10 OUT
$\overline{B1}$	R	14	B9 OUT
SIG RTN	S	15	ANA RTN
INPUT	T	16	INPUT
	U	17	B(N+1)†
(B14)† B(N+1)**	V	18	
ANA RTN	W	19	ANA RTN
−15V	X	20	−15V
+15V	Y	21	+15V
+10V REF OUT	Z	22	

†For AN2714C
††For AN2710C
*For AN2712C
**For AN2713C

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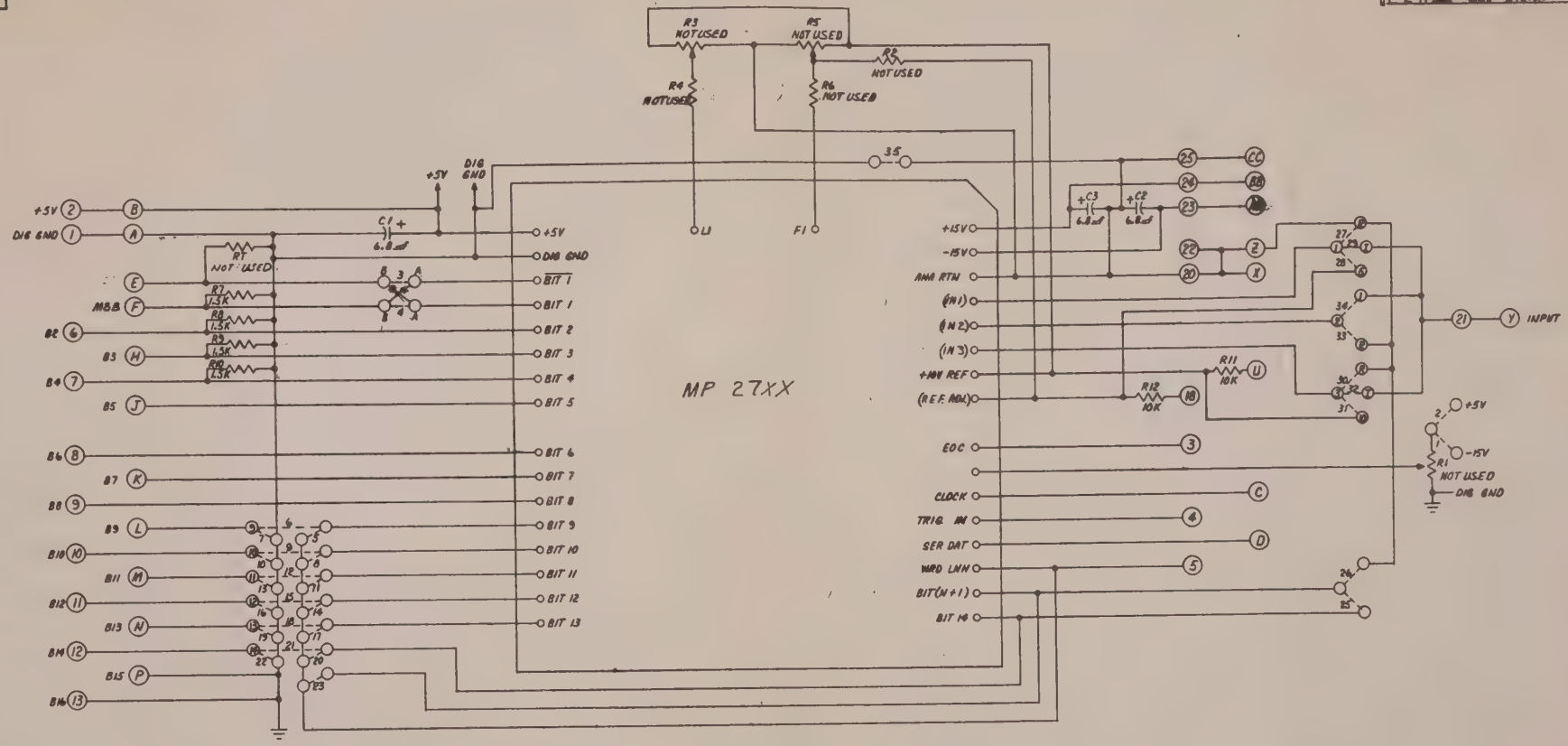
REV	ECO	DESCRIPTION	DWN	APPVD	DATE
1	—	ENG RELEASE	RR	—	7-8-76
1A	4-582	SEE E.C.O.	DP	[illegible]	8-17-76
2	4-643	SEE E.C.O.	DP	L.M.	1-28-80



RESOLUTION	JUMPER E
14 BITS	23, 21, 18, 15, 12, 9, 6
13 BITS	20, 22, 18, 15, 12, 9, 6
12 BITS	11, 22, 19, 15, 12, 9, 6
11 BITS	14, 22, 19, 16, 12, 9, 6
10 BITS	11, 22, 19, 16, 13, 9, 6
9 BITS	8, 22, 19, 16, 13, 10, 6
8 BITS	5, 22, 19, 16, 13, 10, 7

RANGE	JUMPER E
-10 TO +10V	27, 34, 31
0 TO +10V	27, 34, 32
-5 TO +5V	29, 33, 31
0 TO +5V	29, 34, 32

CODING	JUMPER
BINARY	3 & 4 CUT ETCH A:B 2 PLACES
2'S COMPLEMENT	NONE

LIST OF MATERIAL

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

PL10-7441	AC2XXX
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

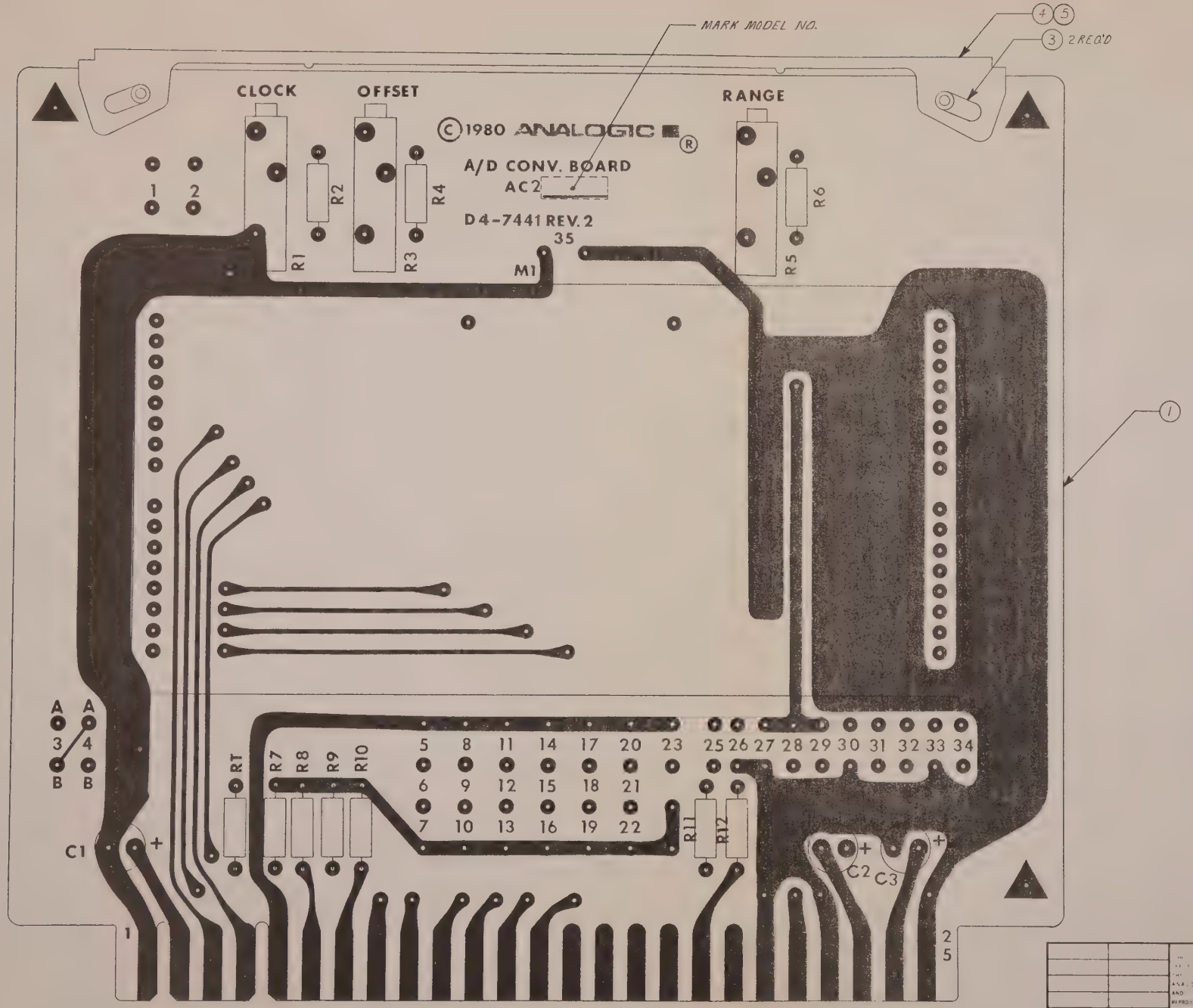
APPLICABLE SPECIFICATIONS

DRAWN	R. Rees	8-12-76
CHECKED	[illegible]	8-14-76
DESIGNER	[illegible]	8-14-76
ENGINEER	H. WEEDON	8-16-76
APPROVED	[illegible]	8-17-76
RELEASED	[illegible]	8/19/76
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC
MOTHER BD. FOR MP27XX
AC27XX

ORDER ENTRY NO. 31814	SIZE D	5-7441	REV 2
SCALE —	ACCOUNT NO. —	SHEET 1 OF 1	



REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
2	9565	SEE ECO	DP	M	2580

D 7-7441 REV 2

NOTES:
1. FOR SCHEMATIC SEE D5-7441.
2. ASSEMBLE PER A2-1027.

COMPONENT SIDE

		DRAWN	D. MULREY	DATE 12-4-75
		CHECKED	R.F. BRY	3/4/76
		DESIGNER	K.W. Hynes	8-17-76
		ENGINEER	E. DINOWITZ	8-19-76
		APPROVED		
		RELEASED	R. FRANE	8-17-76
		WEIGHT		
PL10-7441	AC 2XXX			
NEXT ASSY	USED ON			
APPLICATION				

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ASSEMBLY
A/D CONV. MOTHER BOARD
AC 2XXX

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SCALE 4:1	ACCOUNT NO		SHEET 1 OF 1

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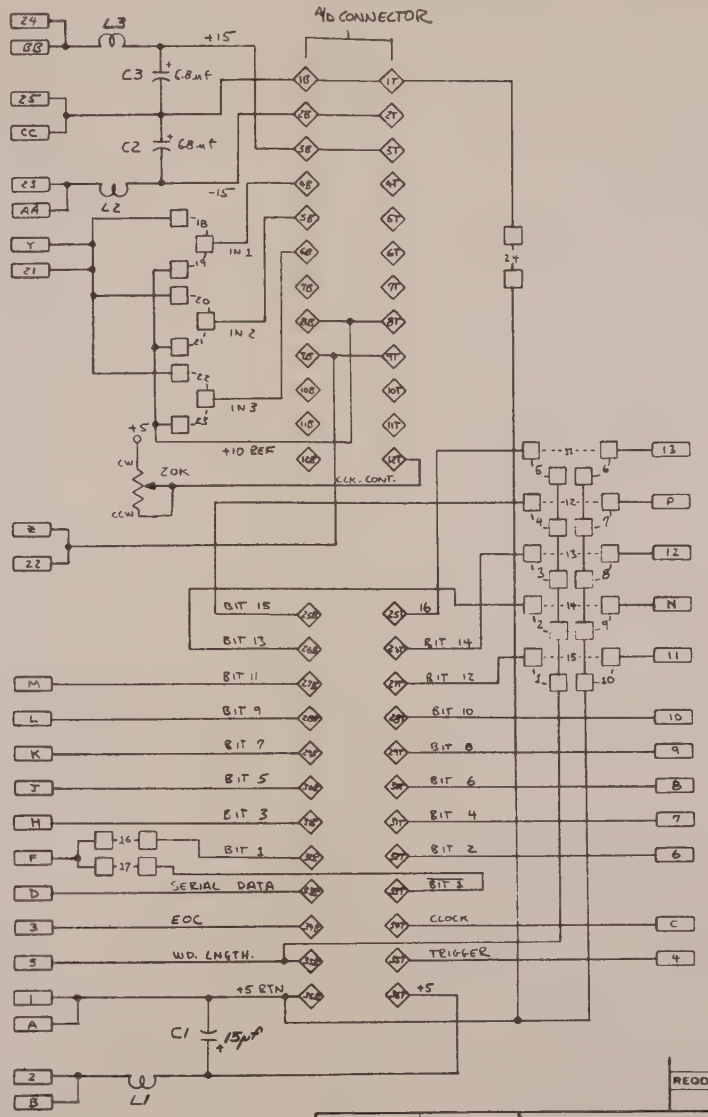
SIZE C 5-7442 REV 1



VOLTAGE RANGE	JUMPERS
±10	17, 20, 23
0-10	16, 20, 22

RESOLUTION	JUMPERS
12 BIT	15, 1, 9, 8, 7, 6
13 BIT	2, 15, 14, 8, 7, 6
14 BIT	3, 15, 14, 13, 7, 6
15 BIT	4, 15, 14, 13, 12, 6
16 BIT	5, 15, 14, 13, 12, 11

ANALOG TO DIGITAL GND. — JUMP 24

LIST OF MATERIAL

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

RIO-7442	AC 8XXX
NEXT ASSY	USED ON
APPLICATION	

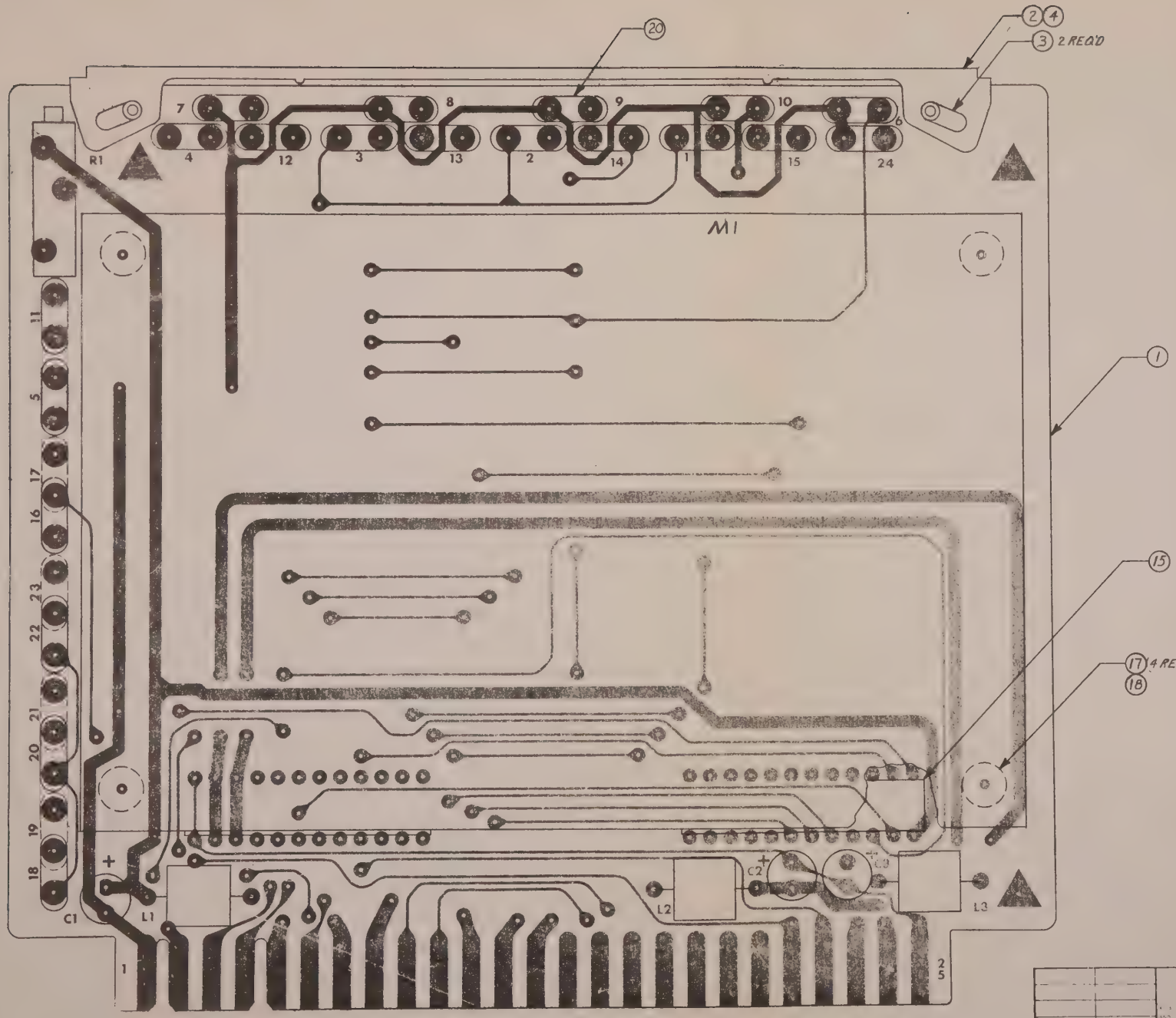
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	RWH	11-8-76
CHECKED		14 DEC 76
DESIGNER	RWH	12-19-76
ENGINEER	RWH	12-19-76
APPROVED		14 DEC 76
RELEASED		12/14/76
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

AC 8XXX, A/D MOTHER BOARD

CODE IDENT NO	SIZE		REV
31814	C	5-7442	1
SCALE NONE	ACCOUNT NO		SHEET 1 OF 1



REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPL'S	DATE
1	4567	SEE E.C.O.	RG	DP	L.M. 1-27-77

D 7-7442 1

NOTES:
1. FOR SCHEMATIC SEE C5-7442.
2. ASSEMBLE PER A2-1027.

COMPONENT SIDE

PL10-7442	AC 8XXX	R. FRENTISS	6-12-76	ANALOGIC MAKER ELD MASS 01880
NEXT ASSY	LSI ITEM	R. PERRY	12-14-76	ASSEMBLY
APPLICATION		R.W. HAVENER	12-14-76	A/D MOTHER BOARD
		R.W. HAVENER	12-14-76	AC 8XXX
		R.F. POWELL	12-14-76	
		R. PEAKE	12-14-76	
				CODE IDENT NO 31814 · SIZE D · 7-7442 · REV 1
				SCALE 4:1 · ACCOUNT NO · SHEET 1 OF 1

7.6 Front Panel Display and Control

7.6.0 General

The ANDS5400 front panel consists of two PC boards mounted directly behind the front display panel of the system. The larger board, the display panel (see schematic D5-8663 in this section), contains the LED displays, local control pushbuttons, and timing logic; the smaller board, the address board (see schematic D5-8662), has the address register and decoding circuitry, digiswitch buffers, and data display multiplexer/registers.

The display panel is discussed first, and the addressing system is described in detail in sections 7.6.23 through 7.6.29.9.

7.6.1 Connector J84

The following signal list contains all of the signals going to and coming from the front panel through connector J84, which goes to the internal backplane.

INT = Interface
SP = Signal Processor
J28 = J28 Connector On Rear Panel Of System
ADC = A/D Converter
ADD = Address Board
UC = User Card Backplane
PS = Power Supply

Signal Name	Conn.	To	From	Function
$\overline{\text{CLR2}}$	J84-1	UC		Clear 2, General Clearing Pulse
DIG STROBE	J84-2	UC		Digital Strobe, Loads Data Into UC
DIG IN	J84-3	INT		Dig Bus "In" Mode Sig For Interface
RDY TO HOLD	J84-4	J28		Synchronizes External SSH Transactions
RMT	J84-5	INT		High When In "Remote"
RDUSR	J84-6	UC		Dig Bus "In" Mode Sig For User Cards
REQ OUT	J84-7		UC	Indicates UC Interrupt Request
SSH	J84-8	INT		Indicates Ext SSH Completion
RUN	J84-9		INT	High To Lock Out Front Panel Controls
$\overline{\text{HOLD}}$	J84-10		J28	External SSH "Hold" Command
$\overline{\text{SE}}$	J84-11	SP		Low In Single-ended Modes
MSR1	J84-12	SP		Starts A/D Conversion
M2	J84-13	SP		Signal Processor Gain Determining Bit
$\overline{\text{M1}}$	J84-14	SP		Signal Processor Gain Determining Bit
$\overline{\text{GA}}$	J84-15	SP		Special Mode Bit For Some Signal Proc
+5	J84-16		PS	
M3	J84-17	SP		Signal Processor Gain Determining Bit
$\overline{+5}$	J84-18		PS	
$\overline{\text{CLR1}}$	J84-19		INT	Clear 1, Clears SSH Status
+5	J84-20		PS	
DIG OUT	J84-21		INT	Strobes Data Into User Card Registers
+5	J84-22		PS	
OUT	J84-23		INT	Puts Digital Bus In "Out" Mode
+5	J84-24		PS	
IN	J84-25		INT	Puts Digital Bus In "In" Mode
DIG GND	J84-26		PS	
D/A	J84-27		INT	Puts Address Decoding In "D/A" Mode
DIG GND	J84-28		PS	
A/D	J84-29		INT	Puts Address Decoding In "A/D" Mode
DIG GND	J84-30		PS	
MSR	J84-31		INT	Requests A/D Conversion
DIG GND	J84-32		PS	
RS	J84-33		INT	Range Strobe, Loads Range Register
$\overline{\text{DIG GND}}$	J84-34		PS	
$\overline{\text{CLR}}$	J84-35		INT	Clear, General Clearing Pulse
DIG GND	J84-36		PS	
INCRM	J84-37		INT	Increments Address Register
DIG GND	J84-38		PS	
LMAR	J84-39		INT	Loads Multiplexer Address Register
DIG GND	J84-40		PS	

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7.6.2 Connector J83

Connector J83, listed below, carries information between the two front panel boards.

Signal Name	Conn.	To	From	Function
AR9	J83-1		ADD	Address Register Bit 9
AR7	J83-2		ADD	Address Register Bit 7
AR10	J83-3		ADD	Address Register Bit 10
AR8	J83-4		ADD	Address Register Bit 8
AR12	J83-5		ADD	Address Register Bit 12 (LSB)
AR6	J83-6		ADD	Address Register Bit 6
AR11	J83-7		ADD	Address Register Bit 2
AR5	J83-8		ADD	Address Register Bit 5
RR1	J83-9		ADD	Range Register Bit 1 (MSB)
AR3	J83-10		ADD	Address Register Bit 3
RR2	J83-11		ADD	Range Register Bit 2
AR4	J83-12		ADD	Address Register Bit 4
RR4	J83-13		ADD	Range Register Bit 4 (LSB)
AR2	J83-14		ADD	Address Register Bit 2
RR3	J83-15		ADD	Range Register Bit 3
$\overline{\text{AR1}}$	J83-16		ADD	Address Register Bit 1 (MSB)
ERA	J83-17	ADD		Enable Range & Address Reg Readback
$\overline{\text{BB5}}$	J83-18		ADD	Address Board Bus Bit 5
EDIG	J83-19	ADD		Enable Digiswitch Readback
BB6	J83-20		ADD	Address Board Bus Bit 6
DIG IN	J83-21	ADD		Digital Input Mode
BLAD	J83-22		ADD	Blank Data Display
DA	J83-23	ADD		D/A Address Decoding
DL15	J83-24		ADD	Data Lites Bit 15
DL14	J83-25		ADD	Data Lites Bit 14
DL4	J83-26		ADD	Data Lites Bit 4
DL16	J83-27		ADD	Data Lites Bit 16 (LSB)
DL13	J83-28		ADD	Data Lites Bit 13
DL1	J83-29		ADD	Data Lites Bit 1 (MSB)
DL3	J83-30		ADD	Data Lites Bit 3
DL2	J83-31		ADD	Data Lites Bit 2
DL9	J83-32		ADD	Data Lites Bit 9
DL7	J83-33		ADD	Data Lites Bit 7
DL5	J83-34		ADD	Data Lites Bit 5
DL11	J83-35		ADD	Data Lites Bit 11
DL10	J83-36		ADD	Data Lites Bit 10
DL8	J83-37		ADD	Data Lites Bit 8
DL12	J83-38		ADD	Data Lites Bit 12
DL6	J83-39		ADD	Data Lites Bit 6
+5	J83-40		PS	
DADD	J83-41	ADD		Dynamic Address Mode
+5	J83-42		PS	
LRAN	J83-43	ADD		Load Range Register
+5	J83-44		PS	
CLR2	J83-45	ADD		Clears Range And Address Registers
DIG GND	J83-46		PS	
IADD	J83-47	ADD		Increments Address Register
DIG GND	J83-48		PS	
LADD	J83-49	ADD		Load Address Register
DIG GND	J83-50		PS	

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7.6.3 Logic Elements

The logic elements on the front panel are a combination of low power Schottky and CMOS technologies. Schottky is used for speed in all the key registers and decision making paths to allow for high speed computer communication; CMOS is used to save power in non-critical areas or to meet the interfacing requirements of the CMOS user card bus.

7.6.4 Interface Signal Blocking in "Local" Control

During "local" control the front panel does not attempt to block the signals coming from the interface; the interface has circuitry that puts all of the signals going to the front panel into a known state during "local" control, and the RMT signal from the front panel causes the interface to block its own signals. The normal levels of the lines from the interface during "local" control are listed below:

Signal	"LOCAL" State
RUN	Indeterminate (Set By Computer)
$\overline{\text{CLR}}$	High
$\overline{\text{CLR1}}$	High
INCRM	Low
LMAR	Low
MSR	Low
A/D	Low
D/A	Low
OUT	High
IN	High
DIG OUT	Low
RS	Low

7.6.5 Local/Remote Selection

IC Z11 and its associated components control the "local/remote" status of the front panel. When the Q output of Z11 is high, the panel is in the "local" mode of operation, where the front panel buttons perform their prescribed functions and the computer commands are locked out. When the Q output is low, the front panel is in the "remote" mode, where the front panel buttons are ignored and the computer commands from the interface control the system. C6 and R11 hold the clear input of Z11 low during power-up to ensure that the system warms up in the "remote" mode, thus allowing automatic computer control when the system is started. If the computer sets the "RUN" bit high in the status register of the interface, the D input of Z11 will be low, thus preventing "local" operation under any circumstances. If the "RUN" bit is not high, then the operator may put the system in "local" control by momentarily pushing the SELECT button, which will send the stored charge on C12 into the clock input of Z11 as a positive pulse. Continued pushing of the SELECT button will cause Z11 to alternate between "local" and "remote" because of the feedback into the D input through pin 5 of Z12. The RM pulse caused by pushing the SELECT button also puts the system in the "out" mode to allow loading of the range and address registers. The "local/remote" status of the front panel is sent to the interface through the RMT signal on J84-5. The status is also shown by the two LED indicators driven by two sections of Z22. Since one of the two lites must be on at all times, they also serve as power-on indicators.

7.6.6 A/D or D/A Mode Selection

The other half of Z11 controls the address decoding mode of the system. When Z11 pin 9 (Q output) is high, the D/A decoding mode is selected; when it is low, the A/D decoding mode is selected. The ANALOG MODE (A/D decoding) and DIGITAL MODE (D/A decoding, or digital input, or digital output) pushbuttons have a 5 volt level applied to them only when the panel is in "local" control; thus, they are disabled during the "remote" mode. During the "local" mode the A/D and D/A signals from the interface are both low, allowing alternate pushing of the ANALOG MODE and DIGITAL MODE buttons to force the state of Z11 through the clear and preset inputs. The D/A signal on J83-23 goes to the address board to choose the decoding mode. During "remote" control the A/D and D/A signals from the interface set Z11 to choose the decoding mode.

7.6.7 User Card Interrupt Requests

The REQUEST LED (DS1), illuminated whenever the REQ OUT line from the user card backplane is high, indicates that a user card is requesting interrupt service.

7.6.8 Address Register Loading

IC Z8 pin 12 will have a negative pulse on it whenever the ANALOG MODE or DIGITAL MODE button is released during "local" control. The trailing edge of this pulse will trigger the other half of Z8, generating LADD on J83-49, which loads the address register. Thus, momentarily pushing either button during "local" control will load the address register and select the appropriate decoding mode at the same time. During "remote" control LMAR signals from the interface cause LADD pulses, loading the address register. Z8 is triggered when pin 9 goes low (i.e. when the buttons are pushed "in"), but R7 and C4, the timing components, are tied to this pin so that the IC cannot complete its pulse until the buttons are released. This technique eliminates the effects of a switch bounce that could create spurious LADD pulses that might interfere with the reading back of the address register.

7.6.9 Range Register Loading

Z16-5 will have a positive pulse on it whenever the ANALOG MODE button is pushed, loading the range register through LRAN on J83-43. RS (range strobe) pulses from the interface activate LRAN through Z18-5 during "remote" control. As a result the ANALOG MODE button loads both the address and range registers.

7.6.10 Address and Range Register Readback

Due to the delay added by the first part of Z8 in the process of loading the address register, the selection of the decoding mode (A/D or D/A) will always occur before the loading of the address register during "local" control. The same relationship is also true during "remote" control because it is the trailing edge of the LMAR pulse from the interface that triggers Z8-13, thus adding a short delay.

This timing relationship allows us to use Z3-6, Z10-6, and the generation of the ERA signal on J83-17 to read back the information in the range and address registers. In "local" or "remote" control a digital input cycle with an address of 2000 should result in reading the information stored in the range and address registers. Normally, any digital input cycle will cause the address requested to be loaded into the address register, but in the case where the address is 2000 we want to read the last address stored in the register, not the new address. If we loaded the address first and then enabled the readback,

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we would read 2000 every time! Z3-6, which is normally high, goes low only when BB6 is high, BB5 is low, and we are in the D/A mode. The two BB signals come from the address board and correspond to information that is about to be loaded into the address register. BB5 corresponds to the MSB of the address and is adjacent to BB6. Thus, the decoding conditions are met with an address of 2000 (they are actually met with any address between 2000 and 3777, as long as the MSB bit is off and the next MSB is on). When these conditions are met, Z3-6 goes low and blocks LADD through Z9-12 before it is created. When Z8 is triggered, the pulse on Z8-4 clocks a zero into Z10, making Z10-6 go high, thus creating ERA (enabling the range and address readback) which, if we are doing a digital input transaction, puts the range and address information on the system digital bus. The first address loaded that does not meet all of these conditions will cause Z10-6 to go back down. Note that LADD pulses are also prevented if digital outputs are attempted on addresses between 2000 and 3777. However, this is of no concern since there are no active digital output channels in this address range in any system.

7.6.11 Address Register Incrementing

The two halves of Z1 create the pulses that increment the address register. Incrementing is not a feature of the front panel controls, so this IC is used only in "remote." The INCRM signal from the interface is a positive going pulse that goes right through Z6 to make a negative pulse on J83-47 (IADD), incrementing the address register. If we are in the A/D decoding mode (AD is high) and the range register contains a differential range code ($\overline{SE}$ is high), then Z1 is enabled and will trigger at the falling edge of INCRM. The trailing edge of the resulting pulse from Z1-4 will trigger the other half of Z1 provided that AR12 is high. The final pulse from Z1-5 will create a second IADD pulse that will increment the address register again.

The net result is that the address register will be incremented at least once for every INCRM pulse received and will be incremented twice if we are scanning differential A/D channels. All differential A/D channels have even addresses, so the inclusion of AR12 prevents the scanning of odd channels. If the first channel is odd, the register will increment only once to the next even channel and will thenceforth skip over the odd channels. The incrementing function is useful only in certain system configurations. Many interfaces do not provide incrementing capability at all, and those that do must be used with analog input cards that have 32 single-ended channels or 16 differential channels per card or digital cards with 4 channels to make the most of the feature. Incrementing is most useful if the user must scan hundreds of successive high-level channels, for it avoids the necessity of sending down a new address for each channel.

7.6.12 Front Panel Digiswitch Readback

Whenever the signal $\overline{EDIG}$ on J83-19 is low, it puts the front panel digiswitches on the system digital bus. This occurs when LDS (local digital strobe) is high or when pin 1 or 2 of Z15 is low. Pin 1 of Z15 is low during "local" control and not in the digital input mode; pin 2 of Z15 is low during a digital input cycle, while the address and range registers are not being read, and the current address is in the range from 6000 to 7777 (both AR1 and AR2 are high). LDS is a signal whose function here duplicates that of Z15-11 and is included for testing purposes. The net result is that the digiswitches are always on the bus in the "local" mode unless the digital input mode is selected, in which case they are on the bus only if the digiswitch address is used.

7.6.13 Digital Input and Output Modes

Z10-9 is high when the system is in the digital input mode and digital data is being sent back to the computer or to the data lites on the front panel. Z10-9 is low when the system is in the output mode and data is being sent from the computer to user cards or to the range and address registers. The 'in" and "out" modes correspond to "read" and "write" from the computer's view-point. In "remote" control the state of Z10 is controlled by the negative pulses IN (J84-25) and OUT (J84-23) from the interface. A pulse on the IN line pulls down on the pre-set input, forcing the selection of the input mode; a pulse on the OUT line clocks a zero into the flip-flop, selecting the "out" mode. The $\overline{Q}$ output of the flip-flop is inverted and sent back to the interface as DIG IN on J83-3 to indicate which mode the system is in. The DIG IN signal also goes to Z3-9, where it is gated and buffered to drive the RDUSR (read user cards) line (J84-6), which goes to the user card backplane to tell the user cards when the system is in the "in" mode so that they can place their digital information on the bus if they are addressed. The RDUSR signal is blocked if the address and range registers ($\overline{ERA}$) or the digiswitches (AR2 is high) are being read. Thus, the user cards are prevented from going on the bus if address 1777 is exceeded in the digital input mode.

During "local" control the DATA IN and DATA OUT buttons control the state of Z10-9 when the system is in the D/A mode. Under these conditions Z12-1 will be high. Pushing the DATA IN button will send a positive pulse through Z18-8 to the pre-set input of Z10, selecting the "in" mode. The DATA OUT button will have a high on it during "local" control; pushing it then will send a positive level to Z19-9, clearing Z10 and thus selecting the "out" mode. Additional inputs to Z19 cause the selection of the "out" mode whenever the ANALOG MODE or DIGITAL MODE buttons are pushed (through T1), whenever the system is cleared (through CLR), or whenever the SELECT button is pushed (through RM). The LDS signal from Z20 is similar to the $\overline{DIN}$ line in that it reflects the selection of the "out" mode, but it differs in that it operates only during "local" control (cleared by RMT). To indicate the "out" mode, LDS goes high slightly after $\overline{DIN}$ (due to R46 & C39), and to indicate the "in" mode it goes low slightly before $\overline{DIN}$ (due to R47 & C40). As a result LDS indicates the "out" mode slightly after it has been selected, thus providing an advance indication of the selection of the "in" mode before it occurs. LDS is used to gate the DIG STROBE pulses that strobe data into the user cards so that they have valid data presented to them at all times.

7.6.14 Digital or ADC Data Indicator Lites

Z9-3 and Z15-6 drive the DIGITAL DATA and ADC DATA lites on the front panel. The DIGITAL DATA lite is on when the system is in the "in" mode; the ADC DATA lite is on when the system is in the A/D mode; but both lites are off when BLAD (blank display) is high (BLAD is high during the D/A "out" mode).

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7.6.15 CLEAR Signals

The CLR2, $\overline{\text{CLR2}}$, and $\overline{\text{CLR}}$ signals are activated during "remote" control by the $\overline{\text{CLR}}$ line from the interface or during "local" control by the CLEAR button. These signals are the primary clearing and initialization lines for the system. Their functions are tabulated below:

CLR (on the display panel)

1) Puts the address register in the A/D decoding mode.
2) Puts the system in the "out" mode.
3) Disables the LDS signal.
4) Disables the "dynamic" mode.

CLR2 (on the address board)

1) Clears the range and address registers.

$\overline{\text{CLR2}}$ (on the user card backplane)

1) Goes to all user cards to perform "local" clearing and resetting functions (e.g. opening relays, clearing DAC's, etc.).

7.6.16 Local Oscillator

IC Z21 is an oscillator that produces pulses twice each second when the system is in "local" control. These pulses, in conjunction with the front panel push buttons, control three system functions. In the D/A output mode when LDS is high, the pulses send DIG STROBE's to the user cards through Z15 pins 9 & 10. In the A/D mode the local oscillator sends MSR1 pulses to the signal processor through Z6 pins 5 & 6 and Z6-3 to start A/D conversions. (Note that during "remote" control the MSR pulses from the interface go to the signal processor through Z6-2.) The third function of the local oscillator is to gate the dynamic address signal (DADD) on and off when the dynamic mode is in operation.

7.6.17 DYNAMIC Mode

IC Z20 pin 9 is high when the front panel is in the "dynamic" mode. This IC and its associated components are operable only during "local" control; they simulate the changing address conditions typical of computer control during the "remote" mode. If the system is in "local" control and in the A/D mode, pushing the DYNAMIC MSR button will strobe a "1" into Z20, lighting the DYNA MSR indicator LED and enabling gate Z6. Now, whenever the front panel oscillator goes high, it will cause Z6-1 and Z6-10 to go low. When Z6-10 goes low, it enables normal A/D addressing on the address board, and Z6-1 starts an A/D conversion. Some period of time after the A/D conversion is completed, the front panel oscillator will go low, causing DADD to go high, thus inverting the MSB of the address word going to the user card backplane.

The net result is that the address chosen by the operator and loaded into the address register is sent to the analog multiplexers at the same time that the A/D conversion is started (simulating computer control), and that address is removed before the next conversion begins. This technique is useful in testing slew rate, settling time, charge pump, and other dynamic analog system characteristics.

7.6.18 Digital Strobe Pulses and SSH Control

IC Z16 pin 4 produces the digital strobe signal that goes to the user card backplane through Z4 and J83-2 to strobe digital data into the user card being addressed during a digital output transaction. These pulses are initiated by DIG OUT (J83-21) from the interface during "remote" control or by the front panel oscillator through Z15-8 during "local" control. Another way to initiate a digital strobe pulse is via the externally synchronized simultaneous sample-and-hold (SSH) circuitry built around IC Z2. This circuitry comes into action whenever a digital output occurs to addresses of 400X or 600X (or any address where AR2 in the address register is high). Digital output addresses in the "6000" block are used to operate simultaneous sample-and-hold user cards with an external synchronization control as follows.

Digital Output Address

Computer Controlled	Externally Controlled	Effect
4000	6000	All Channels In "Sample"
4001	6001	Even Channels In "Hold"
4002	6002	Odd Channels In "Hold"
4003	6003	All Channels In "Hold"

The user cards decode the LSB's of the address to perform the specific function desired upon receipt of the digital strobe pulse. The purpose of Z2 is to hold off the digital strobe pulse until an external signal coming through J28 on the rear panel of the ANDS5400 starts the process. If AR2 is high, Z14-12 blocks DIG OUT from triggering Z16. When AR2 is high, Z18-12 is low and Z2-1 is high, releasing the flip-flop. When DIG OUT does occur, Z2 has a "one" clocked into it, causing the READY TO HOLD signal (J83-4) to go high on J28, thus indicating to the user that the computer has issued the external "hold" command and the system is "ready to hold." At the same time Z2-9 will go high, driving the SSH line back to the interface on J83-8, thus telling the program that the system is waiting for the external trigger. When the external event occurs, the user will raise the HOLD line on J83-10 coming from J28-5, causing the DIG STROBE pulse to go to the user cards. The rising edge of DIG STROBE will clear Z2-5, causing READY TO HOLD to go down; the trailing edge of DIG STROBE will clear SSH, telling the computer that the sequence is completed.

If the user does not pull down on the HOLD line at all, the sequence will still be completed with READY TO HOLD and SSH rising and falling briefly. To avoid hanging the system because of a lack of response from the HOLD line, the program can abort the sequence by pulsing the CLR1 line from the interface through J83-19, thus resetting both halves of Z2.

7.6.19 Address Register Display

The four IC's Z33, Z34, Z35, and Z36 are BCD-to-seven-segment decoder/drivers that are connected directly to the address register on the address board through the AR1 (address register MSB) to AR12 (address register LSB) lines. The four octal displays on the front panel always show the contents of the address register during both "local" or "remote" modes. The pin 5 to pin 4 connections between the IC's serve to blank leading zeros on the display.

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7.6.20 DATA Display

Two sections of Z23, as well as Z27, Z28, Z29, Z30, and Z31 drive the data displays in a similar way. The data lines DL1 (MSB) through DL16 (LSB) come from a digital multiplexer on the address board that selects between the system digital bus (to show digital input data) or the A/D converter data (to show the results of a conversion). Leading zeros are blanked here also, and the entire display goes blank during digital output transactions when BLAD (blank display) is active.

7.6.21 Range Register Display

Z32 and its associated components decode and display the range register bits RR1 (MSB) through RR4 (LSB). Both digits of the octal display are blank except during the A/D mode.

7.6.22 Range Register Decoding

The remaining circuitry drives the lines that establish the gain and measurement mode (single-ended or differential) of the signal processor card according to the following truth table:

Display Octal	Range Register Bits				Signal Processor Control Lines				
	RR1	RR2	RR3	RR4	M1	M2	M3	$\overline{SE}$	$\overline{GA}$
17	1	1	1	1	1	1	1	1	0
16	1	1	1	0	1	1	0	1	0
15	1	1	0	1	1	0	1	1	0
14	1	1	0	0	1	0	0	1	0
13	1	0	1	1	0	1	1	1	1
12	1	0	1	0	0	1	0	1	1
11	1	0	0	1	0	0	1	1	1
10	1	0	0	0	0	0	0	1	1
7	0	1	1	1	1	1	1	0	1
6	0	1	1	0	1	1	0	0	1
5	0	1	0	1	1	0	1	0	1
4	0	1	0	0	1	0	0	0	1
3	0	0	1	1	0	1	1	0	1
2	0	0	1	0	0	1	0	0	1
1	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	0	0	0	1

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7.6.23 Front Panel Address Board

The front panel address board, mounted behind the display board, is a multilayer PC card containing the front panel digiswitches and drivers, the address register, the range register, the data display multiplexer, and the A/D or D/A decoding circuitry.

There are two 50-pin connectors on the address board that connect to the display board (J1) and the system internal backplane (J2). J1 mates with J83 on the display panel, so its signals' names and fuctions are identical to those listed under J83 at the beginning of this section. The J2 signal listing is as follows:

Signal Name	Conn.	To	From	Function
A7	J2-1	UC		User Card Address Bus Bit 7
A6	J2-2	UC		User Card Address Bus Bit 6
A4	J2-3	UC		User Card Address Bus Bit 4
A8	J2-4	UC		User Card Address Bus Bit 8
A5	J2-5	UC		User Card Address Bus Bit 5
A10	J2-6	UC		User Card Address Bus Bit 10
$\overline{A5}$	J2-7	UC		User Card Address Bus $\overline{Bit\ 5}$
A11	J2-8	UC		User Card Address Bus Bit 11
$\overline{A4}$	J2-9	UC		User Card Address Bus $\overline{Bit\ 4}$
A9	J2-10	UC		User Card Address Bus Bit 9
$\overline{A6}$	J2-11	UC		User Card Address Bus $\overline{Bit\ 6}$
A12	J2-12	SP		User Card Address Bus Bit 12
$\overline{BX0}$	J2-13			Not Used
D5	J2-14	UC	UC	ANDS5400 Bidirectional Digital Bus Bit 5
A1	J2-15	UC		User Card Address Bus Bit 1
D8	J2-16	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 8
A2	J2-17	UC		User Card Address Bus Bit 2
D1	J2-18	UC	UC	ANDS5400 Bidirect'al Dig Bus Bit 1 (MSB)
A3	J2-19	UC		User Card Address Bus Bit 3
D2	J2-20	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 2
$\overline{A7X}$	J2-21	UC		User Card Address Bus Bit $\overline{A7X}$
D4	J2-22	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 4
A7X	J2-23	UC		User Card Address Bus Bit A7X
D3	J2-24	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 3
D16	J2-25	UC	UC	ANDS5400 Bidirect'al Dig Bus Bit 16 (LSB)
D14	J2-26	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 14
D10	J2-27	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 10
D15	J2-28	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 15
D11	J2-29	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 11
D13	J2-30	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 13
D7	J2-31	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 7
D9	J2-32	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 9
D6	J2-33	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 6
D12	J2-34	UC	UC	ANDS5400 Bidirect'al Digital Bus Bit 12
B2	J2-35		ADC	A/D Converter Bit 2
B3	J2-36		ADC	A/D Converter Bit 3
B1	J2-37		ADC	A/D Converter Bit 1 (MSB)
B4	J2-38		ADC	A/D Converter Bit 4
B13	J2-39		ADC	A/D Converter Bit 13
B14	J2-40		ADC	A/D Converter Bit 14
B16	J2-41		ADC	A/D Converter Bit 16 (16 bit LSB)
B8	J2-42		ADC	A/D Converter Bit 8
B15	J2-43		ADC	A/D Converter Bit 15
B6	J2-44		ADC	A/D Converter Bit 6
B7	J2-45		ADC	A/D Converter Bit 7
B10	J2-46		ADC	A/D Converter Bit 10
B9	J2-47		ADC	A/D Converter Bit 9
B12	J2-48		ADC	A/D Converter Bit 12
B11	J2-49		ADC	A/D Converter Bit 11
B5	J2-50		ADC	A/D Converter Bit 5

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7.6.24 Digiswitches and Drivers

The front panel digiswitches are shown on the schematic as SW1A (MSD) through SW1F (LSD). Their common arms are tied to +5 volts through R7, and their outputs are pulled to ground through two 10k ohm resistor networks so that the inputs to Z20, Z22, and Z24 represent a positive-true 16 bit binary word indicative of the octal setting of the switches. These IC's are non-inverting CMOS tri-state bus drivers that put the digiswitch information on the ANDS5400 bidirectional digital bus when the $\overline{\text{EDIG}}$ line is low.

7.6.25 Address and Range Registers

The ANDS5400 12 bit address register consists of IC's Z11, Z16, and Z12; the 4 bit range register is Z15. The inputs to these registers are driven by the non-inverting 8833 receivers Z13, Z14, Z17, and Z18, which "listen" to the system CMOS digital bus and generate enough power to drive the LS inputs of the registers. The address register is loaded by LADD, incremented by IADD, and cleared by CLR2; the range register is loaded by LRAN and cleared by CLR2. The 12 bit address word is labled AR1 (MSB) through AR12 (LSB). The range register outputs are labeled RR1 (MSB) through RR4 (LSB); these bits are loaded by the upper four bits of the digital bus (D1 through D4). The lower 12 bits of the digital bus are used to load the address register; thus, AR1 is loaded by D5, etc.

The outputs of both the range and address registers are pulled up to +5V by RN2 and RN3 to make them compatible with the CMOS inputs of Z19, Z21, and Z23. When $\overline{\text{ERA}}$ is low, these 80C97 non-inverting CMOS tri-state drivers are enabled, placing the contents of the range and address registers on the ANDS5400 digital bus during readback (digital input with address 2000).

7.6.26 DATA Display Multiplexer

IC's Z4, Z5, Z9, and Z8 comprise a 2-into-1, 16 bit digital multiplexer that can choose between the 16 bit A/D converter result or the 16 bit ANDS5400 digital bus. Z3-8 is high (choosing the digital bus) only when DIG IN is high. When Z3-11 goes high, the outputs of the multiplexer all go to zero, regardless of other conditions. This action, used to blank the leading digits of the display through leading zero suppression, creates BLAD, which blanks the final digit of the data display. The data selection and display blanking is dictated by the system modes according to the following truth table:

Address Mode	Bus Mode	Display
D/A	OUT	Blanked
D/A	IN	Digital Bus Data
A/D	OUT	A/D Converter Data
A/D	IN	Blanked (Illegal Mode Combination)

7.6.27 A/D and D/A Decoding

The address register outputs do not go directly to the user card backplane but pass through a digital multiplexer (Z1, Z6, and Z10) that can select between two forms of address bit manipulation, A/D or D/A decoding. A/D decoding is used when the system is measuring analog inputs with the A/D converter; D/A decoding is used when digital data is being transferred through digital output or digital input transactions. The multiplexer IC's apply their "A" inputs to their "Y" outputs during A/D decoding and their "B" inputs to the "Y" outputs during D/A decoding.

The "A" and "B" inputs to the multiplexer come from an area on the PC board that has been layed out to accept two 24-pin sockets; socket S1 (denoted by circles on schematic D5-8662) dictates the D/A decoding that goes to the "B" inputs, and socket S2 (denoted by hexagons on the schematic) dictates the A/D decoding that goes to the "A" inputs. Many variations of decoding are made possible by altering the jumpers on these sockets; however, to provide standardization without sacrificing flexibility, standard decoding that allows 32 analog channels and 4 digital channels per card slot is used in all systems, unless a deviation is absolutely necessary. Since standard decoding is almost always used, the jumpers necessary to accomplish this have been put in the PC board etch (denoted as cuttable jumpers on the schematic) so that sockets and jumpers are not required. The correspondence between the address register bits (AR1 through AR12) and the address bus bits (A1 through A12) is listed below for standard decoding:

7.6.28 Standard Decoding Chart (A/D 32/16 channels; D/A 4 channels)

Address Reg Bit	Address Bus Bit (A/D)	Address Bus Bit (D/A)
AR1	A1	$\overline{\text{A11}}$
AR2	A2	Not Used By User Cards
AR3	A3	A10
AR4	A4	A1
AR5	A5	A2
AR6	A6	A3
AR7	A7	A4
AR8	A8	A5
AR9	A9	A6
AR10	A10	A7
AR11	A11	A8
AR12	A12*	A9

*(Goes to the Signal Processor)

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7.6.29 System Addressing

7.6.29.0 General

The address and logic control circuits provide the signals necessary to select a specific user card and to direct data to or from the user input/output and computer interface cards. The elements that tie these cards together are the Address Bus, the Data Bus, and the Analog Bus. The user may find it helpful to refer to Figure 7-1 throughout this discussion of system addressing.

Address	Digital Input	Digital Output	Analog Input
7777 6000	Front Panel Digiswitch	Ext SSH	All User Card Analog Input Channels
4000	Interrupt Vectors	Int SSH	
2000	Range & Address Register	Not Used	
1000	Not Used		
0000	User Cards	User Cards	

Figure 7-1. System Address Map

7.6.29.1 Address Mode Format

There are two methods of accessing channels in the ANDS5400 system. The first is for analog input, the second for digital input, digital output (analog output). Based on the command sequence, which precedes or accompanies the address information, the hardware decides which method of address decoding shall be used to access system channels. The address words delivered to the ANDS5400 system allow selection of a particular channel as shown in Figure 7-2.

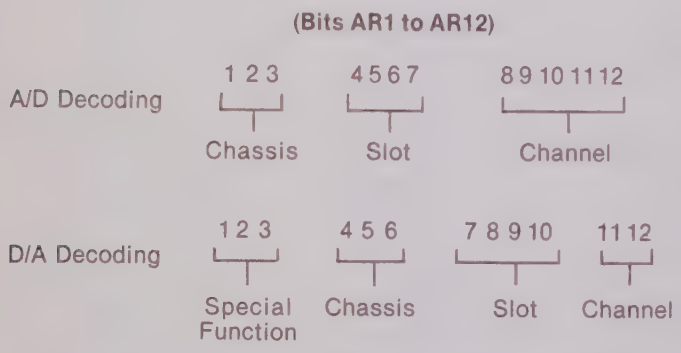

Figure 7-2. Address Register Bit Interpretation

The address format is hardware configurable; that is, jumpers may be installed to change the address map to different configurations. The 32/4 jumper format is referenced here since it yields a maximum of 32 analog input channels per card and a maximum of four digital input, digital output (analog output) channels per card. These jumper configurations are by far the most widely used and, once understood, can be readily transposed to represent the other addressing formats.

7.6.29.2 Analog Mode Addressing

The three MSB's of the 12 bit Address Word (see Figure 7-2) determine the chassis in which the user card and channel of interest are located; the next four bits determine the user card selected within the indicated chassis; and the five LSB's select the channel on that user card. The 12 bit address yields a maximum potential address field of 4,096 channels.

The ANDS5400 may include a maximum of eight chassis. These chassis are selected by the three MSB's of the Address Word, and these bits correspond directly to the number of the chassis in the system. For example, 000 in the three MSB's corresponds to the master chassis, and 111 represents the seventh expansion or, including the master, the eighth chassis in the system.

Each chassis contains 16 input/output slots. The addresses of user cards installed in these slots are determined by the next four MSB's. The first user card in any chassis has a binary code of 0000; the second card a binary code of 0001; the third card a binary code of 0010; and the 16th card has a binary code of 1111. By transmitting the appropriate binary number within both the chassis and the card slot section of the address word, the user may select the chassis in which the card is located and the card that is to be interrogated.

The five LSB's form the Channel Address on any given user card. The maximum number of channels on any given card is 32; therefore, five binary bits are required to decode the channels on the card. A binary code of 00000 in the five LSB's corresponds to the first channel on that card; a binary code of 00001 corresponds to the second channel; a code of 10000 the 17th channel; a code of 11111 the 32nd channel on that card. Therefore, the proper use of the chassis, slot, and channel address bits will permit access to any chassis, card, or channel in the system.

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Figure 7-3 indicates the relative addresses available in any chassis with the 32 Analog Input Address format. To obtain the absolute address the user simply adds the MSB, indicating the expansion chassis number (0-7), to the relative address of the chassis. The addresses are indicated in octal form; therefore, 32 channels in J1 correspond to the addresses in 0 through 37, and so forth to the addresses in J16, which are 740 to 777. The addressing of specific channels on the various types of analog input cards available in the product line is discussed in section 7.6.29.5.

Figure 7-3. Analog Input Address

7.6.29.3 Digital Mode Addressing

As indicated in Figure 7-2, the first three MSB's of the address word are normally unused, except for specific functions, such as simultaneous sample-and-hold. The next three bits of the address word are the chassis address; the next four bits the slot addresses. The user card and chassis address format is identical to that of the analog input mode. As can be ascertained by the two remaining bits, there are only four available addresses per card in this mode of operation.

Figure 7-4 details the relative addresses available in any chassis when the digital input/digital output mode of addressing is used. By simply adding the appropriate chassis address, the user may select any digital input/output channel within the system. It should be noted that it is possible and, in fact, likely that the analog input addresses and the digital input/output addresses will often overlap. For example, an analog input user card may be installed in J1 with the address field of 0 through 037 (octal). A digital output card may also be installed in J2 with addresses of 4 through 7 (octal). There is no interaction between these overlapping addresses; they are completely separated by the addressing hardware into distinct card and channel locations.

7.6.29.4 Address Patch (Refer to Section 7.6.27)

The only address decoding that will normally be available to the customer is the 32/4. There are other address options that may, in special applications, aid the user in system utilization. These are:

Analog Input	16, 8, 4, 2, and 1
Digital Input	8, 2, and 1

These alternate jumper formats will be available only to OEM customers on special request.

7.6.29.5 Address Interpretation

Figures 7-5 and 7-6 delineate the binary and octal equivalents in an example of both analog and digital decoding. The address in Figure 7-5 indicates that the system is addressing the ninth channel in slot 3 of the first expansion chassis. Figure 7-6 indicates that the system is addressing the third channel in slot 6 of the third expansion chassis. As is apparent, the binary address words may be readily and consistently generated using the information provided in the preceding paragraphs. The octal equivalents of those addresses are simply a shorthand means of denoting the binary address that has been generated for a specific channel.

7.6.29.6 Single-Ended/Differential Operation

The AC260, AC261, and AC262 signal processor cards provide the capability, via appropriate programming, to operate the system in either its differential or single-ended mode. Control over the operation is accomplished by writing to the range register of the AC260/AC262 a "1" or a "0" bit in the most significant octal location of its control register. For example, to operate the system in the single-ended mode of operation using the AC262, the user would program an octal 00 into the range register. To operate it differentially, the user would program an octal 10 into the range register of the AC262. The AC260 and AC261 extend the capabilities of the AC262 by permitting programmable gain ranges in binary steps up to X32. These gains are implemented by programming the least significant octal digit of the range word with a binary code.

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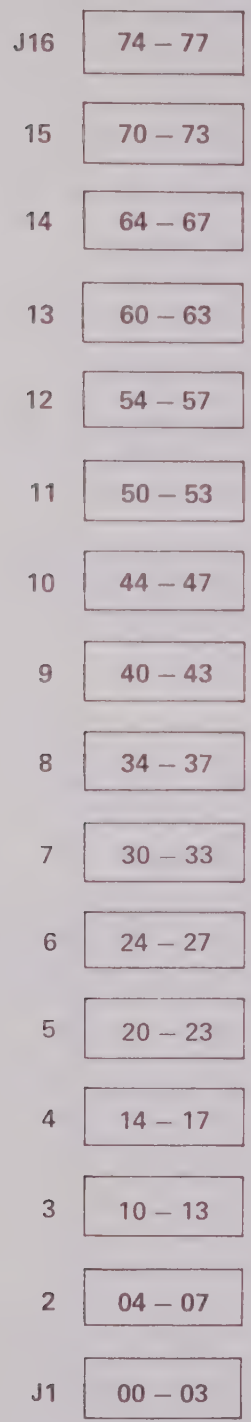

Figure 7-4. Digital Input/Digital Output Address Map

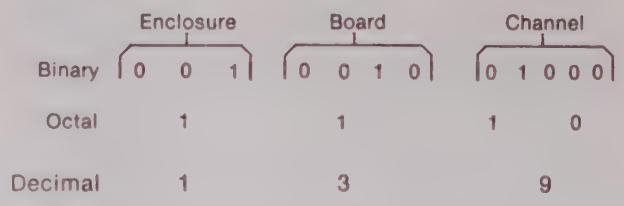

Figure 7-5. Analog Input Address

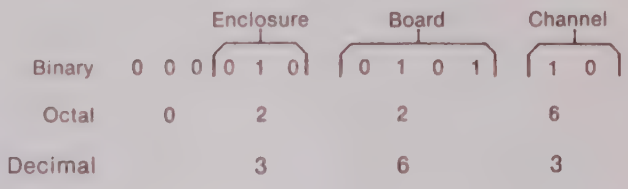

Figure 7-6. Digital Input, Digital Output (Analog Output) Address

MODEL	Valid Octal Address
AC405X Series AC407X Series AC425X Series AC427X Series AC43XX Series	0, 10, 20, 30, 40, 50, 60, 70
AC4720 (SE)	0-37 40-77
AC4720 (DI) AC473X AC4740 AC475X AC476X	0, 2, 4, 6, 10...36 40, 42, 44, 46, 50...76
AC280/1 (DI)	0, 10, 20, 30, 40, 50, 60, 70

Figure 7-7. Absolute Analog Address

MODEL	OCTAL ADDRESS
AC19XX AC19XXTC DC66X0 DC6700	0 4
AC1330 AC1530 AC1813/14 DC6000 DC6100 DC6200 DC6500	0,2 4,6
AC1562 DC6300	0,1,2,3, 4,5,6,7

Figure 7-8. Absolute Digital Input, Digital Output (Analog Output) Address

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7.6.29.7 Absolute Analog Addressing

Figure 7-7 delineates the twelve basic analog input cards that are available in the ANDS5400 and their valid octal addresses. The AC405X, AC407X, AC425X, AC427X, and AC43XX are 4-channel input cards and have valid addresses at 0, 10, 20, and 30 in odd-numbered card slots and 40, 50, 60, and 70 in even-numbered card slots. These cards are intended to be measured with the signal processor range register in its differential mode of operation.

The AC4720 provides 32 channels of analog input. Its valid addresses are 0 through 37 in odd-numbered card slots, and 40 through 77 in even-numbered card slots. This device is intended to be used with either single-ended or differential modes. When differential operation is selected, the valid addresses in the odd card slots are 0, 2, 4, 6, 10, and so forth, to 36 and in even card slots 40, 42, 44, 46, 50, and so forth, to address 76.

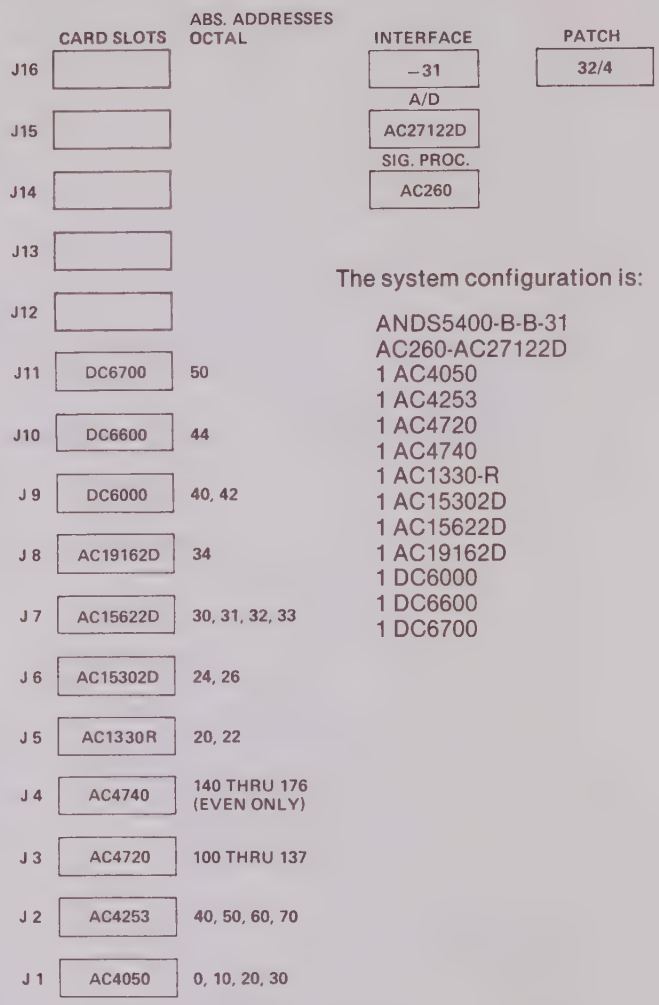
The AC4730, AC4740, AC4750, and AC4760 are specialized versions of the AC4720. All of the devices in the AC4730 through AC4760 category are measured differentially and, therefore, have odd card slot addresses of 0, 2, 4, 6, 10, and so forth to 76. The AC280 and AC281 are 4-channel input devices that are measured differentially. The odd card slot addresses are 0, 10, 20, and 30, and the even card slot addresses are 40, 50, 60, and 70.

7.6.29.8 Absolute Digital Addresses

Figure 7-8 delineates the valid addresses for digital input/output devices in octal code. The AC19XX, the AC19XX-TC, the DC6620, and the DC6700 are all single-channel devices. The valid address at odd card slots is 0; the valid address at even card slots is 4. AC1330, AC1530, AC1813/14, DC6000, DC6100, DC6200, and DC6500 have two addresses on each card. The valid address at odd card slots is 0 and 2 and at even card slots 4 and 6. The AC1562 and DC6300 have valid addresses in odd card slots of 0, 1, 2, and 3, and even card slots of 4, 5, 6, and 7.

7.6.29.9 Addressing Sample

The preceding paragraphs have progressed from the address structure of the ANDS5400 to the address configuration of the device. For an overall view of the implications cited above, refer to Figure 7-9, a typical system configuration converted to an absolute address map.



The system configuration is:

ANDS5400-B-B-31
AC260-AC27122D
1 AC4050
1 AC4253
1 AC4720
1 AC4740
1 AC1330-R
1 AC15302D
1 AC15622D
1 AC19162D
1 DC6000
1 DC6600
1 DC6700

Figure 7-9. Example Absolute Address Map

Note: The ANDS5400-B-B-31, AC260, and AC27122D do not have addresses since the front panel control display, interface, signal processor card, and A/D converter are shared by all input cards within the address structure of the system.

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Section 7.6
Front Panel Display and Control

Card Number	Drawing Number	Title
—	D7-2357	Front Panel Display Assembly
—	D5-8663	Display Panel Assembly
—	D4-8663	Display Board Drilling
—	D7-8663	Display Board Assembly
—	D5-8662	Address Board Schematic
—	D7-8662	Address Board Assembly

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REVISIONS					
REV	ECO	DESCRIPTION	DRWN	APP'D	DATE
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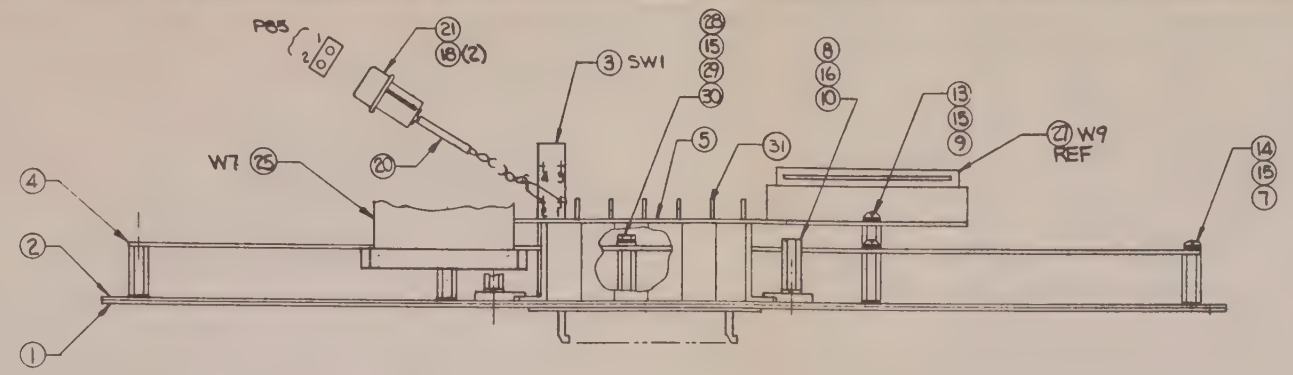
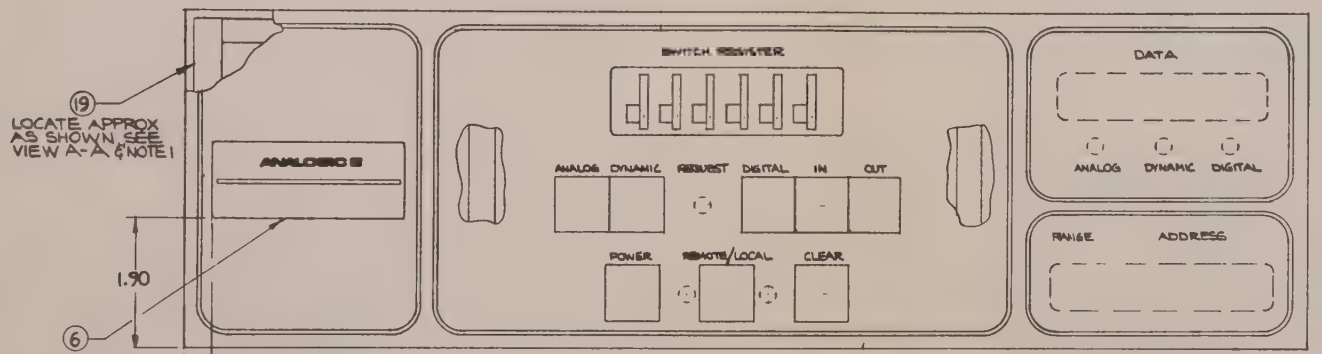
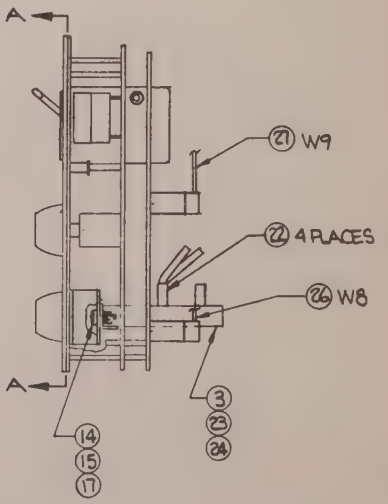
2	1-474	SEE ECO.	DP		7 9 79

D T-2357 2



WIRE LIST				
WIRE NO.	ITEM NO.	COLOR	FROM	TO
1	12	BLK	SW1-1	P85-1
2	11	RED	SW1-2	P85-2





NOTES:

1. INSTALL ITEM 19 BETWEEN ITEMS 1 & 2.
2. TOOLING REQD
   CRIMPING-AMP# 90123-2
   INSERTION-
   EXTRACTION-AMP# 465644-1
3. ASSEMBLY PROCEDURE:
   A. INSTALL ITEM 7 (SPACER) & ITEM 15 (L/WASHER) TO ITEM 2 (SUB PANEL) 9 PLACES.
   B. INSTALL ITEM 31 (SWITCH), ITEM 10 (RETAINER), ITEM 16 (L/WASHER), & ITEM 8 (SPACER).
   C. INSTALL ITEM 1 (FRONT PANEL), (SEE NOTE 1).
   D. INSTALL ITEM 4 (DISPLAY BOARD) WITH REQ'D. HDWR, DO NOT TIGHTEN.

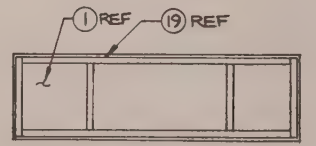
ASSY PROCEDURE CONT.

E. ADJUST ITEM 4 (DISPLAY BOARD), KEY TOPS MUST NOT CONTACT ITEM 1 (FRONT PANEL), TIGHTEN HDWR, INSTALLED AT STEP D.

F. INSTALL ITEM 5 (ADDRESS BOARD), ITEM 9 (SPACER), ITEM 13 (SCREW) & ITEM 15 (L/WASHER), DO NOT TIGHTEN.

G. SOLDER ITEM 31 (SWITCH) TO ITEM 5 (ADDRESS BOARD), TIGHTEN HDWR, INSTALLED AT STEP F.

H. INSTALL ITEM 3 (POWER SWITCH) & RELATED PARTS, NOTE THAT KEY TOP MUST NOT CONTACT ITEM 1 (FRONT PANEL).



VIEW A-A
SCALE 1/4

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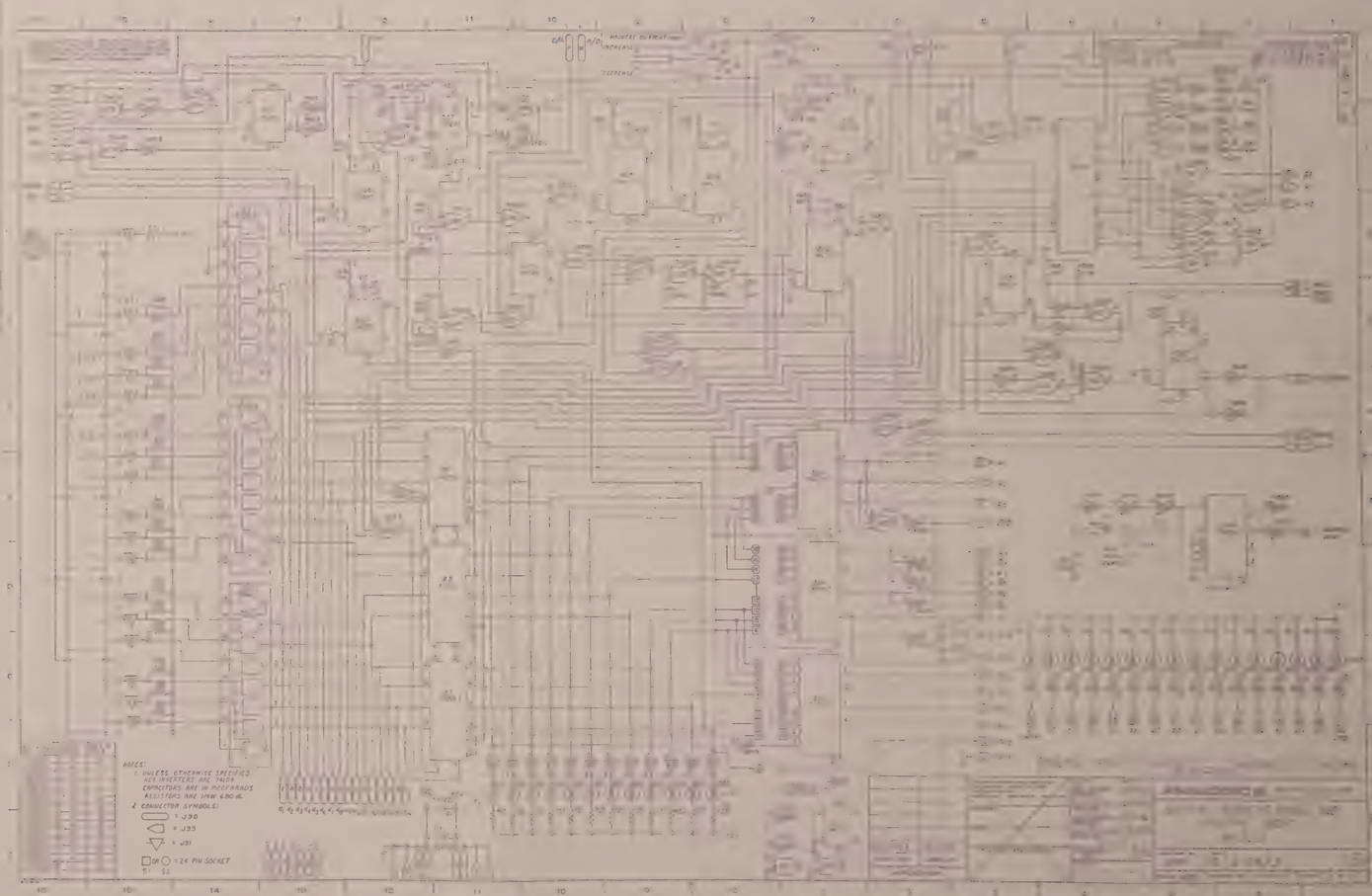
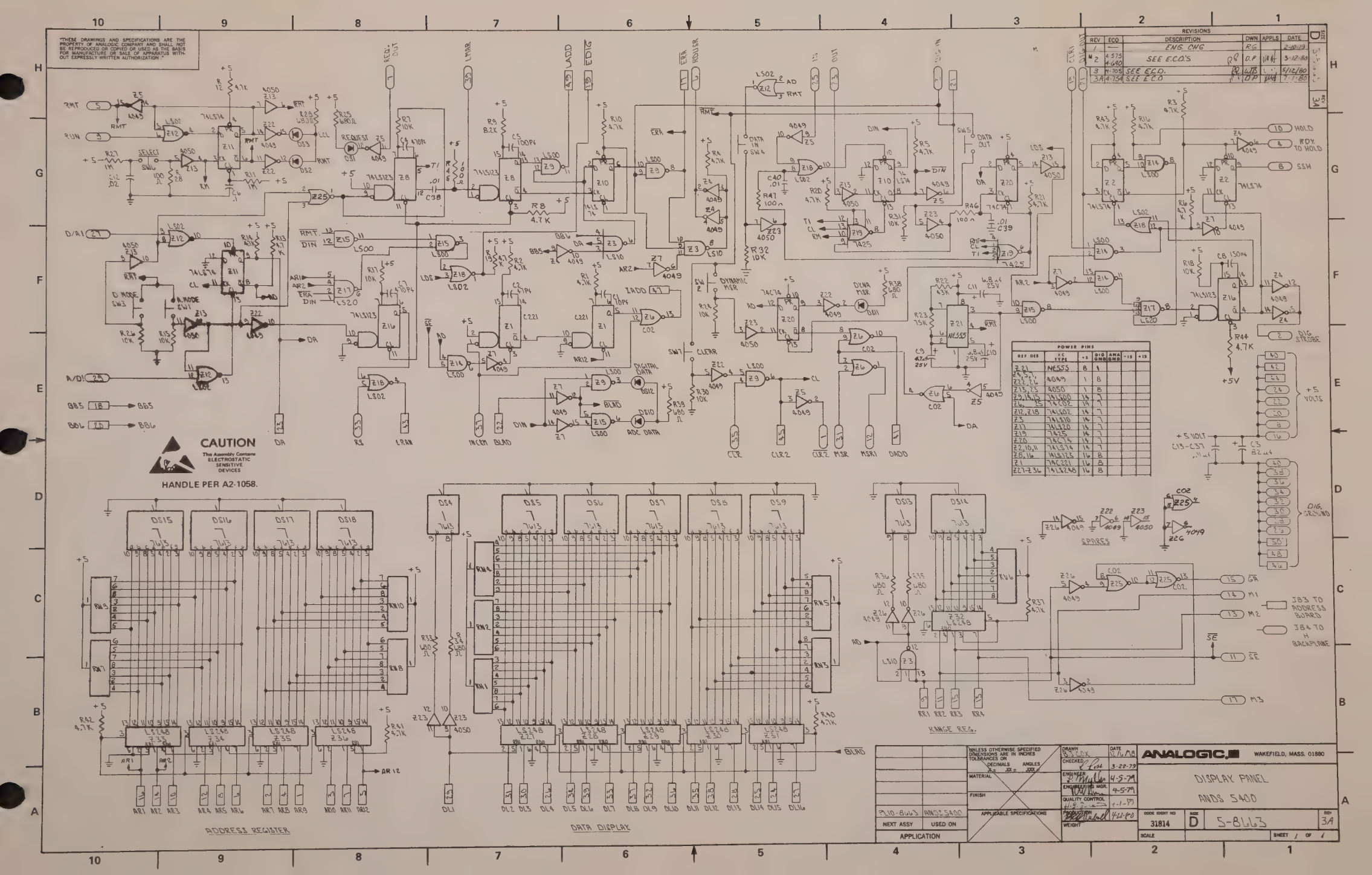
			CHECKED	7 DEC 78	FRONT PANEL ASSY "B"
		MATERIAL	ENGINEER	4-5-79	
		FINISH	ENGINEERING MGR.	4-5-79	
			QUALITY CONTROL	4-22-79	
RIO-3188	AND5400	APPLICABLE SPECIFICATIONS	PRODUCTION CONTROL	4-17-79	
NEXT ASSY	USED ON		WEIGHT		CODE IDENT NO 31814 · SIZE D · DWG NO T-2357 · REV 2
APPLICATION					SCALE 1/1 · SHEET 1 OF 1

		ANALOG P/N
	CAP., .01uf, DISC.	13-110086
	CAP., .1uf, DISC.	13-110086
	CAP., 22pf	13-101008
CR1-34	L.E.D.S.	15-220008
R1-33	RES., 680, 1/4W, 5%, C.C.	12-026819
R34-49,52,53	RES., 22K, 1/4W, 5%, C.C.	12-027339
R50,57,58,65,68,70	RES., 10K, 1/4W, 5%, C.C.	12-027139
R51	RES., 47, 1/4W, 5%, C.C.	12-026709
R55	RES., 100, 1/4W, 5%, C.C.	12-023109
R54,56	RES., 1M, 1/4W, 5%, C.C.	12-027659
R59,62-64,66,69	RES., 4.7K, 1/4W, 5%, C.C.	12-027279
R60	RES., 10M, 1/4W, 5%, C.C.	12-027069
R61,67	RES., 22M, 1/4W, 5%, C.C.	12-022269
R71	RES., 100K, 1/4W, 5%, C.C.	12-027049
SW1-5	SWITCH PUSH BUTTON	15-430000
Y1	CYRSTAL, 200Kc, HC-6 CASE	15-140200
Z1-3,38	I.C., 74C193	14-60C193
Z4	I.C., 74C175	14-60C175
Z5,18,21,25,31,34	I.C., 74C00	14-074C02
Z6-8	I.C., 80C97	14-L80C97
Z9	I.C., 4002	14-L00I0
Z10,12,29	I.C., 74C00	14-074C00
Z11,19,27	I.C., 74C74	14-074C74
Z13-17,26	I.C., 74L04	14-074L04
Z20	I.C., 4025	14-L04025
Z22,28,33,39	I.C., 4049	14-L04049
Z23	I.C., 74C20	14-074C20
Z24,30,32	I.C., 74C221	14-60C221
Z35-37	I.C., 74C157	14-60C157

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REVISIONS
REV ECO DESCRIPTION DWN APPLS DATE
ENG. CHG. RG 2-10-79
SEE E.C.O'S 3-12-80
SEE E.C.O. 5/12/80
SEE E.C.O 7-1-80
CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
POWER PINS
REF DES I.C. TYPE +5 DIG GND ANA GND -15 +15
Z21 NE555 8 1
Z22,23,24 4049 1 8
Z13,23 4050 1 8
Z9,14,15 74LS00 14 7
Z6,25 74LS02 14 7
Z12,Z18 74LS02 14 7
Z3 74LS10 14 7
Z17 74LS20 14 7
Z19 74125 14 7
Z20 74125 14 7
Z2,10,11 74LS174 16 8
Z5,16 74LS123 16 8
Z1 74S221 16 8
Z1-Z36 74LS248 16 8
ADDRESS REGISTER
DATA DISPLAY
KNOB REG.
SPARES
ANALOGIC
WAKEFIELD, MASS. 01880
DISPLAY PANEL
AMDS 5400
5-8663
31814
SIZE D
REV 3A
SHEET 1 OF 1
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN 3-22-79
CHECKED 4-5-79
ENGINEER 4-5-79
ENGINEERING MGR. 7-1-80
QUALITY CONTROL
WEIGHT 422-60
5-8663 AMDS 5400
NEXT ASSY USED ON
APPLICATION

REVISIONS					
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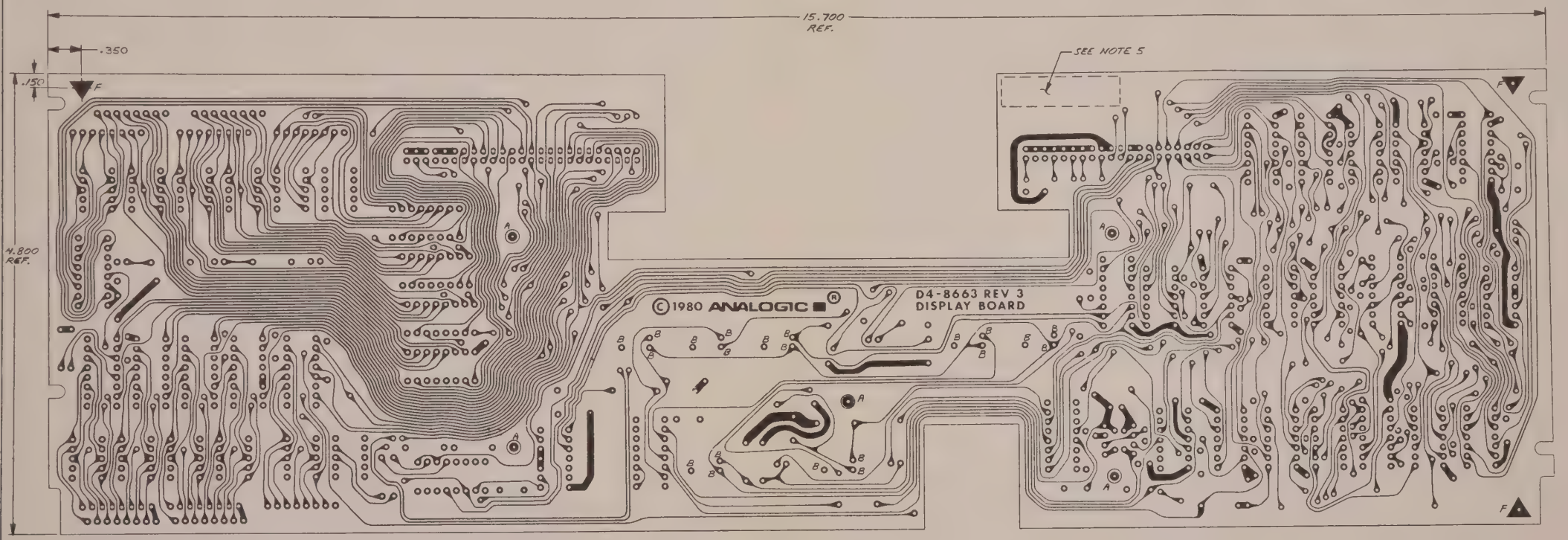
D 4-8663 REV 3



WIRING SIDE

NOTES:

1. FOR MACHINING AND FABRICATION SEE DG-7077.
2. FOR ASSY. SEE 07-8663.
3. SOLDER MASK BOTH SIDES PER A2-1040 PARA 4.2.3 USING SMT 4 OF THIS DRAWING.
4. FABRICATE PER A2-1040.
5. P.C. BOARD MANUFACTURER WILL BE U.L. APPROVED AND WILL MARK THIER U.L. CODE IDENTIFICATION AND THE FLAMMABILITY RATING, EITHER UL-94V-01 OR UL-94V-02 (DEPENDING ON MATERIAL USED). THESE MARKINGS WILL BE PUT ON THE WIRING SIDE OF THE BOARD IN THE AREA DESIGNATED.
6.

HOLE	SIZE	COMMENTS	QTY
NH	.032-.038 DIA.	AFTER PLATING	A/R
A	.147-.152 DIA.	DO NOT PLATE	5
B	.036-.041 DIA.	AFTER PLATING	21
P	.165 +.003 -.000 DIA.	DO NOT PLATE	3

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS X ± .XX ± ANGLES .XXX ±	DRAWN E.J.G.	DATE 5-1-79	ANALOGIC WAKEFIELD MASS 01880
			CHECKED R. EVANS	5-11-79	DRILLING D.F.-AI BOARD AMOS5400
		MATERIAL A2-1040	ENGINEER L. MILLER	4-5-79	
		FINISH A2-1040	ENGINEERING MGR R.J.H.	4-5-79	
			QUALITY CONTROL [illegible]	4-11-79	
PWO-8663	AMOS5400	APPLICABLE SPECIFICATIONS A2-1040	PRODUCTION R. KNOWLES	4-11-79	
NEXT ASSY	USED ON		WEIGHT		CODE IDENT NO 31814 · SIZE D · 4-8663 · REV 3
APPLICATION					SCALE 2:1 · SHEET 1 OF 5

REVISIONS					
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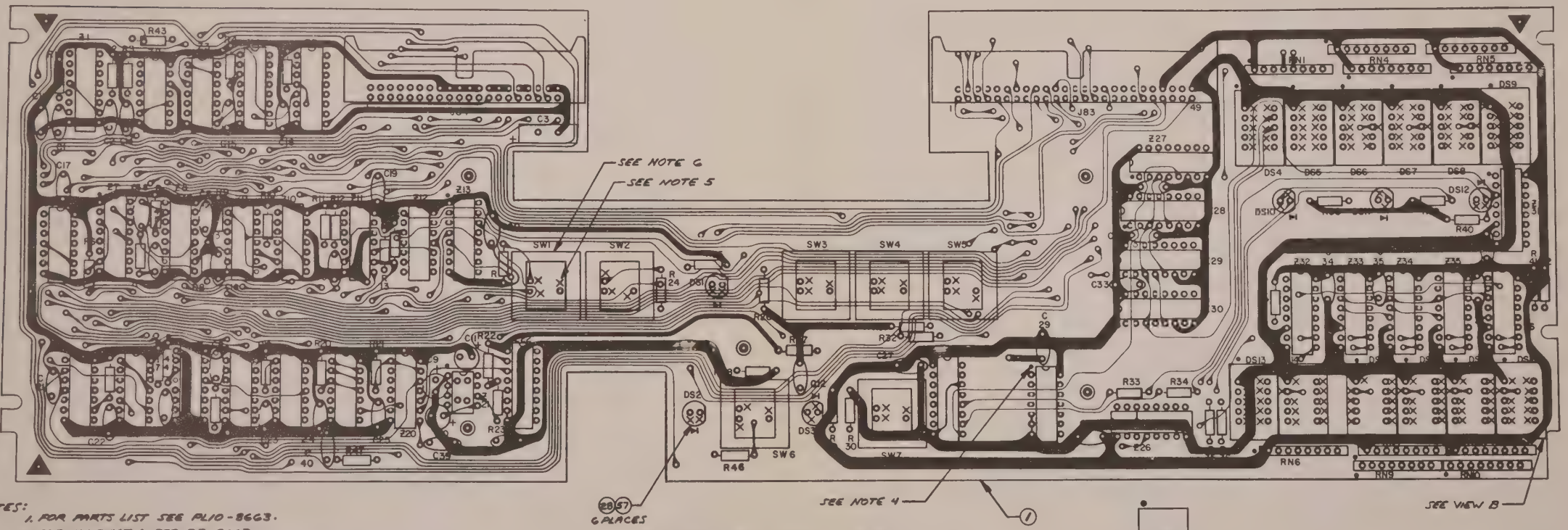
D 7-8663 3



COMPONENT SIDE

NOTES:

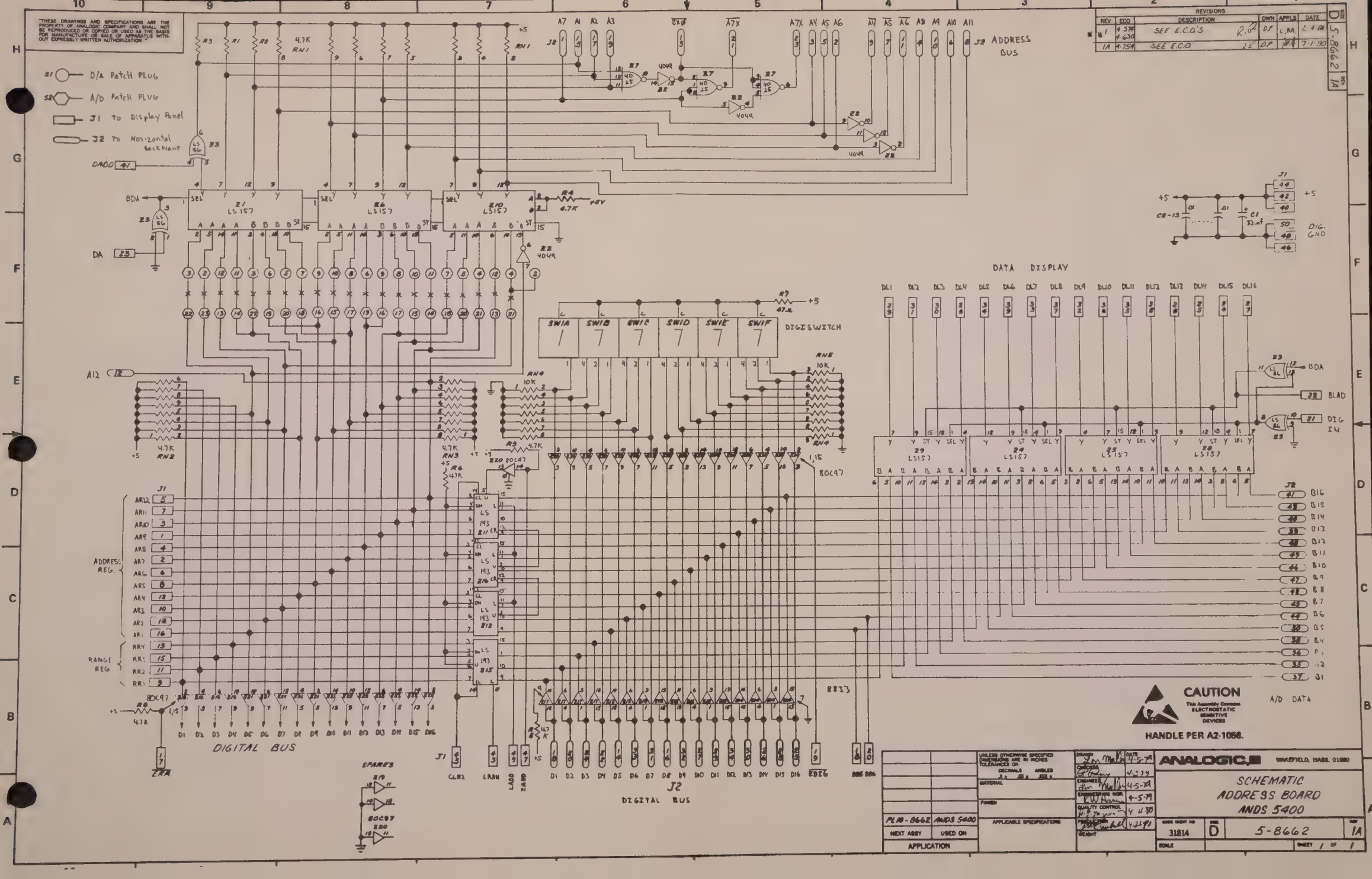
1. FOR PARTS LIST SEE PL10-8663.
2. FOR SCHEMATIC SEE DS-8663.
3. FOR ASSY PROCEDURE SEE A2-1027 & NOTE 7.
4. DOT INDICATES PIN #1 OF INTEGRATED CIRCUITS RESISTOR NETWORKS AND DISPLAYS.
5. COAT ALL HOLES MARKED "X" WITH SOLDER MASK ITEM #4 BEFORE FLOW SOLDERING (QTY: 153).
6. SW1-SW7 (ITEM 60) TO BE MOUNTED FLUSH TO BOARD SURFACE.
7. ASSEMBLY PROCEDURE, ALSO SEE NOTE 3:
   - A. INSTALL ITEM 26 (DISPLAY) TO ITEM 56 (SOCKET) CHECK ORIENTATION ("VIEW B") & INSTALL ON BOARD (ITEM 1) TACK SOLDER 1 LEAD (12 PLACES).
   - B. CHECK ORIENTATION & INSTALL ITEM 28 (LED) ON ITEM 1 (BOARD) TACK SOLDER 1 LEAD (6 PLCS).
   - C. INSTALL ITEM 1 (BOARD) TO A DUMMY FRONT PANEL FIXTURE.
   - D. WITH COMPONENT SIDE DOWN LOOSEN TACK SOLDER JOINTS ALLOWING ITEMS 28 (LED'S, 6 PLCS) AND ITEM 26 (DISPLAYS, 12 PLACES) TO FALL INTO POSITION AGAINST BACK OF FINISHED PANEL AND SOLDER.
   - E. TRIM LEADS APPROPRIATELY.

VIEW B

TYPICAL ORIENTATION OF DISPLAYS ITEM #26 (12 PLACES) MOUNTED ON ITEM #56, SEE NOTE 7

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .X ± .03 .XX ± .01 ANGLES .5°	DRAWN D. Rawn 9/1/77	ANALOGIC	
		MATERIAL	CHECKED R. Ross 9/2/77	ASSEMBLY DISPLAY BOARD AND5400	
		FINISH	ENGINEER L. Miller 9/6/77		
			ENGINEERING MGR. [illegible] 9/6/77		
			QUALITY CONTROL [illegible] 9/14/77		
PL10-8663	AND5400	APPLICABLE SPECIFICATIONS	PROJECT ENGR. [illegible] 9/14/77	CODE IDENT NO 31814	DWG NO D 7-8663 REV 3
NEXT ASSY	USED ON	A2-1027	WEIGHT	SCALE 2:1	SHEET 1 OF 1
APPLICATION					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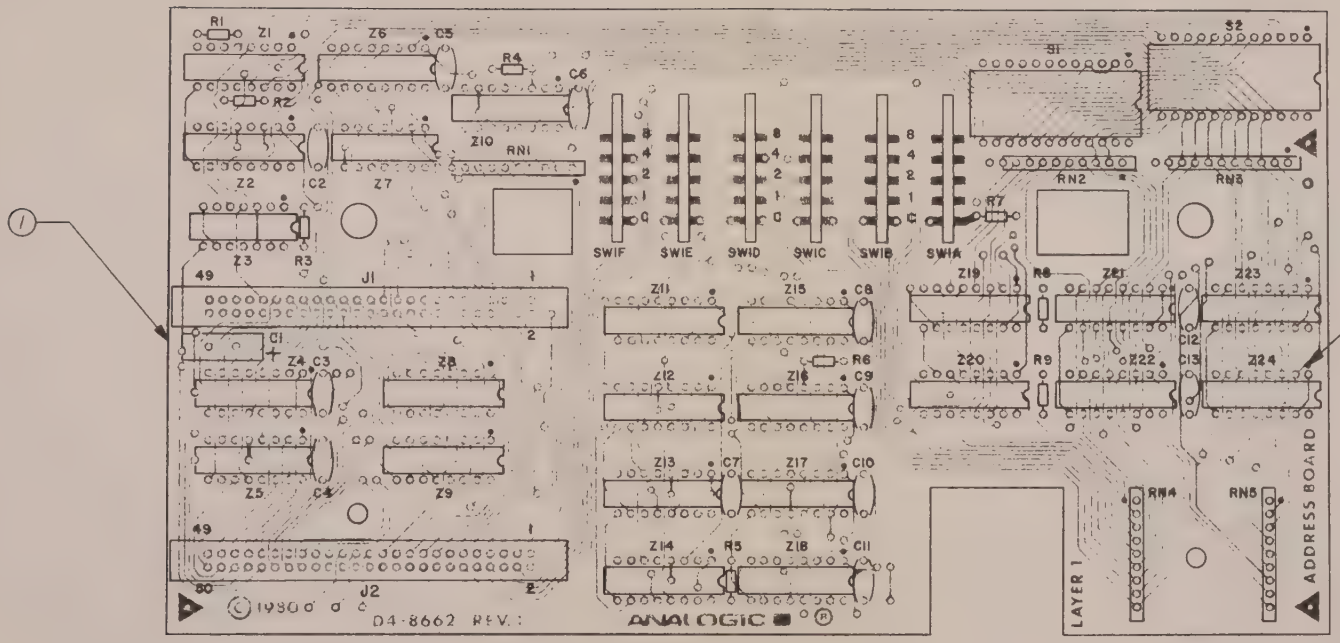
REVISIONS
REV ECO DESCRIPTION DWN APPD DATE
1 4-574 4-630 SEE E.C.O'S R.G. DP L.M. 2-4-88
1A 4-754 SEE E.C.O. DP 7-1-90
D5-8662 1A
S1 D/A PATCH PLUG
S2 A/D PATCH PLUG
J1 TO DISPLAY PANEL
J2 TO HORIZONTAL BACKPLANE
ADDRESS BUS
DATA DISPLAY
DIGISWITCH
DIGITAL BUS
A/D DATA
CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.
SPARES
ANALOGIC
WAKEFIELD, MASS. 01880
SCHEMATIC
ADDRESS BOARD
ANDS 5400
5-8662
1A
31814
SCALE
SHEET 1 OF 1
PLN-8662 ANDS 5400
NEXT ASSY USED ON
APPLICATION
APPLICABLE SPECIFICATIONS

REV	ECO	DESCRIPTION	DWN	APPLS	DATE
1	9-574 1-630	SEE E.C.O.'S	R.P.	D.P.	L.M.	2-4-80

D 7-8662 1



SEE NOTE 2

NOTES:
1. FOR SCHEMATIC SEE D5-8662.
2. DOT INDICATES PIN 1 OF I.C.'S, RN'S & SOCKETS.
3. MANUFACTURE PER A2-1027.

COMPONENT SIDE

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON: DECIMALS .X ±.03, .XX ±.01, ANGLES ±2°	DRAWN R.P.	DATE 11-8-78	ANALOGIC. WAKEFIELD, MASS. 01880
MATERIAL	CHECKED R.CLARY	4-3-79	ASSEMBLY ADDRESS BOARD ANDS 5400
FINISH	ENGINEER L. MULLER	4-5-79	
	ENGINEERING MGR. R.M. HAVLNER	4-5-79	
	QUALITY CONTROL [illegible]	4-1-80	
PL10-8662 ANDS 5400	APPLICABLE SPECIFICATIONS A2-1027		CODE IDENT NO 31814 · SIZE D · 7-8662 · 1
NEXT ASSY · USED ON · APPLICATION			SCALE 2:1 · SHEET 1

7.7 User Card Backplane

7.7.0 General

The user card backplane, at the rear of the ANDS5400 system, has 16 slots that connect to a universal bus structure used to communicate to any type of user card. Provided that the total power availability in the chassis is not exceeded, any combination of cards is acceptable.

7.7.1 User Card Bus Pin Connections

NOTE: EXP = Expansion Cards

Signal Name	Conn.	To	From	Function
A8	JXX-1		FP	Address Bus Bit 8
A9	JXX-2		FP	Address Bus Bit 9
A10	JXX-3		FP	Address Bus Bit 10
A11	JXX-4		FP	Address Bus Bit 11
D2	JXX-5	INT,FP	INT,FP	Bidirectional Digital Bus Bit 2
D4	JXX-6	INT,FP	INT,FP	Bidirectional Digital Bus Bit 4
D6	JXX-7	INT,FP	INT,FP	Bidirectional Digital Bus Bit 6
D8	JXX-8	INT,FP	INT,FP	Bidirectional Digital Bus Bit 8
D10	JXX-9	INT,FP	INT,FP	Bidirectional Digital Bus Bit 10
D12	JXX-10	INT,FP	INT,FP	Bidirectional Digital Bus Bit 12
D14	JXX-11	INT,FP	INT,FP	Bidirectional Digital Bus Bit 14
D16	JXX-12	INT,FP	INT,FP	Bidirectional Digital Bus Bit 16
DIG STROBE	JXX-13		FP	Digital Strobe To Load Data
$\overline{\text{CLR2}}$	JXX-14		FP	Clearing, Resetting Pulse
PRIORITY IN	JXX-15		EXP	Interrupt Priority Input Signal
DIG. GND.	JXX-16		PS	Digital Ground
+5	JXX-17		PS	+5 Volt Power
+15	JXX-18		PS	+15 Volt Power
−15	JXX-19		PS	−15 Volt Power
BOX SIG. RTN.	JXX-20	EXP		Chassis Signal Return Analog Bus
BOX ODD	JXX-21	EXP		Chassis "Odd" (−) Analog Bus
ANA. GND.	JXX-22		PS	Analog Ground
A4 or $\overline{\text{A4}}$	JXX-A		FP	Address Bus Bit (See Text)
A5 or $\overline{\text{A5}}$	JXX-B		FP	Address Bus Bit (See Text)
A6 or $\overline{\text{A6}}$	JXX-C		FP	Address Bus Bit (See Text)
A7X or $\overline{\text{A7X}}$	JXX-D		FP	Address Bus Bit (See Text)
D1	JXX-E	INT,FP	INT,FP	Bidirectional Digital Bus Bit 1
D3	JXX-F	INT,FP	INT,FP	Bidirectional Digital Bus Bit 3
D5	JXX-H	INT,FP	INT,FP	Bidirectional Digital Bus Bit 5
D7	JXX-J	INT,FP	INT,FP	Bidirectional Digital Bus Bit 7
D9	JXX-K	INT,FP	INT,FP	Bidirectional Digital Bus Bit 9
D11	JXX-L	INT,FP	INT,FP	Bidirectional Digital Bus Bit 11
D13	JXX-M	INT,FP	INT,FP	Bidirectional Digital Bus Bit 13
D15	JXX-N	INT,FP	INT,FP	Bidirectional Digital Bus Bit 15
$\overline{\text{RDUSR}}$	JXX-P		FP	Read User Cards, High During Dig. In
$\overline{\text{BOX REQUEST}}$	JXX-R	EXP,INT		Pulled Low By User Cards To Req Intpt
PRIORITY OUT	JXX-S	NXT UCD		Priority Out To Next User Card
DIG. GND.	JXX-T		PS	Digital Ground
+5	JXX-U		PS	+5 Volt Power
+15	JXX-V		PS	+15 Volt Power
−15	JXX-W		PS	−15 Volt Power
BOX SIG. RTN.	JXX-X	EXP		Chassis Signal Return Analog Bus
BOX EVEN	JXX-Y	EXP		Chassis "Even" (+) Analog Bus
ANA. GND.	JXX-Z		PS	Analog Ground

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7.7.2 User Card Address Bus

The user cards recognize their addresses by monitoring the CMOS compatible signals A4, A5, A6, A7X, A8, A9, A10 and A11 on the user card bus. (See Figure 7-11). The signals that determine the slot address, A4, A5, A6, A7X, $\overline{A7X}$, are wired differently on each user card slot within each chassis so that user cards will assume the address of the slot into which they are plugged. These four lines are capable of accessing 16 slots in a binary counting fashion; however, to avoid using address switches on each card the signals have been wired to the slots in either their true or complement form as required so that the cards need only look for "ones" on all four lines.

PIN	J1	J2	J3	J16
A	$\overline{A4}$	$\overline{A4}$	$\overline{A4}$	A4
B	$\overline{A5}$	$\overline{A5}$	$\overline{A5}$	A5
C	$\overline{A6}$	$\overline{A6}$	$\overline{A6}$	A6
D	$\overline{A7X}$	A7X	$\overline{A7X}$	A7X

Figure 7-11. User Card Address Bus

In addition to this special wiring, A7X has been preconditioned so that A7X or $\overline{A7X}$ can be high only in the chassis being addressed. As a final result, an analog or a digital user card need only check for "ones" on these four pins to determine if its chassis and slot have been addressed.

The remaining four bits are used for channel addressing on the card. An analog card may have up to 32 single-ended or 16 differential channels. Signals A8, A9, A10, and A11 choose one of 16 possible channels for each differential analog card; single-ended cards have two analog signals on the system analog bus for each address. Bit A12 is used by the signal processor to choose between these two analog signals to allow for 32 channel operation. Analog cards with only 8 channels would ignore A11; those with four channels would ignore A10 and A11, and those with one channel would ignore all four bits.

Digital cards use A8 through A11 differently. Since digital cards can have a maximum of four channels per card, they need only decode A8 and A9. A10 is not used by digital cards, but A11 has a special purpose. Certain digital addresses must cause a response on many cards in the system simultaneously, such as commands to sample-and-hold cards or interrupt vector inputs. To allow for "group" addressing during D/A address decoding, A11 is connected to the complement of the address register MSB. Consequently, A11 will be high during all normal digital input or output transactions, and this level must be sensed and decoded by all digital cards. Cards that respond to "group" addressing (e.g. SSH cards and interrupt cards) must sense a low on A11 during "group"commands.

Examples of the addressing structure have been provided earlier in this chapter in the "Front Panel Display and Control" section.

7.7.3 User Card Digital Bus

The ANDS5400 user card digital bus is a 16 bit, CMOS compatible, parallel, bidirectional, bus structure. It consists of signals D1 (MSB) through D16 (LSB) on the user card backplane. The bus is buffered and re-created in each expansion chassis and will drive up to 70 CMOS loads in any chassis.

7.7.4 User Card Analog Bus

The ANDS5400 user card analog bus consists of three lines, "EVEN," "ODD," and "SIGNAL RETURN." All analog measurements are based on the voltages placed on these bus lines by the input cards. The signal processors interpret the signals on these lines differently, depending on the type of measurement, single-ended or differential, being made. In the single-ended mode "even" addresses (0, 2, 4, etc.) cause measurements to be made between the signal return bus and the "even" bus; "odd" addresses (1, 3, 5, etc.) cause measurements to be made between the signal return line and the "odd" bus. In the differential mode all measurments are made between the "even" (+) and "odd" (−) buses. Although the signal return line is not used in measuring differential signals, it should be tied to a potential near ground since it is used during the auto-zero cycle of some signal processors. For this reason, the signal return line is strapped to ground on the rear panel of each chassis. This strap should be removed only if the signal return will be wired to a solid ground near the user's voltage sources. The "even" and "odd" analog buses are shielded from capacitively coupled interference by their placement between the analog ground and signal return etch.

7.7.5 Digital Control Lines

7.7.5.1 $\overline{CLR2}$

This CMOS compatible pulse is pulled low by a clear instruction from the interface or by pushing the front panel clear button. It is optional on all user cards, but it typically performs some kind of resetting function, such as clearing registers, opening relays, etc. Note that this line is called $\overline{CLR}$ on some user card schematics.

7.7.5.2 DIG STROBE

This CMOS compatible positive pulse serves to strobe digital data into registers on addressed cards. Since data validity is not guaranteed on the rising edge, the data should be loaded into the latches on the trailing edge of this pulse.

7.7.5.3 RDUSR

This CMOS compatible signal goes high during digital input transactions to allow addressed user cards to place their digital data on the system digital bus. Note that this signal is called DIG IN on some user card schematics.

7.7.5.4 $\overline{BOX\ REQUEST}$

This "wired-or" line is pulled low by any user card making a system interrupt request. The pull down line must sink 20mA at 0.5V.

7.7.5.5 PRIORITY IN

This low power Schottkey TTL compatible signal goes high to pass priority to each user card from J1 through J16 in conjunction with the PRIORITY OUT line. The highest priority user card requesting an interrupt will block the passage of the priority signal and place its vector on the bus during a DIG IN transaction with an address of 4000.

Note: Some older non-interrupting cards may not have the priority grant jumper between 15 & S. Therefore, care must be taken to ensure that this jumper is installed.

7.7.5.6 PRIORITY OUT

This low power Schottkey TTL output is driven high by any user card that receives PRIORTY IN and is not requesting an interrupt. User cards that do not use the interrupt capability at all must have priority IN and OUT wired together to avoid breaking the priority chain.

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Section 7.7
User Card Backplane

Card Number	Drawing Number	Title
—	D5-8653	User Card Backplane Wiring Table
—	D4-8653	User Card Backplane Fabrication
—	D7-8653	User Card Backplane Assembly

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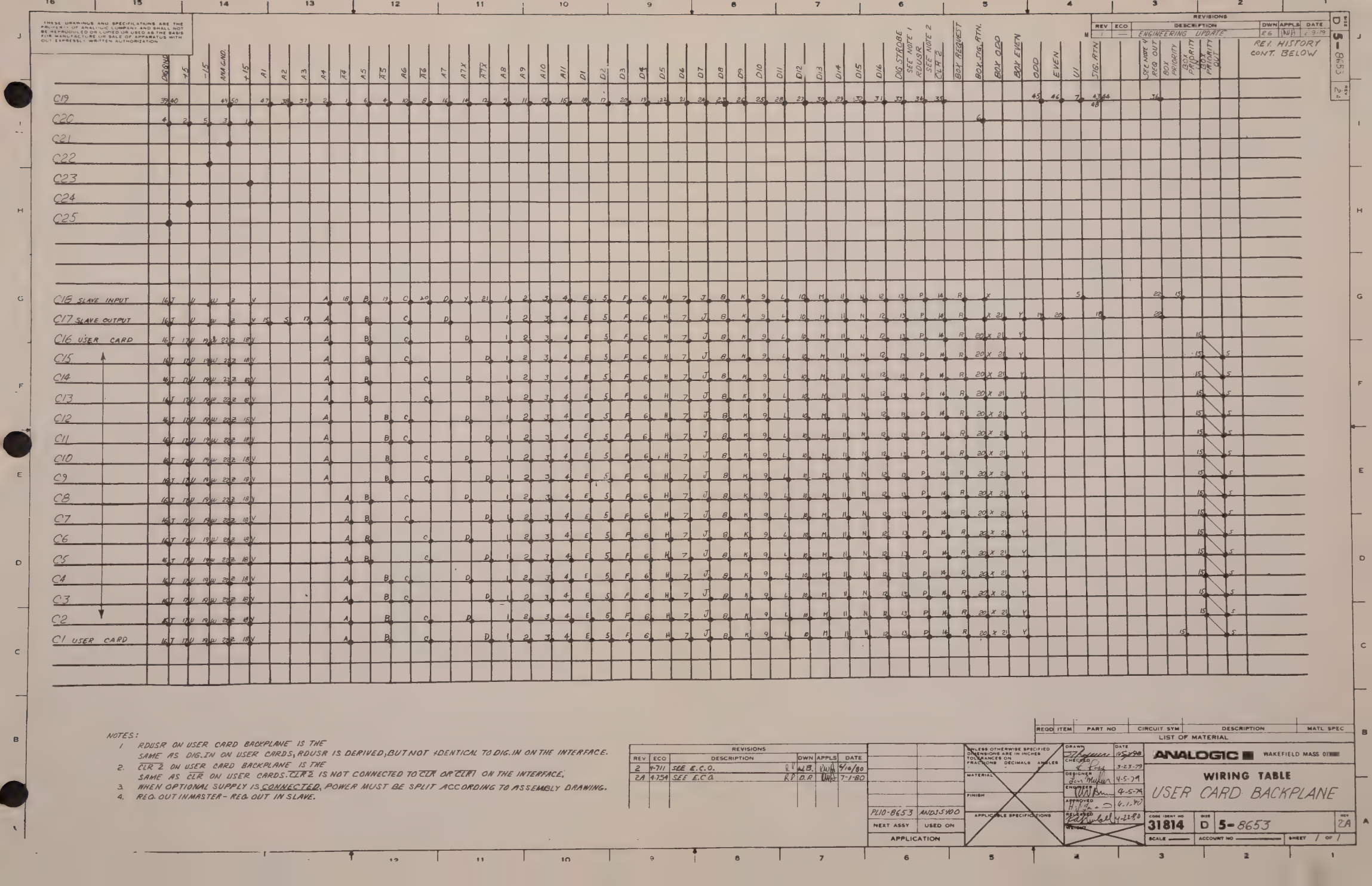
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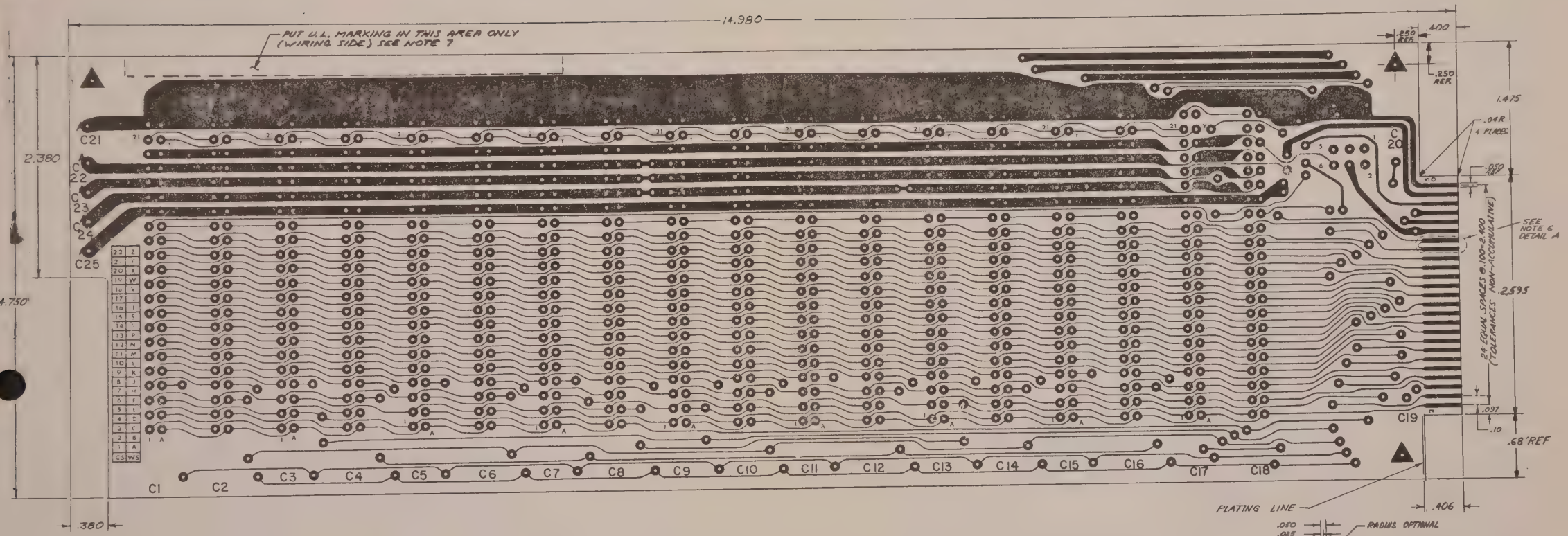
REVISIONS
REV ECO DESCRIPTION DWN APPLS DATE
1 — ENGINEERING UPDATE EG 9-19
REV. HISTORY CONT. BELOW
SIZE D 5-8653 REV 2A
DIGGND +5 -15 ANAGND +15 A1 A2 A3 A4 A4 A5 A5 A6 A6 A7 A7X A7X A8 A9 A10 A11 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 DIG STROBE SEE NOTE 1 RDUSR SEE NOTE 2 CLR 2 BOX REQUEST BOX SIG. ATN. BOX ODD BOX EVEN ODD EVEN U1 SIG. ATN SEE NOTE 4 REQ OUT BOX PRIORITY BOX PRIORITY OUT BOX PRIORITY OUT
C19
C20
C21
C22
C23
C24
C25
C18 SLAVE INPUT
C17 SLAVE OUTPUT
C16 USER CARD
C15
C14
C13
C12
C11
C10
C9
C8
C7
C6
C5
C4
C3
C2
C1 USER CARD
NOTES:
1 RDUSR ON USER CARD BACKPLANE IS THE SAME AS DIG.IN ON USER CARDS, RDUSR IS DERIVED, BUT NOT IDENTICAL TO DIG.IN ON THE INTERFACE.
2. CLR 2 ON USER CARD BACKPLANE IS THE SAME AS CLR ON USER CARDS. CLR 2 IS NOT CONNECTED TO CLR OR CLR1 ON THE INTERFACE.
3 WHEN OPTIONAL SUPPLY IS CONNECTED, POWER MUST BE SPLIT ACCORDING TO ASSEMBLY DRAWING.
4. REQ. OUT IN MASTER - REQ. OUT IN SLAVE.
REVISIONS
REV ECO DESCRIPTION DWN APPLS DATE
2 4-711 SEE E.C.O. WB. 4/10/80
2A 4-754 SEE E.C.O. RP D.R 7-1-80
PL10-8653 AND/SY00
NEXT ASSY USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN DATE 19-3-80
CHECKED 3-23-79
DESIGNER 4-5-79
ENGINEER 4-5-79
APPROVED 4-1-80
RELEASED 4-22-80
WEIGHT
REQD ITEM PART NO CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL
ANALOGIC WAKEFIELD MASS 01
WIRING TABLE
USER CARD BACKPLANE
CODE IDENT NO 31814 SIZE D 5-8653 REV 2A
SCALE ACCOUNT NO SHEET 1 OF 1

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APP'D	DATE
1	—	ENGINEERING UPDATE	[illegible]	[illegible]	2/8/79
2	4-711	SEE E.C.O.	[illegible]	[illegible]	5/17/80



WIRING SIDE

NOTES:
1. MATERIAL: GLASS EPOXY (FR4) DOUBLE SIDED, 2 OZ COPPER, GREEN .062 THK.
2. SOLDER TIN PLATE (60/40) .0005 -.0010 THK.
3. SOLDER MASK BOTH SIDES. [illegible] PLATING, OF THIS DRAWING. [illegible]
4. FINGERS TO BE PLATED UP TO PLATING LINE WITH .00002 NICKEL WITH AN OVERPLATING OF .00002 RHODIUM OR .00005 GOLD.
5. FABRICATE PER A2-1040.
6. KEY AS INDICATED
7. P.C. BOARD MANUFACTURER WILL BE U.L. APPROVED AND WILL MARK THIER U.L. CODE IDENTIFICATION & THE FLAMMABILITY RATING, EITHER UL-94V-01 OR UL-94V-02 (DEPENDING ON MATERIAL USED) ON THE WIRING SIDE OF THE BOARD IN THE AREA DESIGNATED.
8. HOLE LEGEND:

LTR.	SIZE	QTY.
C	.051-.057 AFTER PLATING	A/R
A	.067-.073 " "	5
B	.125 +.003 -.000 UNPLATED	3

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS ± 1/64, DECIMALS .XX ± .01, .XXX ± .005, ANGLES ± 1°

MATERIAL: SEE NOTE 1

FINISH: SEE NOTES 2 & 4

APPLICABLE SPECIFICATIONS: A2-1040

PL10-8653 | AND8540D0

NEXT ASSY | USED ON

APPLICATION

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	DRAWN	DATE
CHECKED	[signature]	2-20-79
DESIGNER	[signature]	4-5-79
ENGINEER	[signature]	4-5-79
APPROVED	[signature]	4-1-80
QUALITY	[signature]	4-22-80

WEIGHT

ANALOGIC WAKEFIELD, MASS. 01880

FABRICATION
USER CARD BACKPLANE

CODE IDENT NO. 31813 | SIZE D | 4-8653 | REV. 2

SCALE 1/4 | ACCOUNT NO. | SHEET 1 OF 1

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
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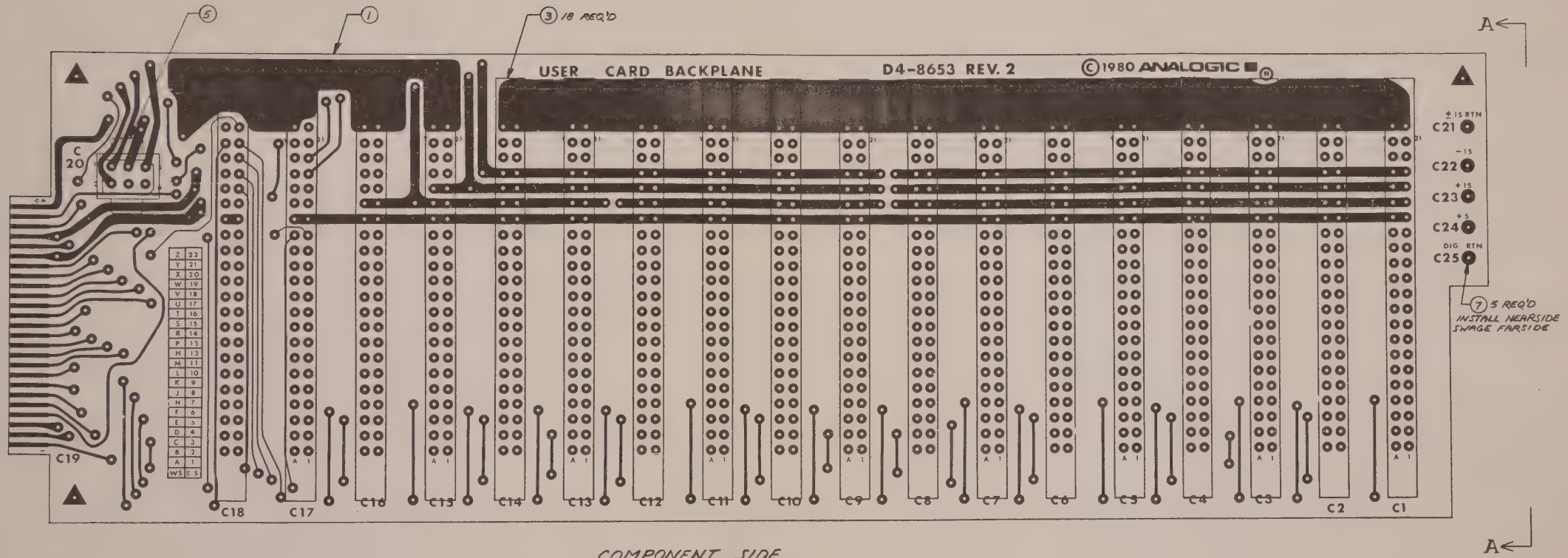
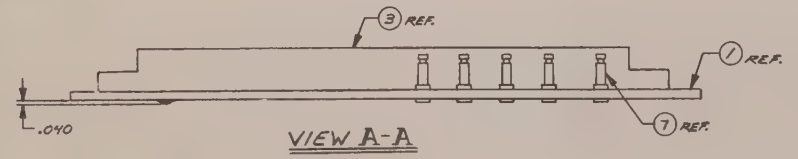
D 7-8653 REV 2



COMPONENT SIDE

NOTES:
1. FOR WIRING TABLE SEE D5-8653
2. ASSEMBLE IN ACCORDANCE WITH A2-1027



VIEW A-A

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS ANGLES X = .XX ± XXX ±	DRAWN L. REPPUCCI	DATE 8/14/78	ANALOGIC WAKEFIELD, MASS. 01880
			CHECKED R. ROSS	8/20/79	ASSEMBLY USER CARD BACKPLANE
		MATERIAL	ENGINEER LAN MULLER	9/4/79	
			ENGINEERING MGR R.W.L.N.	9/5/79	
		FINISH	QUALITY CONTROL N. LARSON	9/24/80	
PL10-8653	AN055400	APPLICABLE SPECIFICATIONS A2-1027	PRODUCTION L. KIMBALL	9/22/80	CODE IDENT NO 31814 SIZE D 7-8653 REV 2
NEXT ASSY	USED ON		WEIGHT		SCALE 2/1 SHEET 1 OF 1
APPLICATION					

7.8 Expansion Cards

7.8.0 General

The index of the drawings and schematics in this section follows section 7.8.2.2.

7.8.1 AC333 Expansion Card Theory of Operation

In the master chassis the AC333 expansion card set plugs into slots J17 and J18 and serves to select the correct chassis (master or expansion) for analog and digital transactions. Refer to schematic D5-8637 in this section, which depicts both boards, AC333-1 and AC333-2, that form the AC333 assembly.

Refer to drawings D7-8637 and D7-8638 in this section. Note that the AC333-1 board has six small connectors labeled J1 through J6, and an additional connector J7 is on AC333-2. These connectors are cabled to the analog outputs of each expansion chassis as chassis are added to the system. Thus, the AC333 can choose the source of the analog signals "even," "odd," and "signal return," which are fed to the signal processor card and then to the A/D converter. The solid state analog multiplexers Z1, Z2, and Z3 are each used to select from one of eight sources for their respective signals. Pin 13 on each multiplexer looks at the analog bus signals from the master chassis; pin 11 looks at signals from the first expansion chassis; pin 10 from the second expansion chassis; and so forth until pin 5, which looks at the last expansion chassis through connector J7.

The three bits A1, A2 and A3, representing the upper three bits of the 12 bit analog address word, form an octal digit that ranges from 0 to 7 to select from chassis 0 (master) to chassis 7 (last expansion chassis).

Resistor networks RN1 through RN6 serve as current limiting resistors that protect the multiplexers from damage in the event of an overscale input voltage. The transistor circuit built from Q1, Q2, Q3, and Q4 produces two stable voltages at + 12 and − 12 volts, which are applied to diode clamps located on each of the analog lines that go to the signal processor card. The diode clamps protect the signal processor card from overload by preventing the analog lines from exceeding 13 volts under any conditions.

The AC333-2 card contains the digital section of the expansion structure. The address bits generated from the address register on the front panel enter the expansion card as A1 through A11 and represent the top 11 bits of the 12 bit analog address word. A12, the LSB of the analog address word, goes only to the signal processor card, where it is used in channel selection during single-ended operation. Address bits A1, A2 and A3 are read from the user card backplane by the AC333-1 card; they are used for multiplexer control and are cabled to the AC333-2 card, where they join the other address bits and are buffered by high impedance 8837 inverting receivers. Bits A4 through A11 then drive 8833 non-inverting power drivers that drive the expansion bus going to all the expansion chassis. Bits A1, A2, and A3 go to decoder Z19, which connects the upper octal digit of the address word to its eight states denoted as $\overline{U0}$ through $\overline{U7}$. The $\overline{U1}$ through $\overline{U7}$ states pass through power drivers then on to the expansion bus for the expansion chassis. Each one of these states represents one of the chassis; U0 is the master chassis and U7 the last expansion chassis.

Most of the IC's on the AC333-2 card form a bidirectional bus translator for the 16 bit digital bus in the ANDS5400. The 16 bit CMOS bidirectional digital bus of the master chassis, made up of bits D1 (MSB) through D16 (LSB), goes to the interface, front panel, and user cards. Bits D1' through D16' form the 16 bit bidirectional power bus that goes to all the expansion chassis. The translator operates in one of two modes controlled by the XMIT/RCV line, which comes from Z6 pin 8. When this line is high, the translator transmits the information from the master chassis digital bus to the expansion chassis and brings the power level up from the CMOS bus in the master chassis to that of the power bus used by the expansion chassis. When the XMIT/RCV line is low, the translator listens to the expansion bus and drives the CMOS bus in the master chassis.

7.8.1.1 Typical Operation

We can follow a typical bit through the translator to see how the power level is shifted. In the XMIT mode D1 comes in on pin E of the user card backplane and looks into a disabled 80C96 tri-state driver and an 8837 high impedance receiver; the 8837 drives an enabled 8834 tri-state driver, which goes to pin 49 of the expansion bus cable. In the RCV mode the driver portion of the 8834 is disabled, while its receiver section "listens" to the expansion bus being driven by one of the expansion chassis. The output of this receiver has a pull-up from RN1 to ensure compatibility with the input of the 80C96. Finally, the 80C96, which is now enabled, drives the CMOS digital bus in the master chassis.

IC Z6, an AND/OR gate, controls the XMIT/RCV line. The translator is always in the XMIT mode (driving toward the expansion chassis) unless the master chassis is not being addressed AND address bit A11 is high AND a digital input cycle is underway; OR the master chassis is not requesting an interrupt AND bit A11 is low AND a digital input cycle is underway. Only under one of these two conditions will the translator go into the RCV mode, where it "listens" to the expansion chassis. The first of the two conditions represents a normal digital input cycle, where the card being addressed is beyond the master chassis; the second condition occurs when the computer controlling the ANDS5400 is trying to read the vector from the highest priority interrupting user card that is not in the master chassis.

The three signals DIG IN, DIG STROBE, and $\overline{CLR}$ from the master chassis are monitored by 8837 receivers that drive 8833 power drivers going to the expansion bus. The inverted signals on the expansion bus are then called $\overline{DIG\ IN}$', $\overline{DIG\ STROBE}$', and CLR'.

7.8.1.2 Interrupt Structure

The remaining logic on the AC333-2 board is primarily involved with the ANDS5400 interrupt structure. $\overline{BOX\ REQUEST}$ is the line from the master chassis user card bus that, when pulled low, indicates that one of the user cards in the master chassis is requesting an interrupt. $\overline{REQ\ IN}$ is the line from the expansion bus that, when pulled low, indicates that a user card in one of the expansion chassis is requesting an interrupt. Both inputs have pull-ups on them so that the lines will be high if no cards are requesting interrupts or if no expansion cards nor expansion chassis are installed. If a request is made by the master chassis or an expansion chassis, Z7 pin 11 will be high. This signal will normally pass through Z1 to drive the REQUEST output high. The REQ OUT signal goes to the ANDS5400 interface then back to the computer to indicate a user card request. Z1 is blocked only while a user card vector is being read.

The REQ OUT signal is blocked during the reading of a vector to create a new rising edge of the REQ OUT line if more that one user card is interrupting. If only one card

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is requesting an interrupt, the REQ OUT line goes down while the vector is being read; however, the act of reading the vector removes the request so that when the block is removed, the REQ OUT line stays low. If more then one card is requesting, the REQ OUT line will rise after the first vector is read, triggering the interface to create another interrupt to the computer.

The act of reading a vector is sensed by Z1, which detects a digital input cycle occuring when A11 is low. This condition corresponds to a digital input with an address of 4000. When a vector is being read, Z1 creates a rising edge on Z8's clock input, latching the current state of the request line of the master chassis. At this point, if the master chassis is requesting an interrupt, pin 8 of Z8 will be high. Now, the BOX PRIORITY line, which is used only in the master chassis, goes high and daisy-chains down through the user cards until it reaches the highest priority interrupting user card in the master chassis. As a result, that particular user card puts its vector on the digital bus to be read by the computer. If the master chassis is not requesting an interrupt, Z8 pin 9 goes high, causing PRIORITY OUT to go high, and this signal goes on the expansion bus to the appropriate expansion chassis. Z8 pin 9 also goes to the translator to put it in the RCV mode, so the vector from the expansion chassis can be driven onto the master chassis digital bus and read by the computer. The short delay created by R2 and C15 prevents spurious noise on the request line from causing artificial interrupts. The delay caused by R1 and C14 has two purposes: it prevents the establishment of priority signals until Z8 has settled, and it allows flip-flops like Z8, which are in every expansion chassis, to settle before priority is established.

7.8.2 AC334 Expansion Chassis Expansion Card Theory of Operation

In the expansion chassis the AC334 expansion card set plugs into slots J17 and J18 of the expansion chassis and serves to receive and transmit analog and digital information to the master chassis. Refer to schematic D5-8636, which depicts both the boards, AC334-1 and AC334-2, that form the AC334 assembly.

The AC334-1 card serves two functions; it is a connector board for the expansion bus, and it has the analog buffers that drive the expansion analog signals back to the master chassis. The connector board has a 50-pin connector, J2, that attaches to the cable coming from the master or the preceding expansion chassis. Most of the signals from this connector go to a 40-pin, permanently attached cable that connects to the AC334-2 board. Some of the grounds in the expansion bus are connected to AC334-1. The $\overline{\text{REQ OUT}}$ signal, which comes from the AC334-2 board, is interconnected through pin 22 of the user card backplane.

Z1 and Z2 are analog amplifiers that buffer the ODD and EVEN analog buses in the expansion chassis and drive shielded cable that goes back to the master chassis. R5 and R2 are the offset adjustment pots for the amplifiers. The RC networks on the amplifier outputs prevent oscillation while driving the analog cables. The signal return pin from the analog connector goes directly to the signal return line on the user card backplane and from there to the signal return post on the rear of the chassis.

The AC334-2 card contains the digital section of the expansion structure. The address bits that are generated from the master chassis enter an expansion card on an expansion chassis as $\overline{A4}$' through $\overline{A11}$'. These bits are received by 8837 high impedance receivers whose outputs are pulled up by RN2 to be CMOS compatible. The resulting signals, A4 through A11, go directly to the user card backplane, where they drive the user cards in the expansion chassis. Three sections of Z7 are used to invert A4', A5', and A6' to supply the complement of these signals to the user card backplane. A7 is split into its true and complement forms and gated against U1 to create A7X and $\overline{A7X}$. Thus, these two signals are both low unless the expansion chassis is being addressed. Refer to the "User Card Backplane" section of this chapter for details on how these address bits are used by the user cards.

The "U" lines from the master chassis go low to activate each expansion chassis as it is addressed. These lines are received by the connector on the AC334-1 card and cabled to the AC334-2 card, where they exit from connector P2 and go to the next expansion chassis. The "U" lines are labeled $\overline{U1}$ through $\overline{U7}$ when they enter the expansion chassis and $\overline{U1}$' through $\overline{U7}$' as they leave for the next expansion chassis. There is NOT a direct correspondence between the lines as they enter and as they leave, because of a twisting process implemented before they go to next expansion chassis. The effect of this twisting process is shown in Figure 7-12. Basically, when these lines leave the master chassis, U1 through U7 represent expansion chassis 1 through 7, respectively. The first expansion chassis connected to the the expansion bus accepts the U1 line and twists the "U" bus so that U2 occupies the U1 position on the bus. The next expansion chassis does the same thing, accepting U2 and putting U3 in the U1 position. Each expansion chassis continues the process so that the seventh chassis accepts U7. As a result, each expansion chassis assumes the appropriate location in the address table without the use of adddress jumpers or switches.

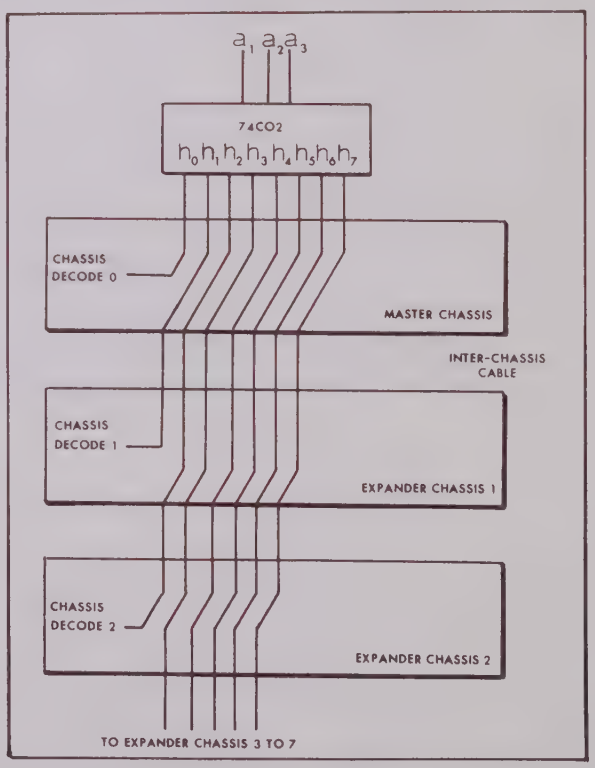

Figure 7-12. Chassis Address Decoding

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Most of the IC's on the AC334-2 card form a bidirectional bus translator for the 16 bit digital bus in the ANDS5400. Bits D1 (MSB) through D16 (LSB) form the 16 bit CMOS bidirectional digital bus of the expansion chassis. Bits D1' through D16' form the 16 bit bidirectional power bus that comes from the master chassis. The translator operates in one of two modes controlled by the RCV/XMIT line from Z12 pin 8. When this line is high, the translator receives the information from the expansion cable digital bus and puts it on the expansion chassis user card bus, while lowering the power level to that of the CMOS bus in the expansion chassis. When the RCV/XMIT line is low, the translator "listens" to the expansion chassis user card bus and drives the power bus going to the master chassis.

7.8.2.1 Typical Operation

We can follow a typical bit through the translator to see how the power level is shifted. During the RCV mode D1' comes in on pin 49 of the connector on the AC334-1 and is cabled over to the AC334-2. It then looks into a disabled 8834 tri-state driver and its receiver section. It exits on pin 49 of P2 on the AC334-2 board and goes to the next expansion chassis. The 8834 receiver section has a pull-up on its output to assure compatibility with the 80C96, which is enabled and drives D1 on pin E of the user card backplane in the expansion chassis.

During the XMIT mode the driver portion of the 80C96 is disabled while the 8837 receiver "listens" to the user card backplane, which is being driven by one of the cards in the expansion chassis. The 8837 receiver output goes to the enabled 8834 power driver, which drives the expansion bus to the master chassis.

IC Z12, an AND/OR gate, controls the RCV/XMIT line. The translator is always in the RCV mode ("listening" to the master chassis bus output from AC333), unless the expansion chassis is being addressed AND address bit A11 is high AND a digital input cycle is underway; OR when this expansion chassis requests an interrupt AND bit A11 is low AND a digital input cycle is underway AND that expansion chassis has interrupt priority. Only under one of these two conditions will the translator go into the XMIT mode, where it "listens" to the expansion chassis user card bus and transmits this information to AC333 in the master chassis. The first of these conditions represents a normal digital input cycle, where the card being addressed is in a certain expansion chassis; for the purposes of this example, assume this expansion chassis is in the middle of the expansion bus. The second condition occurs when the computer controlling the ANDS5400 is reading the vector from the highest priority interrupting user card in this expansion chassis.

The three signals $\overline{\text{DIG IN}}$', $\overline{\text{DIG STROBE}}$', and CLR' from the master chassis are monitored by 8837 receivers that have pull-ups on their outputs for CMOS compatibility. These outputs directly drive the user cards in this expansion chassis. The signals on the user card bus are then called DIG IN, DIG STROBE, and $\overline{\text{CLR}}$.

7.8.2.2 Interrupt Structure

The remaining logic on the AC334-2 board is primarily involved with the ANDS5400 interrupt structure. $\overline{\text{BOX REQUEST}}$ is the line from this expansion chassis user card bus that, when pulled low, indicates that a user card in this expansion chassis is requesting an interrupt. $\overline{\text{REQ IN}}$ is the line from the expansion bus that, when pulled low, indicates that a user card in an expansion chassis farther down the expansion bus is requesting an interrupt. Both inputs have pull-ups on them so that the lines will be high if no cards are requesting or if no additional expansion boxes are installed. If this expansion chassis or one farther down the line requests an interrupt, Z16 pin 8 will be low. This signal will be channeled upstream to drive the REQUEST line high in the master chassis. This REQUEST line goes to the ANDS5400 interface then back to the computer to indicate a user card request.

The act of reading a vector is sensed by Z6 pin 3, which detects a digital input cycle occuring when A11 is low. This condition corresponds to a digital input with an address of 4000. When a vector is being read, Z8 pin 10 creates a rising edge on Z11's clock input, latching the current state of the request line in that expansion chassis with the user card corresponding to this vector. At this point, if this expansion chassis is requesting an interrupt, pin 6 of Z11 will be high. Now, the PRIORITY OUT line, coming from the master chassis, goes high and daisy-chains down through the expansion chassis (assuming they are not requesting interrupt service) until it reaches the PRIORITY IN input of this expansion chassis. Now, the BOX PRIORITY line in this expansion chassis will go high and daisy-chain down through the user cards until it reaches the first one that is requesting interrupt service. As a result, that particular user card will put its vector on the digital bus to be read by the computer.

If this expansion chassis is not requesting an interrupt, Z11 pin 5 will go high, causing PRIORITY OUT to go high on the expansion bus, and this signal goes to the next expansion chassis down the line.

R6 and C21 function as a noise filter to prevent spurious interrupts from occuring if any digital noise couples into the chassis interrupt request bus.

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Section 7.8
Expansion Cards

Card Number	Drawing Number	Title
AC333	D5-8637	Master Chassis Expansion Card Schematic
—	C7-1546	Expansion Module Assembly
AC333-1	D7-8637	Master Chassis Expansion Card Board 1 Assembly
AC333-2	D7-8638	Master Chassis Expansion Card Board 2 Assembly
AC334	D5-8636	Expansion Chassis Expansion Card Schematic
AC334-1	D7-8635	Expansion Chassis Expansion Card Board 1 Assembly
AC334-2	D7-8636	Expansion Chassis Expansion Card Board 2 Assembly

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J18 AC 333-2

J17 AC 333-1

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR	DATE
1	—	ENG UPDATE	[illegible]		11-28-78
2	4-557	SEE E.C.O.	D.P.		12-20-79
3	4-652	SEE E.C.O	D.P.		3-17-80
4	4-725 4-754	SEE E.C.O.'S	D.P.		7-2-80

SIZE D | 5-8637 | REV 4

POWER PINS			
REF DES	I.C. TYPE	+5	DIG GND
Z1	74LS08	14	7
Z3,9,10	8834	16	7,8
Z4,5,11,12,14	8833	16	1,8,9
Z6	74LS51	14	7
Z7	74LS00	14	7
Z8	74LS74	14	7
Z13,15,16, 17,18,23	8837	16	1,8,9
Z19	7442	16	8
Z20,21,22	8DC96	16	8
RN1		16	8

NOTES:
1. FOR ASSEMBLY SEE D7-8638.

NOTES:
1. FOR ASSEMBLY SEE D7-8637.
2. ALL DIODES ARE IN4148.

J1 TO SLAVE BOX 1
J7 TO SLAVE BOX 7

= DAUGHTER BOARD
= EXP BUS
= MOLEX CONN
= RIBBON CABLE

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-8638	AC333-2				
PL10-8637	AC333-1				
NEXT ASSY	USED ON				
APPLICATION					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON FRACTIONS DECIMALS ANGLES ± ± ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
WEIGHT

DRAWN	RWH	3-30-78
CHECKED	[illegible]	10-27-78
DESIGNER	[illegible]	10-27-78
ENGINEER	[illegible]	10-27-78
APPROVED	[illegible]	4-22-80
QUALITY	[illegible]	4-22-80

ANALOGIC WAKEFIELD, MASS. 01880

SCHEMATIC
MASTER BOX EXPANSION
AC333

CODE IDENT NO. 31819 | SIZE D | 5-8637 | REV 4
SCALE NONE | ACCOUNT NO. | SHEET 1 OF 1

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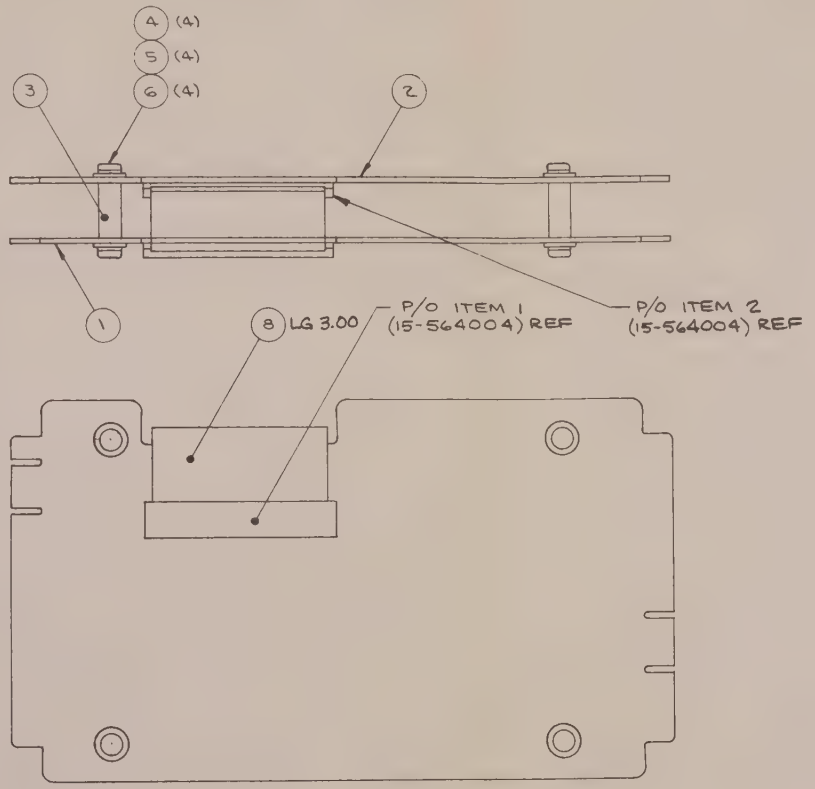
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE
M					

SIZE C 7-1546 REV O



NOTES

1. ASSEMBLE ITEM 8 TO ITEMS 1 & 2 USING HAND PRESS 3M# 3440, LOCATER PLATE 3M# 3443-8, PLATEN 3M# 3442-1 (SETTING ON 3M GAUGE # 3436-1 & 3)

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-5814	AC334
PL10-5813	AC333
PL10-3726	AN5400
PL10-3059	AN5400
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS DECIMALS ANGLES
. : .12 :

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

		DATE
DRAWN	WM L McKINLEY	5 FEB 76
CHECKED	RH	6 AUG 76
DESIGNER	R Shivain	6 FEB 76
ENGINEER	DW Adams	8-6-76
APPROVED	KAJ	
RELEASED		8/9/76
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

EXPANSION MODULE ASSY

CODE IDENT NO	SIZE		REV
31814	C	7-1546	O
SCALE 1/1	ACCOUNT NO	SHEET 1 OF 1	

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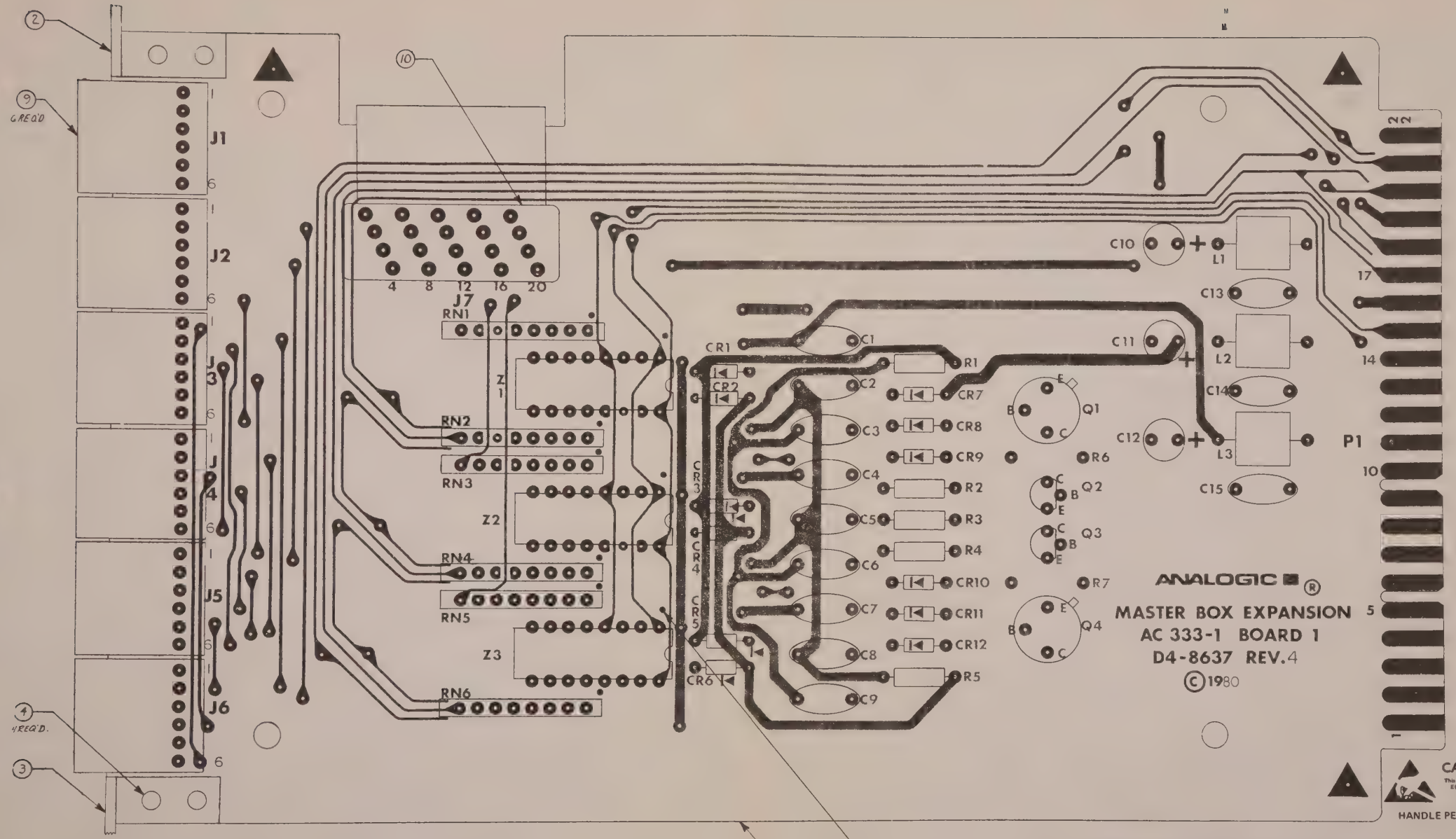


NOTES:
1. FOR SCHEMATIC SEE D5-8637.
2. DOT INDICATES PIN 1 OF IC'S & R.N.'S.
3. ASSEMBLE PER A2-1021.

SEE NOTE 2

COMPONENT SIDE

REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPLS	DATE	
2	M-557	SEE E.C.O.	RP	D.P	12-20-79	
3	M-632	SEE E.C.O.	RP	D.P	3-17-80	
4	M-725	SEE E.C.O.	RP	D.P	7-2-80	

SIZE D 7-8637 REV 4

PL10-8637	AC 333-1	
NEXT ASSY	USED ON	
APPLICATION		

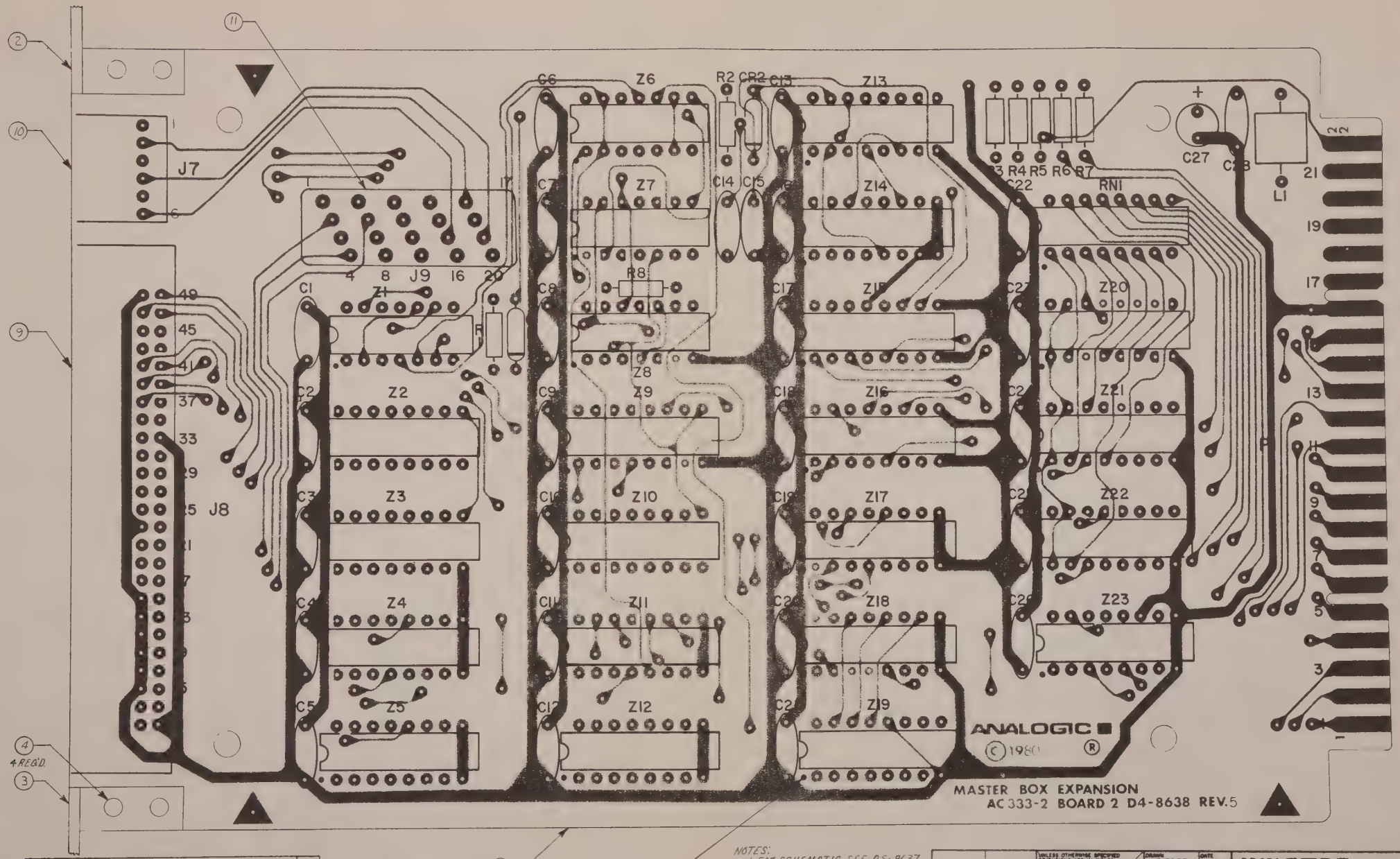
DRAWN P.PFEFFER 10-27-78
CHECKED R.ROSS 10-27-78
ENG APPR L.MULLER 10-27-78
MANUFACTURING APPR
QUALITY CONTROL
PURCHASING APPR
WEIGHT

ANALOGIC WAKEFIELD, MASS 01880

ASSEMBLY
MASTER BOX EXPANSION
AC 333-1 BOARD 1

CODE IDENT NO	SIZE	DWG NO	REV
31814	D	7-8637	4

SCALE 4:1 SHEET 1 OF 1



REVISIONS						
REV	ECO	DESCRIPTION	DWN	APPLS	DATE	
3	9-558	SEE ECO	DP		12-27-79	
4	9-652	SEE ECO	DP		3-17-80	
5	9-725	SEE E.C.O.	D.A.		7-2-80	

D 7-8638 REV 5

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

NOTES:
1. FOR SCHEMATIC SEE D5-8637.
2. DOT IND. CATES PIN 1 OF I.C.'S & R.N.'S.
3. ASSEMBLE PER A2-1027.

PL10-8638	AC 333-2	
NEXT ASSY	USED ON	
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON: DECIMALS .X ±.1, .XX ±.05; ANGLES ±2°. MATERIAL. FINISH. APPLICABLE SPECIFICATIONS. WEIGHT.

DRAWN R. PERRY 10-22-78
CHECKED R. ROSS 10-26-78
ENGINEER L. MULLER 10-27-78
ENGINEERING MGR. R. HAVENER 10-27-78
QUALITY CONTROL 11-6-78
PRODUCTION 11-21-78

ANALOGIC, WAKEFIELD, MASS. 01880

ASSEMBLY
MASTER BOX EXPANSION
AC 333-2 BOARD 2

CODE IDENT NO. 31814 SIZE D 7-8638 5
SCALE 4/3 SHEET 1 OF 1

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(FROM NEXT SLAVE) J18

AC 334-2

TWIST BUS

POWER PINS			
REF DES	I.C. TYPE	+5	GND
Z1,2,3,4	8834	16	7,8
2,5,7,9,13	8837	16	7,8,9
14,17,18			
Z6	74LS00	14	7
Z9,10,15	80C96	16	8
Z11	74LS74	14	7
Z12	74LS51	14	7
RN1,2,3	RES NET	16	8

8834's GND PIN 7

8837's 80C96's GND PIN 7+9

P1 P2 P3

D1' D2' D3' D4' D5' D6' D7' D8' D9' D10' D11' D12' D13' D14' D15' D16'

Z1 Z2 Z3 Z4 Z5 Z6 Z7 Z8 Z9 Z10 Z11 Z12 Z13 Z14 Z15 Z16 Z17 Z18

RN1 RN2 RN3

SPARES

A4' A5' A6' A7' A8' A9' A10' A11'

A4 A5 A6 A7 A8 A9 A10 A11

DIG STROBE

CLR'

DIG IN

PRIORITY IN

PRIORITY OUT

BOX REQUEST

BOX PRIORITY

REQ. IN

REQ. OUT

MORE SPARES

TO 8834's PIN 9

TO 80C96's PINS 1 & 15

R1 100

R2 1K

R3 10K

R4 1K

R5 1K

R6 100

R7 1K

C1-C13, C16-C19 .15μF

C20 15μF

C21 680pF

C14 NOT USED

C15 NOT USED

CR1 1N4454

74LS51

74LS74

80C96

8837

CAUTION

This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES

HANDLE PER A2-1058.

NOTES:
1. FOR ASSEMBLY SEE D7-8636
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE, 1/4W, 5%, C.C. ALL CAPS ARE .01μF

AC334-2

J17 (TOWARD MASTER)

AC 334-1

PRIORITY IN

REQ. IN

REQ. OUT

= DAUGHTER BOARD

= EXP BUS

= RIBBON (TO J18)

= MOLEX CONN

R1,1K R2,100K R3,1K

R4,1K R5,100K R6,1K

R8 100

R9 100

R7 100

C8 56pF

C7 56pF

C11 22pF

C12 60pF

C9 60pF

C10 .01

C5 .01

C1 .01

BOX EVEN

BOX ODD

BOX SIG. RTN.

BOX EVEN

ANA. RTN.

BOX ODD

ANA. RTN.

BOX SIG. RTN.

ANA. RTN.

NOTES:
1. FOR ASSEMBLY SEE D7-8635
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS, 1/4W, 5%, C.C. ALL CAPS .01μF

AC334-1

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR	DATE
2	4-0373	SEE E.C.O.	D.P.	LM	1-7-79
3	4-525	SEE E.C.O	D.P.	RWH	2-9-79
4	4-560	SEE E.C.O.	D.P.	RWH	1-7-80
5	4-652	SEE E.C.O	D.P.	RWH	3-14-80
6	4-725 4-754	SEE E.C.O	D.P.	RWH	7-3-80

D 5-8636 6

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-8636	AC-334-2
PL10-8635	AC-334-1
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± ± ±

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

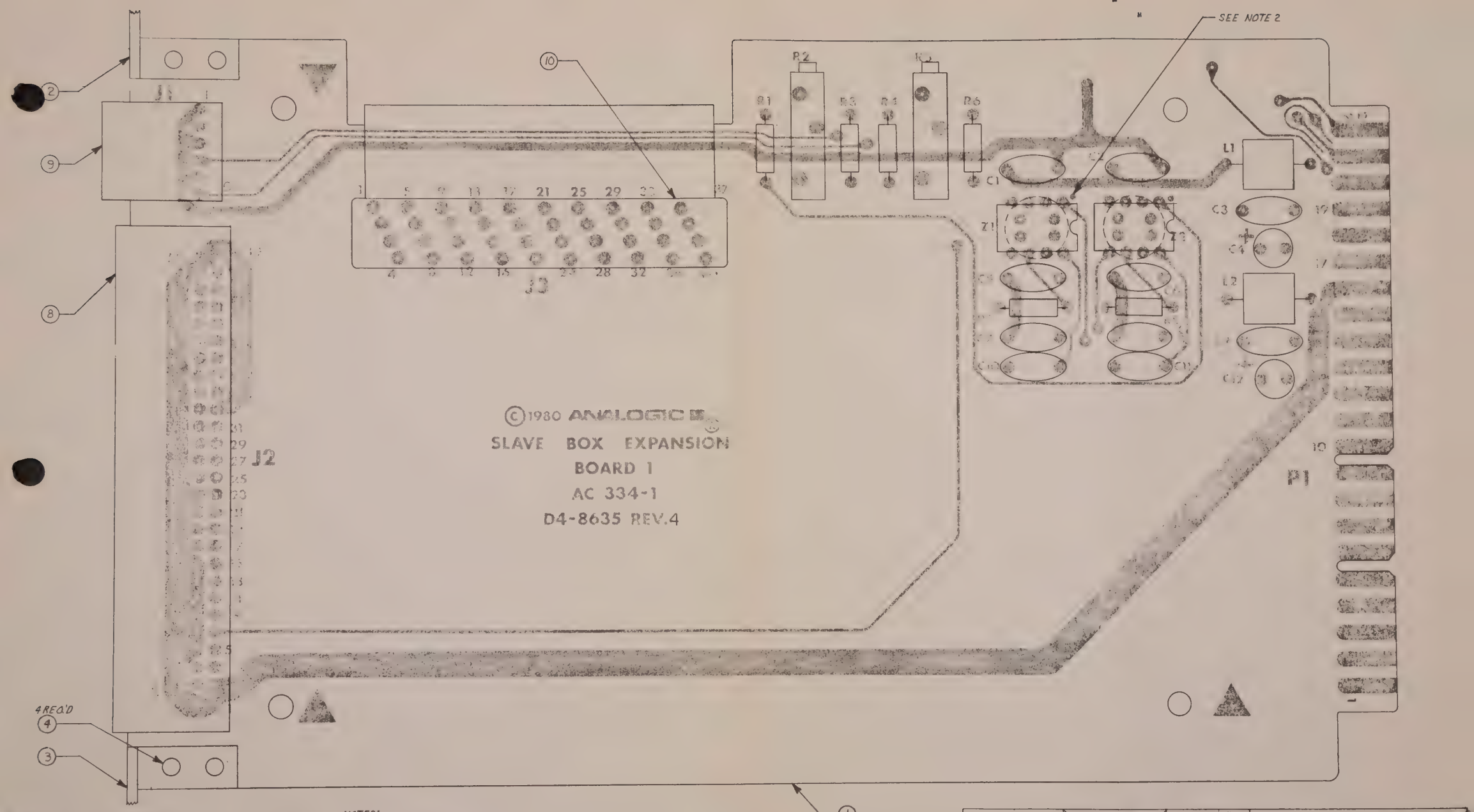
DRAWN	RWH	DATE 5-20-78
CHECKED		8-8-78
DESIGNED		10-27-78
ENGINEER		10-27-78
APPROVED		4-22-80
RELEASED		4-22-80
MFG/MKT		

ANALOGIC WAKEFIELD, MASS 01880

SCHEMATIC
SLAVE BOX EXPANSION
AC334

CODE IDENT NO. 31814 | SIZE D | 5-8636 | REV 6

SCALE — | ACCOUNT NO. | SHEET 1 OF 1



REVISIONS				
CO	DESCRIPTION	DWN	APPLS	DATE
559	SEE E.C.O.	DR		1-2-80
632	SEE E.C.O.	DR		3-14-80
4 4 725	SEE E.C.O.	D.R		7-3-80

D 7-8635 REV 4

NOTES:
1. FOR SCHEMATIC SEE D5-8636.
2. DOT INDICATES PIN 1 OF I.C.'S.
3. ASSEMBLE PER A2-1027.

COMPONENT SIDE

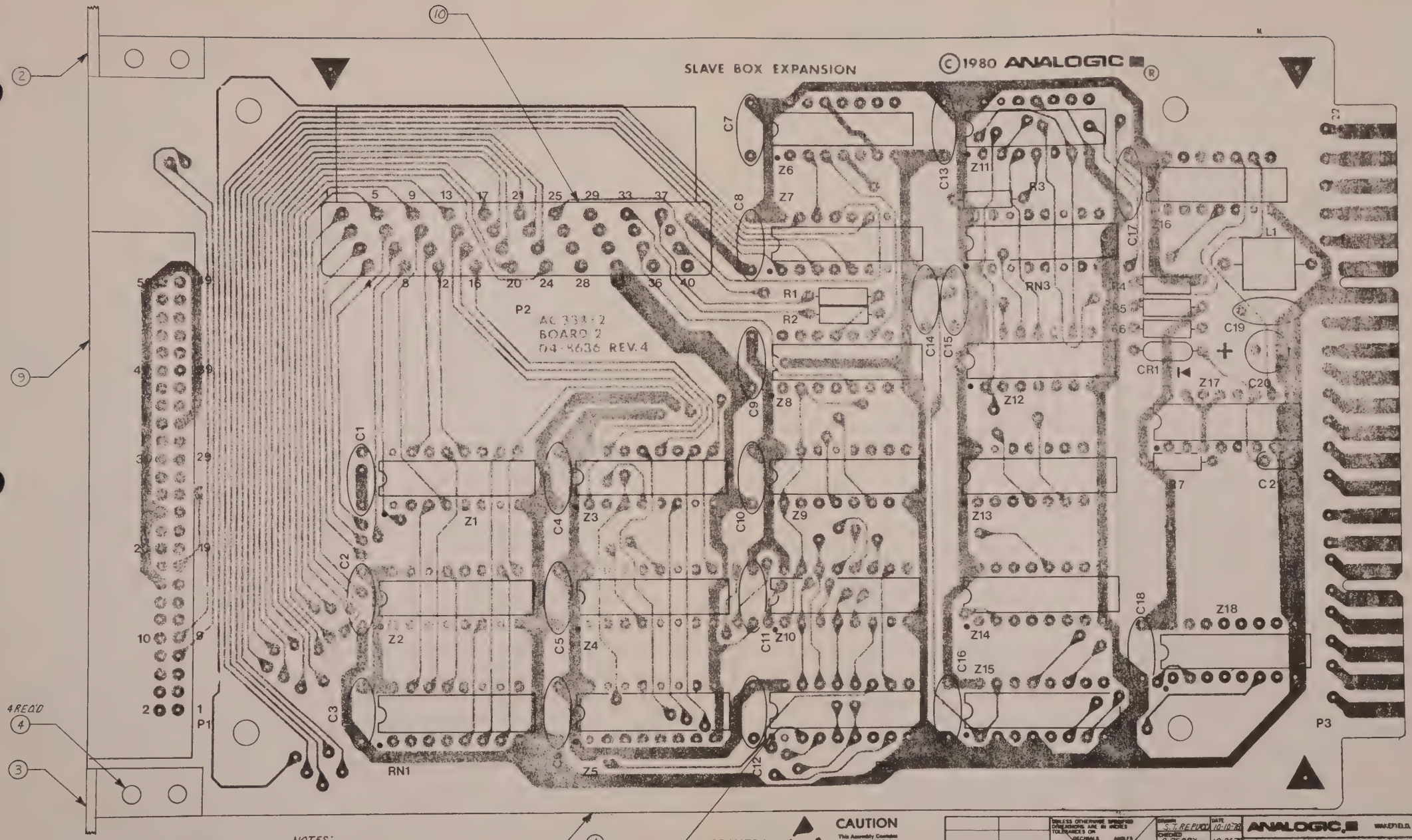
		J. LASPINA	3-30-78
		R. PERRY	10-25-78
		L. MULLER	10-27-78
		R. HAVENER	10-27-78
			4-22-78
			4-22-78

PL10-8635 AC334-1
NEXT ASSY | USED ON
APPLICATION

ANALOGIC — WAKEFIELD, MASS 01880

ASSEMBLY
SLAVE BOX EXPANSION
AC 334-1 BOARD 1

31814	D 7-8635	4
SCALE 4:1		SHEET 1 OF 1



REVISIONS				
ECO	DESCRIPTION	DWN	APPLD	DATE
4-360	SEE E.C.O.	RP	DP	1-7-80

NOTES:
1. FOR SCHEMATIC SEE D5-8636.
2. DOT INDICATES PIN 1 OF I.C.'S & R.N.'S.
3. ASSEMBLE PER A2-1027.

COMPONENT SIDE

CAUTION
This Assembly Contains ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058.

PL10-8636	AC 334-2
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .x ±.1 .xx ±.01 .xxx ±.005
ANGLES ±1°
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN	S.T. REPUCCI	DATE 10-10-78
CHECKED	R. PERRY	10-26-78
ENGINEER	L. MULLER	10-27-78
MANUFACTURING AREA	R. MAVENER	10-27-78
QUALITY CONTROL	W.P. Lawson	4-22-80
APPROVED	T.K. Gallo	4-22-80
WEIGHT		

ANALOGIC, WAKEFIELD, MASS. 01880

ASSEMBLY
SLAVE BOX EXPANSION
AC 334-2 BOARD 2

CAGE CODE NO	DWG. NO	REV
31814	D 7-8636	4
SCALE 4:1		SHEET 1 OF 1

Section 7.9
Power Supplies

Card Number	Drawing Number	Title
AN3007	—	AN3007 Power Supply Data Sheet
—	C5-7420	Power Supply Schematic
—	D7-1537	Power Supply Wiring Table
—	D7-7421	Power Supply 5 Volt Section Assembly
—	D7-7422	Power Supply 15 Volt Section Assembly

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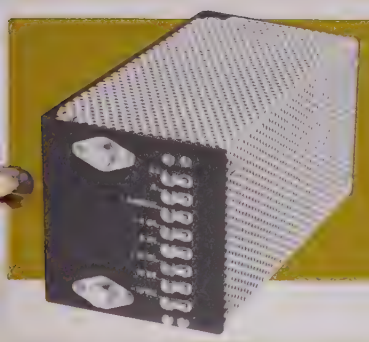


AN3007

High Efficiency, Well-Regulated High Power, AC/DC

CHASSIS MOUNTED POWER SUPPLY

DESCRIPTION

The Analogic AN3007 is an advanced high-performance, well-regulated, ac-to-dc power supply that furnishes +5, +15, and −15Vdc for energizing complete analog and/or digital data conversion modules, instruments, and systems. This power supply uniquely combines a shielded isolation transformer, a sophisticated ±15V linear regulator, and a state-of-the-art +5V switching regulator to provide highly efficient power for digital logic circuits and extremely low-noise power for analog circuits. Total efficiency is more than 60%, delivering 55 watts of power while dissipating less than 35 watts.

The universal input transformer allows operation from foreign and domestic primary power sources, merely by making internal connections to the appropriate transformer terminals. Excellent isolation and shielding are provided between the input stage, the ±15V section, and the +5V section, thereby eliminating ground loops and crosstalk. Large annoying turn-on current surges, common to competitive high-efficiency power supplies, are also minimized.

Characterized by low noise and ripple, fast transient response, and tight line/load regulation, the series-pass linear ±15V regulator outputs feature constant-current protection. When either output is loaded heavily so less than 10 volts are generated, an on-off cycling operation is automatically initiated, thus minimizing power supply dissipation. Normal operation resumes when the overload is removed.

By incorporating high-speed transistors, ultra-fast diodes, moly-permalloy inductors, and four-terminal low-inductance capacitors, the +5V state-of-the-art switching regulator achieves high efficiency and operates at a nominal 30kHz for fast transient response and remarkably low peak-to-peak ripple. No-load-to-full-load regulation is a tight ±0.4%, with constant-current limiting for overload protection. Overvoltage protection is available as an option.

The U-shaped AN3007 metal case is structured for side-mounting to a standard 5.25-inch high chassis, allowing direct chassis contact for heat sinking and freeing the front and rear chassis panels for other component emplacement. The matching U-shaped perforated cover facilitates natural air convection for cooling, eliminating the need for fan-forced air or for cooling fins. Internally, major heat-generating components are bolted directly to the metal case; the other components are installed on two PC cards. Interconnections are of the plug-in quick-disconnect type for rapid disassembly and re-assembly — no soldering is required. Externally, the input and output terminals are vertically aligned on a single terminal strip for accessiblity and service-ability.

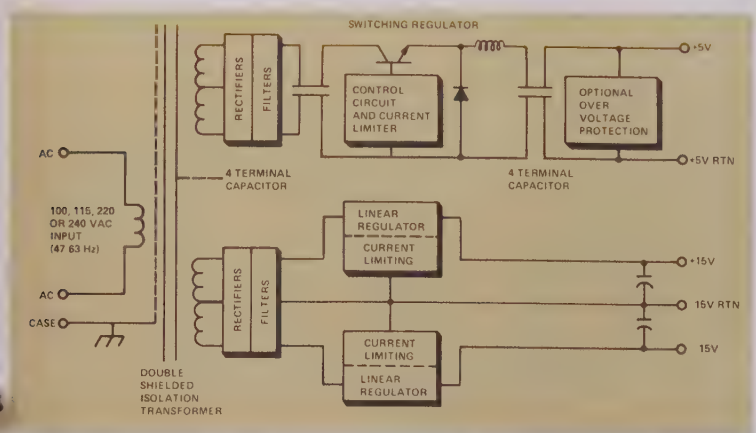


Figure 1. AN3007 Functional Block Diagram

FEATURES

- Furnishes triple outputs: +5Vdc @ 5A, +15Vdc @ 1A & −15Vdc @ 1A
- High Efficiency: >60% under full-load & nominal input conditions
- Adjustable outputs: +5V ±10%, +15V ±7% & −15V ±7%
- Universal shielded transformer for minimal noise coupling, effective input/output isolation & user-selectable 100, 115, 220 or 240Vac (47 to 63Hz)
- Tight control of no-load to full-load regulation: +5V 0.4% & ±15V 0.04%
- Superior high (+10%) to low (−15%) line regulation: +5V 0.4% & ±15V 0.04%
- Excellent load transient response: +5V changes only 150mV & recovers within 400μs for 2A load current step; ±15V changes only 100mV & recovers within 300μs for 0.5A load current step
- Extremely low noise & ripple: 25mV rms for +5V; 1mV rms for ±15V
- Short-circuit current protected
- Self-tracking ±15V for optimum analog balance
- Self-cooling — no fans or fins needed
- Lightweight, compact, metal chassis & perforated cover for side-mounting

APPLICATIONS

- Powering A/D/A circuits, subsystems & systems
- Complete powering of data conversion instruments
- Providing power for large digital logic arrays
- Powering analog & digital modules and DIP packages

ANALOGIC®
. . . The Digitizers

AN3007 SPECIFICATIONS

INPUT CHARACTERISTICS

Input Voltage	100, 115, 220 or 240Vac, −15%, +10%, 47 to 63Hz (Internally selectable)
Input Power	90W (full load); 5W (no load)
Efficiency @ Nominal Input & Full Load	>60%

OUTPUT CHARACTERISTICS

Output Voltages and Currents

+5Vdc	5A
+15Vdc	1A
−15Vdc	1A

Voltage Adjustment Range

+5Vdc	±0.5V
+15Vdc	±1.0V
−15Vdc	±1.0V

No Load-to-Full Load Regulation

+5Vdc	0.4%
+15Vdc	0.04%
−15Vdc	0.04%

Low Line-to-High Line Regulation

+5Vdc	0.4%
+15Vdc	0.04%
−15Vdc	0.04%

Noise & Ripple

+5Vdc	25mV rms; 70mV p-p
+15Vdc	1mV rms; 5mV p-p
−15Vdc	1mV rms; 5mV p-p

Load Switching Transient Response

+5Vdc	For 1A to 3A step, 150mV deviation & 400μs recovery
+15Vdc	For 0.2A to 0.7A step, 100mV deviation & 300μs recovery
−15Vdc	For 0.2A to 0.7A step, 100mV deviation & 300μs recovery

Short Circuit Current

+5Vdc	6A to 8A
+15Vdc	1.2A to 1.7A (Cycles off & on)
−15Vdc	1.2A to 1I7A (Cycles off & on)

ENVIRONMENTAL & PHYSICAL

Operating Temperature Range	0° to +70°C
Storage Temperature Range	−10°C to +85°C
Relative Humidity	0 to 95%, noncondensing
Weight	<8 pounds (<3.6kg)
Dimensions	8.31 x 3.94 x 3.95 inches (211 x 100 x 100mm)
Baseplate Temperature	+60°C max.

ORDERING GUIDE

Simply Specify: **AN3007 –** ☐

For	*Enter*
Overvoltage Protection (+5VDC)	**OVP**

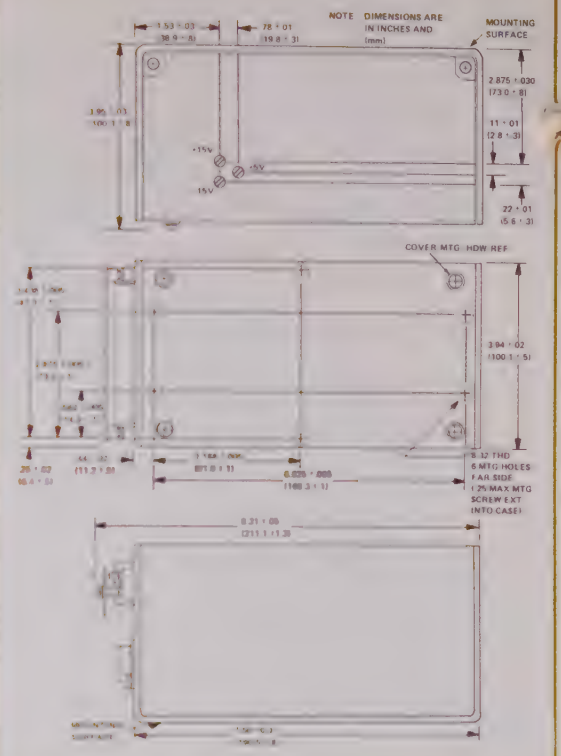
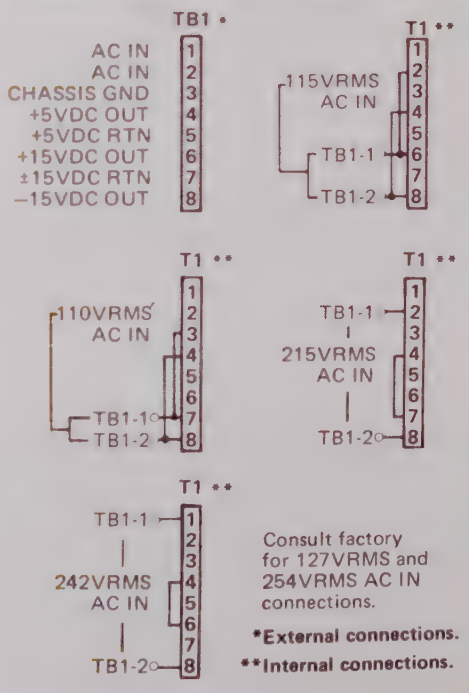


Figure 2. Outline and Mounting Dimensions

TRANSFORMER POWER CONNECTIONS



Consult factory for 127VRMS and 254VRMS AC IN connections.

*External connections.

**Internal connections.

ANALOGIC

ANALOGIC INTERNATIONAL
Audubon Road ■ Wakefield, Massachusetts 01880
Tel. (617) 246-0300 ■ TWX (710) 348-0425 ■ Telex 94-9307

ANALOGIC LIMITED
68 High Street ■ Weybridge, Surrey KT13 8BN ■ England
Tel. Wey 41251 ■ Telex (851) 928030

ANALOGIC REGIONAL OFFICES
San Jose, Calif. (408) 247-6401 ■ Tustin, Calif. (714) 838-7243
Cincinnati, Ohio (606) 371-0064

AVAILABLE FROM:

Bulletin No. 16-100084 REV 1

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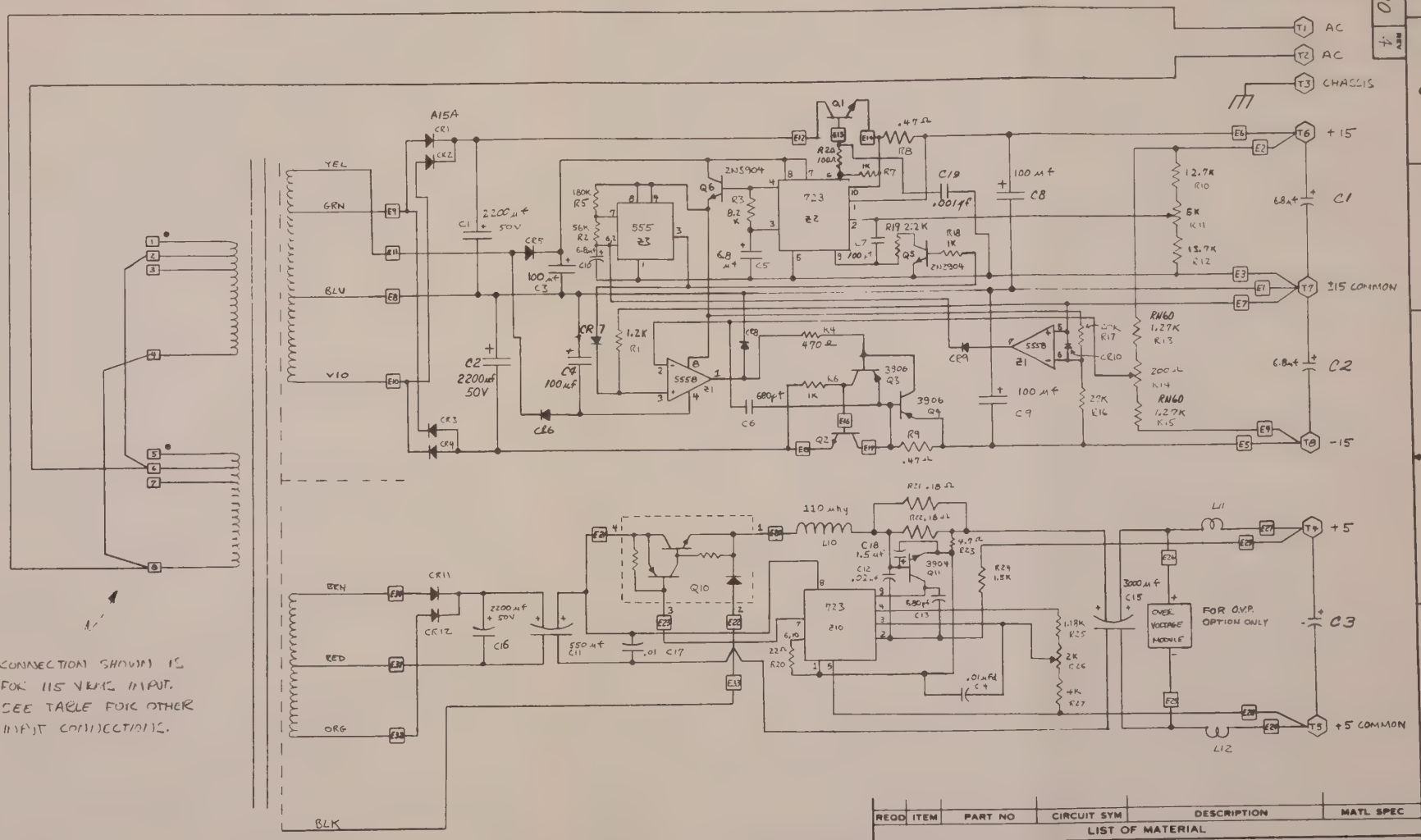
REV.	ECO	DESCRIPTION	DWN	APP'D	DATE
4	4-382 4-583 4-622	SEE E.C.O.'S	RB	D.P	2-22-90

REVISIONS

REV	ECO	DESCRIPTION	DWN	APP'D	DATE
2	7-0638 7-0639	SEE ECO. SEE ECO	BR BR	JRG JRG	12/21/76 12/21/76
3	4-0005 4-0006 7-0769	SEE E.C.O.	JK	J.T.P.	4/4/77

SIZE C | 5-7420 | REV 4



CONNECTION SHOWN IS FOR 115 VRMS INPUT. SEE TABLE FOR OTHER INPUT CONNECTIONS.

INPUT VOLTAGE	INPUT TERMINALS	JUMPERS	INPUT VOLTAGE	INPUT TERMINALS	JUMPERS
100	7,8	5-7, 4-8	215	2,8	4-7
115	6,8	2-6, 4-8	242	1,8	4-6
127	5,8	1-6, 4-8	259	1,8	4-5

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

PL10-2037	AN3007
PL10-7422	AN3007,15V BD
PL10-7421	AN3007,5V BD
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	RWH	12-18-75
CHECKED		3/2/76
DESIGNER		8-17-76
ENGINEER		8-19-76
APPROVED		
RELEASED		8/19/76
WEIGHT		

ANALOGIC WAKEFIELD, MASS. 01880

AN3007 POWER SUPPLY

CODE IDENT NO	SIZE		REV
31814	C	5-7420	4
SCALE —	ACCOUNT NO —	SHEET 1 OF 1	

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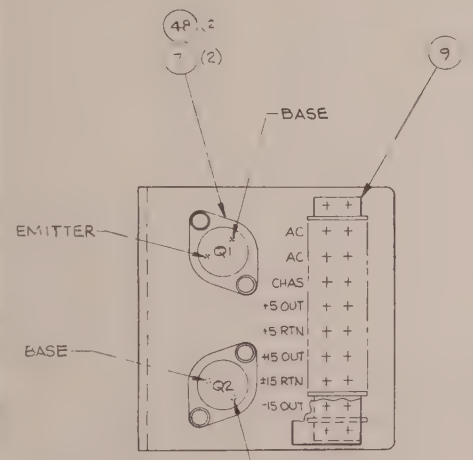
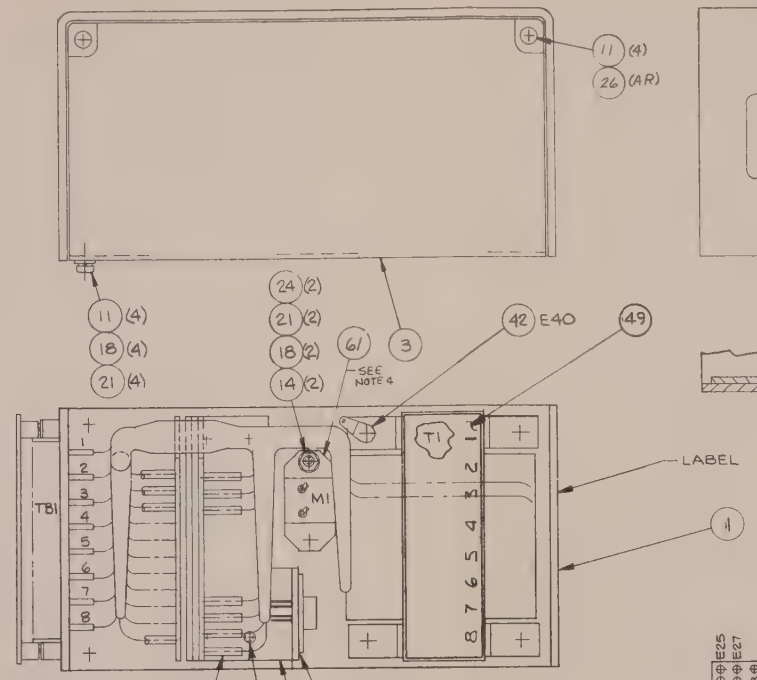
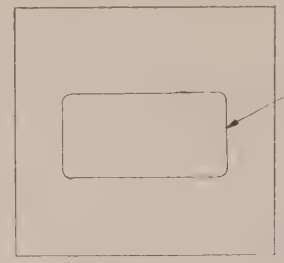
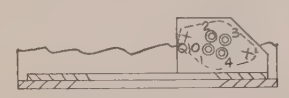
REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPL'S	DATE
1	—	ADDED NOTE 2, ITEM 42 & REV DOC TABLE	RSJ	RSJ	8 MAR 76
2	-	ADDED: ITEMS 48, 47, 46, 45, 44 & WIRE LENGTHS & LABEL	T.B.	RSJ	
3	7-0677	SEE E.C.O	RSP		18 OCT 76
4	4-0073 7-0748 7-0778	SEE ECO.	J.P.		3/28/77
5	7-0788	CHANGED WIRE 34 ADD E33	J.L.		4-28-77
6	4-0051	WIRES 32-33 WERE ITEMS 38-37	J.L.		7-13-77
7	4-0073	ITEM 46 WAS ITEM 11	J.L.		8-23-77
8	4-0127	SEE E.C.O	J.L.		11-21-77
9	4-0134	SEE E.C.O	J.L.		5-21-78
10	4-0217	ADD FLAT WASHER ITEM 21	J.L.		6-25-78
11	4-0249	SEE E.C.O.	L.R.		6-6-78
12	4-0291	SEE ECO	D.F.		10-5-78
13	4-1350	SEE E.C.O	D.F.		6-16-80

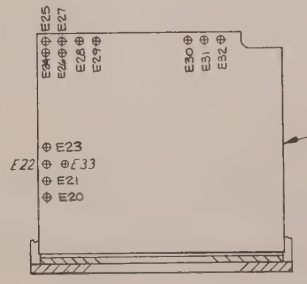
7-1537

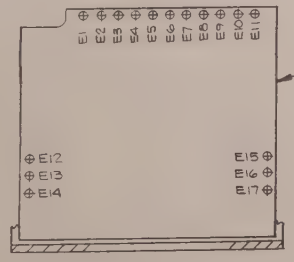


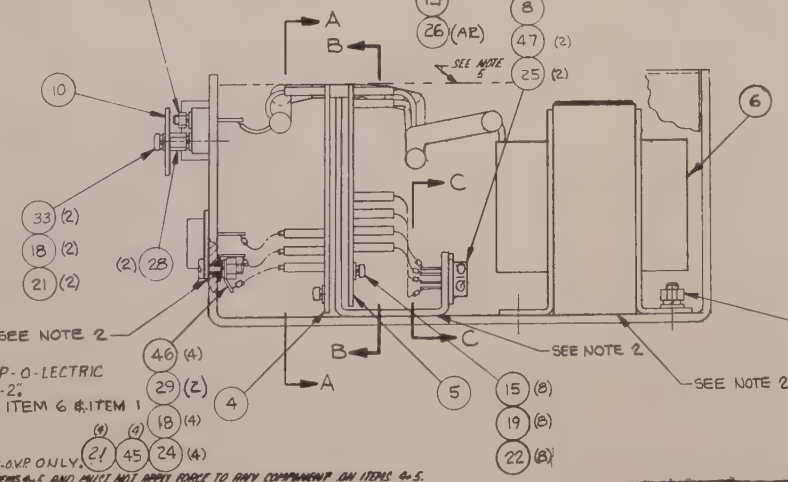












SECTION A-A

NOTES:
1. TO ASSEMBLE ITEM NO. 32, STRIP 12 & CRIMP USING AMP-O-LECTRIC MODEL "K" PRESS WITH MINI-APPLICATOR AMP #466469-2.
2. APPLY ITEM 30 BETWEEN ITEM 1 & ITEM 2, ITEM 6 & ITEM 1 ITEM 8 & ITEM 2, ITEM 7 & ITEM 1
3. STRIP .40 AND TIN WIRES AT TB1, E40, Q1, Q2, Q10
4. INSTALL ITEM 61 AND WIRES 32 AND 33 ON AN3007-OVP ONLY.
5. ALL WIRES MUST BE ASSEMBLED BELOW A LINE EVEN WITH THE TOP EDGE OF ITEMS 4 & 5 AND MUST NOT APPLY FORCE TO ANY COMPONENT ON ITEMS 4 & 5.

WIRING TABLE

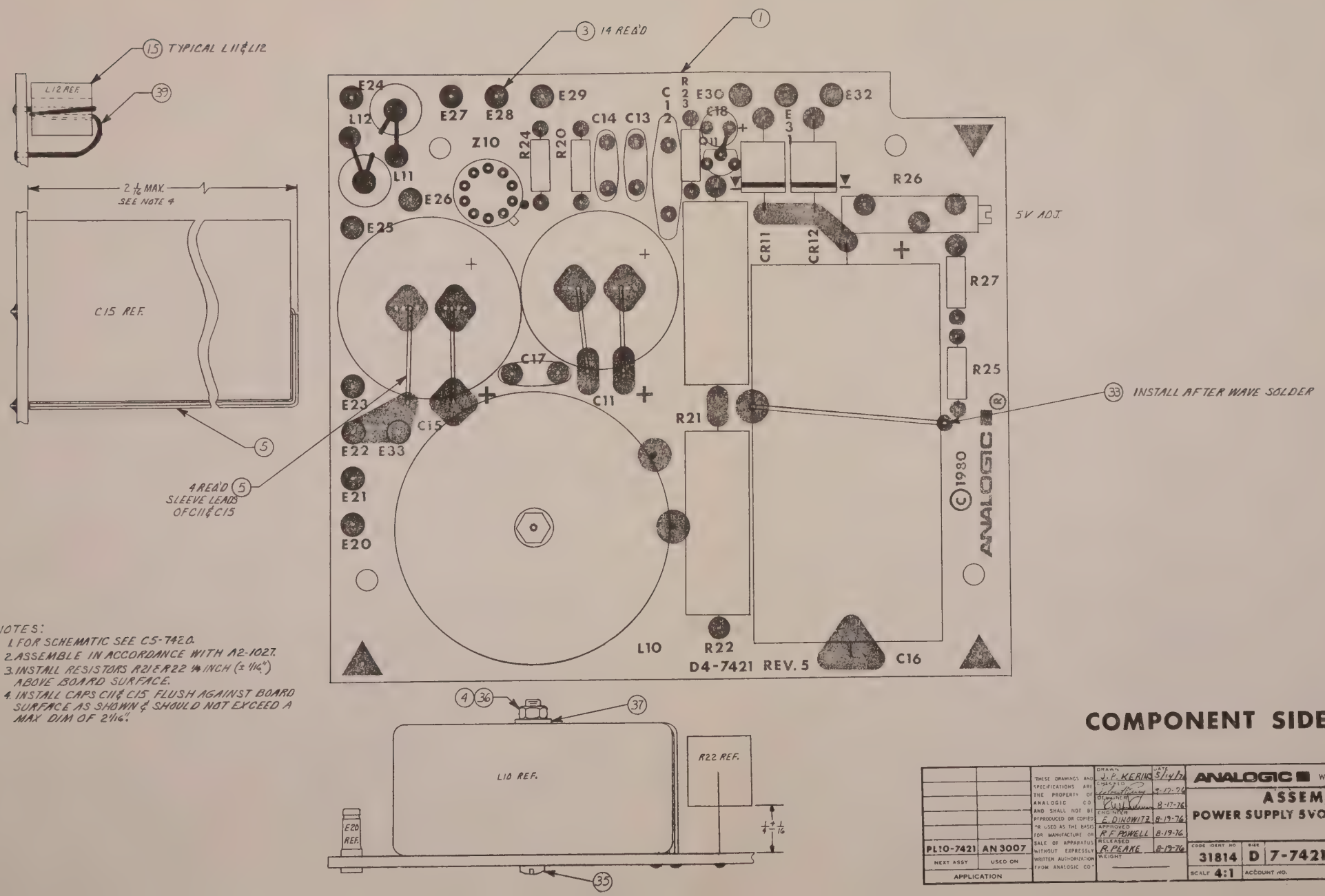
LENGTH IN INCHES	WIRE NO.	ITEM NO.	COLOR	SIZE	ASSEMBLE ITEM NO.	FROM	TO	FUNCTION
TWIST 12	1	35	BLK	20		T1-2	TB1-2	AC
12	2	34	WHT	20		T1-4	TB1-1	AC
10	3	36	BRN	20		E40	TB1-3	CHASSIS GND
10	4	37	YEL		/32	TB1-4	E27	+5 OUT
10	5	37	YEL		/32	TB1-4	E29	+5 OUT
10½	6	38	ORN			TB1-5	E24	+5 RTN
10½	7	38	ORN			TB1-5	E28	+5 RTN
4½	8	39	BLU			TB1-6	E2	+15 OUT
3	9	54	BLU			TB1-6	E6	+15 OUT
5½	10	40	GRY			TB1-7	E1	±15 RTN
5½	11	40	GRY			TB1-7	E3	±15 RTN
2½	12	53	GRY			TB1-7	E7	±15 RTN
4	13	52	VIO			TB1-8	E4	-15 OUT
4	14	52	VIO	20		TB1-8	E5	-15 OUT
	15	P/06	BLU	22		T1-16	E8	
	16		GRN	22		T1-15	E9	
	17		VIO	22		T1-17	E10	
	18		YEL	22		T1-14	E11	
	19		BRN	18		T1-11	E30	
	20		RED	18		T1-12	E31	
	21	P/06	ORN	18		T1-13	E32	
2½	22	53	GRY	20		Q1-C	E12	
3	23	54	BLU			Q1-B	E13	
3	24	55	VIO			Q1-E	E14	
2½	25	53	GRY			Q2-C	E17	
3	26	54	BLU			Q2-B	E16	
3	27	55	VIO			Q2-E	E15	
3	28	56	YEL			Q10-1	E20	
3	29	57	ORN			Q10-2	E22	
3	30	58	WHT			Q10-3	E23	
3	31	59	GRN			Q10-4	E21	
7	32	63	GRN		P/633/1	M1-NEG	E25	
7	33	62	BLK	20	P/633/32	M1-POS	E26	
—	34	P/06	BLK	22		T1-10	E33	
3	35	58	WHT	20		T1-2	T1-6	
3	36	60	BLK	20		T1-4	T1-8	
	37	43	—	—	— —	TB1-4(+)	TB1-5	(C3)
	38	43	—	—	— —	TB1-6(+)	TB1-7	(C1)
	39	43	—	—	— —	TB1-7(+)	TB1-8	(C2)

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC
LIST OF MATERIAL					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ±		DRAWN R. Sullivan	DATE 3 Jan 76	ANALOGIC WAKEFIELD, MASS. 01880	
MATERIAL		CHECKED RSJ	6 Aug 76	POWER SUPPLY AN3007 / AN3007-OVP	
FINISH		DESIGNER [illegible]	8-6-76		
		ENGINEER C. Donnelly	8-19-76		
		APPROVED [illegible]			
PL10-2037	AN3007	APPLICABLE SPECIFICATIONS	RELEASED [illegible]	9/7/76	CODE IDENT NO 31814 SIZE D 7-1537 REV 13
NEXT ASSY	USED ON		WEIGHT		SCALE 1/1 ACCOUNT NO. SHEET 1 OF 1
APPLICATION					

REVISIONS						
REV	E.C.O.	DESCRIPTION	DWN	APPR'D	DATE	
5	4582	SEE E.C.O.	KP	DP	2-21-80	

D 7-7421 5



NOTES:
1. FOR SCHEMATIC SEE C5-7420.
2. ASSEMBLE IN ACCORDANCE WITH A2-1027.
3. INSTALL RESISTORS R21 & R22 1/4 INCH (± 1/16") ABOVE BOARD SURFACE.
4. INSTALL CAPS C11 & C15 FLUSH AGAINST BOARD SURFACE AS SHOWN & SHOULD NOT EXCEED A MAX DIM OF 2 1/16".

COMPONENT SIDE

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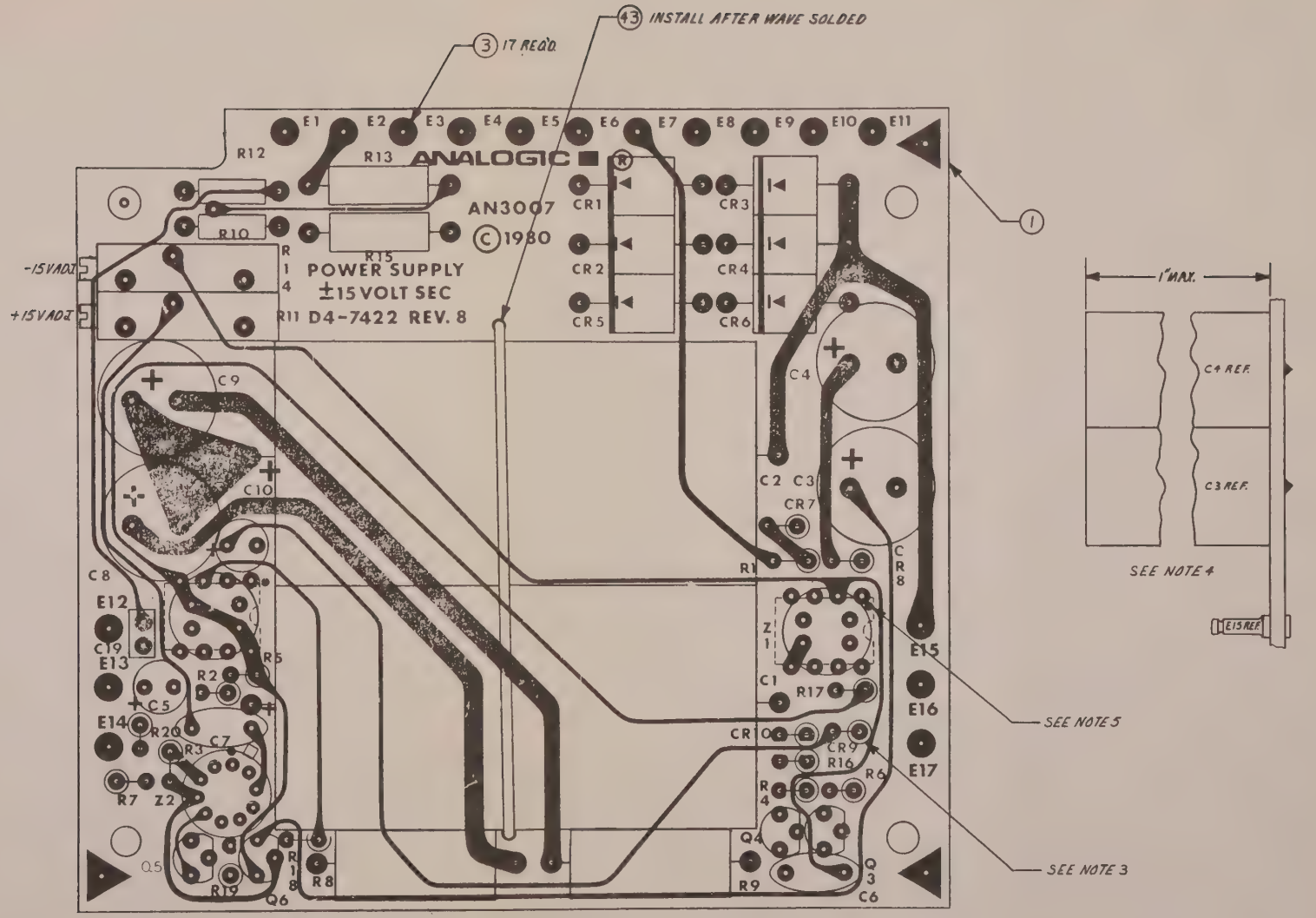
			CHECKED [illegible] 8-17-76	ASSEMBLY POWER SUPPLY 5VOLT SECTION	
			OTHER [illegible] 8-17-76		
			TYD NOTE E. DINOWITZ 8-19-76		
			APPROVED R.F. POWELL 8-19-76		
PL10-7421	AN 3007		RELEASED R. PEAKE 8-19-76		
NEXT ASSY	USED ON		WEIGHT	CODE IDENT NO 31814	SIZE D 7-7421 REV 5
APPLICATION				SCALE 4:1	ACCOUNT NO. SHEET 1 OF 1

REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPD	DATE
8	4-583 4-622	SEE E.C.O.'S	RP	DH	2-27-76

D 7-7422 8



NOTES:
1. FOR SCHEMATIC SEE C.S-7420.
2. ASSEMBLE IN ACCORDANCE WITH A2-1027.
3. INSTALL ALL VERTICAL DIODES WITH ANODE END FLUSH AGAINST BOARD SURFACE.
4. INSTALL CAPS C3, C4, C8 & C9 FLUSH AGAINST BOARD SURFACE.
5. DOT INDICATES PIN 1 OF I.C.'S.

COMPONENT SIDE

		DRAWN	R.COLLINS	12-2-75
		CHECKED	R.PERRY	3-2-76
		DES. SUP.		8-11-76
		ENGINEER	E. DINOMITE	8-19-76
		APPROVED	R.F.POWELL	8-19-76
		RELEASED	R.PEAKE	8-19-76
PL10-2070	AN 3008	WEIGHT		
PL10-7422	AN 3007			
NEXT ASSY	USED ON			

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ANALOGIC WAKEFIELD, MASS. 01880

ASSEMBLY
POWER SUPPLY 15VOLT SECTION

DRAWING NO	SIZE		REV
31814	D	7-7422	8
SCALE 4:1	ACCOUNT NO.		SHEET 1 OF 1

8 QUALITY CONFORMANCE

8.0 General

The success of Analogic Corporation has resulted from our expertise in solving our customers' engineering problems. In line with advanced manufacturing theories, our Engineering, Manufacturing and Quality Assurance (QA) Departments work together with open communication channels to assure our products conform to specification requirements.

8.1 Quality of Design

8.1.1 Product Design

The Project Manager's in-depth understanding of specification parameters and electronics circuit theory assures the quality of each product's design. During the initial design, the prototype is tested under the Project Manager's close supervision for its conformance to all design requirements. After the prototype is acceptable to product design, a limited quantity of parts are released for pre-production manufacturing. During the pre-production phase the Product Engineer monitors all aspects of manufacturing, from procuring parts to final testing and shipping. Based on pre-production findings, the Engineering Department adds to or deletes from the product's documentation to finalize the specifications. When the final design is completed, all the parts are submitted to QA and Manufacturing for final release for full production.

During pre-production, a lead inspector reviews and crosschecks the assembly with the parts list and assembly drawing, a final QA technician reviews the test procedure and data sheet to pinpoint any omissions or errors, and both findings are conveyed to the Engineering Department through the QA supervisor for any documentation update.

8.1.2 Component Specifications

There are several thousand approved component specifications. If a new part specification is needed, the Project Manager delineates the electro-mechanical parameters, and Component Engineering conducts tests and issues a new part number.

8.1.3 Documentation

Product Engineering is responsible for all documentation with respect to each product's specifications. QA reviews all documents for concurrence with Analogic's engineering standards, and no product documentation is acceptable without the QA verification.

Each product must have the following:

1. Parts List, with a full set of released Analogic part numbers.
2. Assembly Drawing
3. Schematic
4. Test Procedure
5. Theory of Operation
6. Product Specification

8.2 Quality of Components

8.2.1 Purchasing

Purchasing can procure components only with fully released documentation. Only quality approved vendors are permissible sources for production components. If any special requirements must be met, the additional quality inputs are given to Purchasing as part of the purchasing conditions.

8.2.2 Incoming Inspection

Incoming Inspection, with its own fully automated computer tester and IC burn-in capability to handle Analogic's increasing needs, verifies that all components conform to specifications in accordance with the component inspection folder and Analogic's sample plan. Component aging, burn-in, and specially selected parts (required to have special marking for identification), fall within the responsibilty of Incoming Inspection.

8.2.3 Storage

Only components accepted by Incoming Inspection are allowed in the parts stock, and the stockbins are purged in the event any problem is reported to QA. Component storage is audited by QA to assure proper stock handling.

8.3 Quality of Manufacturing

The manufacturing operation is continually upgrading its printed circuit board (PCB) assembly processes. IC's and components are mounted by semi-automatic insertion equipment. Wave soldering is done by a completely integrated process from the initial flux wax stabilization to the final wash dry cycle.

Patrol inspection and first-piece inspection have been instituted to assure the Quality Conformance of these high-speed processes. In addition, tollgate inspection stations, operating on a sampling basis, are established

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